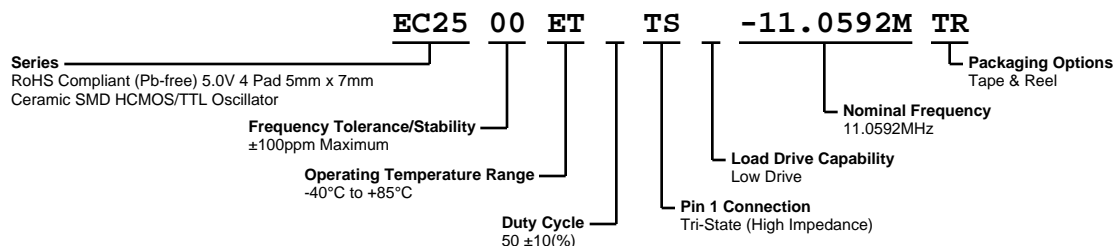


EC2500ETTS-11.0592M TR



ECLIPTEK
CORPORATION



ELECTRICAL SPECIFICATIONS

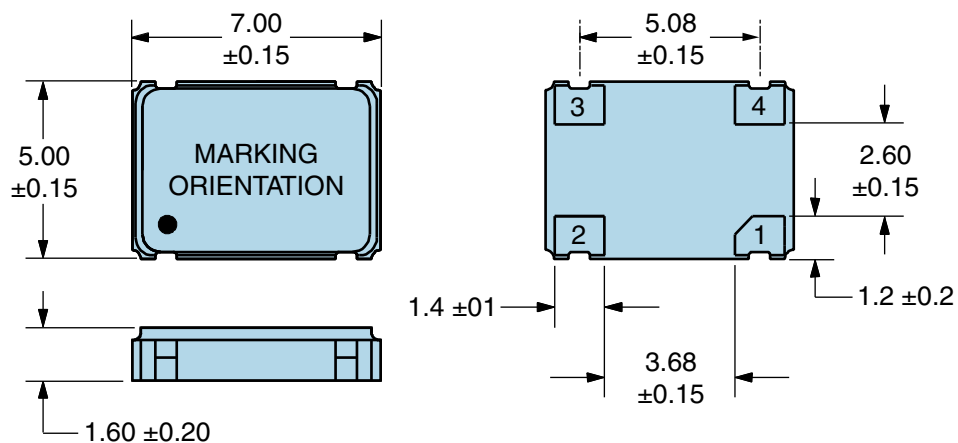
| | |
|---------------------------------------|---|
| Nominal Frequency | 11.0592MHz |
| Frequency Tolerance/Stability | ± 100 ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C , Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C , Shock, and Vibration) |
| Aging at 25°C | ± 5 ppm/year Maximum |
| Operating Temperature Range | -40°C to $+85^{\circ}\text{C}$ |
| Supply Voltage | 5.0Vdc $\pm 10\%$ |
| Input Current | 10mA Maximum (No Load) |
| Output Voltage Logic High (Voh) | 2.4Vdc Minimum with TTL Load, Vdd-0.5Vdc Minimum with HCMOS Load |
| Input Current Logic High (Ioh) | -4mA |
| Output Voltage Logic Low (Vol) | 0.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load |
| Input Current Logic Low (Iol) | 4mA |
| Rise/Fall Time | 10nSec Maximum (Measured at 0.4Vdc to 2.4Vdc with TTL Load; Measured at 10% to 90% of waveform with HCMOS Load) |
| Duty Cycle | $50 \pm 10(\%)$ (Measured at 50% of waveform with HCMOS Load or at 1.4Vdc with TTL Load) |
| Load Drive Capability | Low Drive (10LSTTL Load or 30pF HCMOS Load Maximum) |
| Output Logic Type | CMOS |
| Pin 1 Connection | Tri-State (High Impedance) |
| Tri-State Input Voltage (Vih and Vil) | +2.0Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output. |
| RMS Phase Jitter | 1pSec Maximum (12kHz to 20MHz offset frequency) |
| Start Up Time | 10mSec Maximum |
| Storage Temperature Range | -55°C to $+125^{\circ}\text{C}$ |

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

| | |
|------------------------------|---------------------------------------|
| Fine Leak Test | MIL-STD-883, Method 1014, Condition A |
| Gross Leak Test | MIL-STD-883, Method 1014, Condition C |
| Mechanical Shock | MIL-STD-202, Method 213, Condition C |
| Resistance to Soldering Heat | MIL-STD-202, Method 210 |
| Resistance to Solvents | MIL-STD-202, Method 215 |
| Solderability | MIL-STD-883, Method 2003 |
| Temperature Cycling | MIL-STD-883, Method 1010 |
| Vibration | MIL-STD-883, Method 2007, Condition A |

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MECHANICAL DIMENSIONS (all dimensions in millimeters)



| PIN | CONNECTION |
|-----|----------------|
| 1 | Tri-State |
| 2 | Ground |
| 3 | Output |
| 4 | Supply Voltage |

| LINE | MARKING |
|------|--|
| 1 | ECLIPTEK |
| 2 | 11.059M |
| 3 | XXYYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year |

Suggested Solder Pad Layout

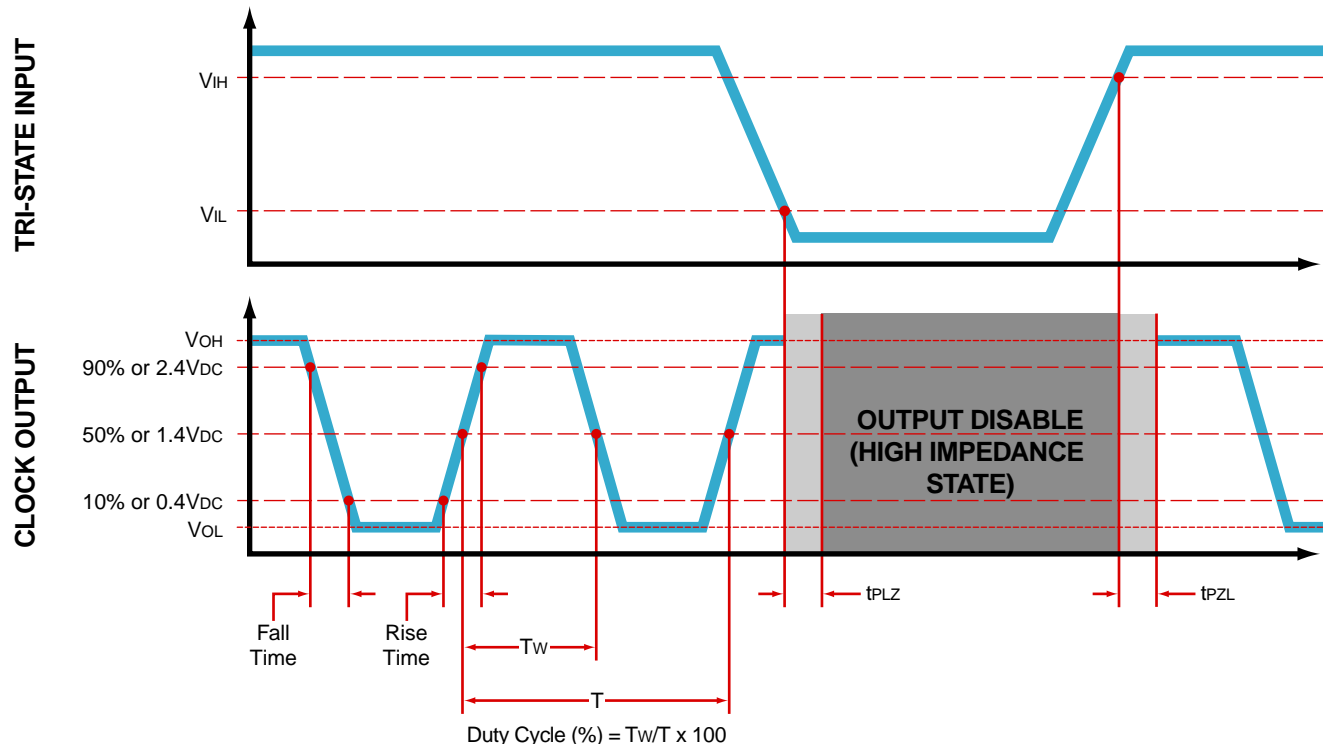
All Dimensions in Millimeters



All Tolerances are ±0.1

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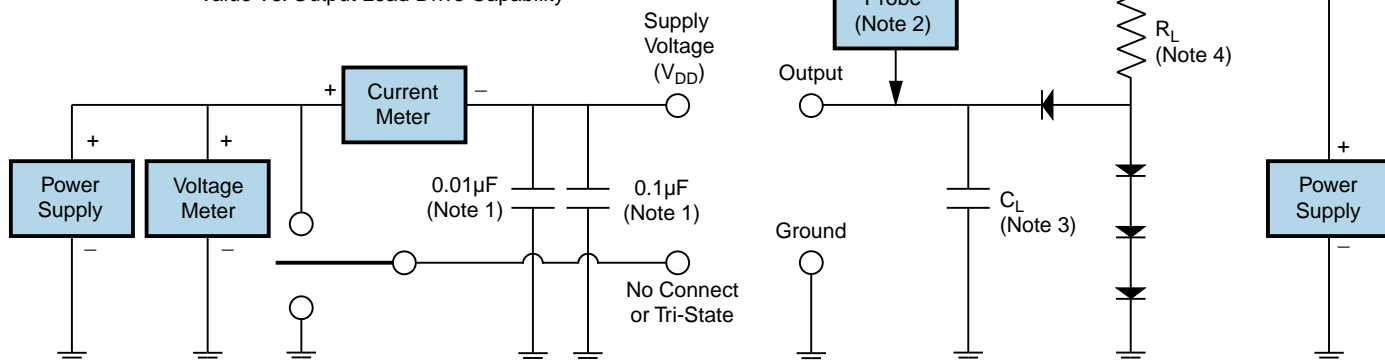
OUTPUT WAVEFORM & TIMING DIAGRAM



Test Circuit for TTL Output

| Output Load Drive Capability | R_L Value (Ohms) | C_L Value (pF) |
|------------------------------|--------------------|------------------|
| 10TTL | 390 | 15 |
| 5TTL | 780 | 15 |
| 2TTL | 1100 | 6 |
| 10LSTTL | 2000 | 15 |
| 1TTL | 2200 | 3 |

Table 1: R_L Resistance Value and C_L Capacitance Value Vs. Output Load Drive Capability



Note 1: An external 0.1μF low frequency tantalum bypass capacitor in parallel with a 0.01μF high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

Note 4: Resistance value R_L is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.

Note 5: All diodes are MMBD7000, MMBD914, or equivalent.

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Test Circuit for CMOS Output

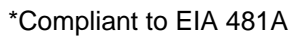


Note 1: An external $0.1\mu\text{F}$ low frequency tantalum bypass capacitor in parallel with a $0.01\mu\text{F}$ high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance ($<12\text{pF}$), 10X attenuation factor, high impedance ($>10\text{Mohms}$), and high bandwidth ($>300\text{MHz}$) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

Quantity Per Reel: 1,000 units



Recommended Solder Reflow Methods



High Temperature Infrared/Convection

| | |
|--|---|
| T_S MAX to T_L (Ramp-up Rate) | 3°C/second Maximum |
| Preheat | |
| - Temperature Minimum (T_S MIN) | 150°C |
| - Temperature Typical (T_S TYP) | 175°C |
| - Temperature Maximum (T_S MAX) | 200°C |
| - Time (t_s MIN) | 60 - 180 Seconds |
| Ramp-up Rate (T_L to T_P) | 3°C/second Maximum |
| Time Maintained Above: | |
| - Temperature (T_L) | 217°C |
| - Time (t_L) | 60 - 150 Seconds |
| Peak Temperature (T_P) | 260°C Maximum for 10 Seconds Maximum |
| Target Peak Temperature (T_P Target) | 250°C +0/-5°C |
| Time within 5°C of actual peak (t_p) | 20 - 40 seconds |
| Ramp-down Rate | 6°C/second Maximum |
| Time 25°C to Peak Temperature (t) | 8 minutes Maximum |
| Moisture Sensitivity Level | Level 1 |
| Additional Notes | Temperatures shown are applied to body of device. |

Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T_S MAX to T_L (Ramp-up Rate) 5°C/second Maximum

Preheat

- Temperature Minimum (T_S MIN) N/A
- Temperature Typical (T_S TYP) 150°C
- Temperature Maximum (T_S MAX) N/A
- Time (t_s MIN) 60 - 120 Seconds

Ramp-up Rate (T_L to T_P) 5°C/second Maximum

Time Maintained Above:

- Temperature (T_L) 150°C
- Time (t_L) 200 Seconds Maximum

Peak Temperature (T_P) 240°C Maximum

Target Peak Temperature (T_P Target) 240°C Maximum 1 Time / 230°C Maximum 2 Times

Time within 5°C of actual peak (t_p) 10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time

Ramp-down Rate 5°C/second Maximum

Time 25°C to Peak Temperature (t) N/A

Moisture Sensitivity Level Level 1

Additional Notes Temperatures shown are applied to body of device.

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)