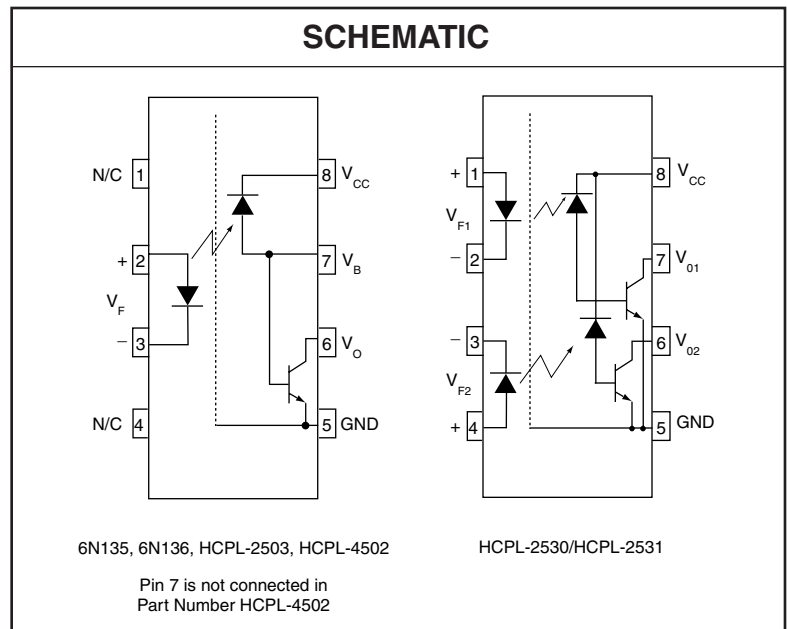
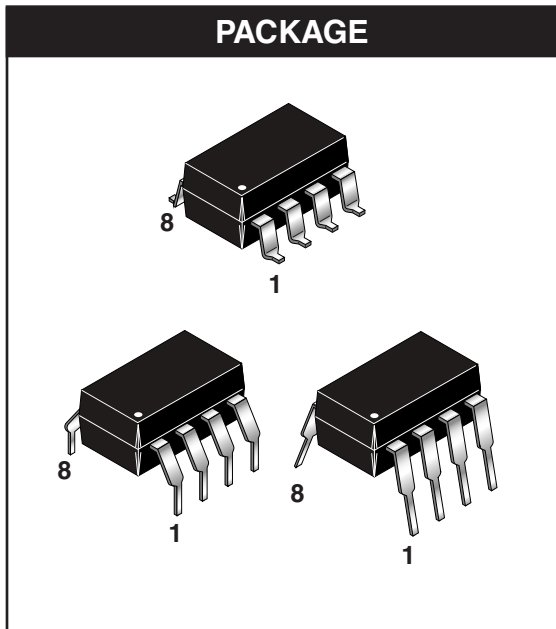


SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

HCPL-2503

HCPL-4502



DESCRIPTION

The HCPL-4502/HCPL-2503, 6N135/6 and HCPL-2530/HCPL-2531 optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

An internal noise shield provides superior common mode rejection of 10kV/μs. An improved package allows superior insulation permitting a 480 V working voltage compared to industry standard of 220 V.

FEATURES

- High speed-1 MBit/s
- Superior CMR-10 kV/μs
- Dual-Channel HCPL-2530/HCPL-2531
- Double working voltage-480V RMS
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)

APPLICATIONS

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

HCPL-2503

HCPL-4502

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	T_{STG}	-55 to +125	$^\circ\text{C}$
Operating Temperature	T_{OPR}	-55 to +100	$^\circ\text{C}$
Lead Solder Temperature	T_{SOL}	260 for 10 sec	$^\circ\text{C}$
EMITTER			
DC/Average Forward Input Current	Each Channel (Note 1)	I_F (avg)	25 mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	Each Channel (Note 2)	I_F (pk)	50 mA
Peak Transient Input Current - ($\leq 1 \mu\text{s}$ P.W., 300 pps)	Each Channel	I_F (trans)	1.0 A
Reverse Input Voltage	Each Channel	V_R	5 V
Input Power Dissipation	(6N135/6N136 and HCPL-2503/4502) (HCPL-2530/2531) Each Channel (Note 3)	P_D	100 45 mW
DETECTOR			
Average Output Current	Each Channel	I_O (avg)	8 mA
Peak Output Current	Each Channel	I_O (pk)	16 mA
Emitter-Base Reverse Voltage	(6N135, 6N136 and HCPL-2503 only)	V_{EBR}	5 V
Supply Voltage		V_{CC}	-0.5 to 30 V
Output Voltage		V_O	-0.5 to 20 V
Base Current	(6N135, 6N136 and HCPL-2503 only)	I_B	5 mA
Output power dissipation	(6N135, 6N136, HCPL-2503, HCPL-4502) (Note 4) (HCPL-2530, HCPL-2531) Each Channel	P_D	100 35 mW

SINGLE-CHANNEL: 6N135

6N136

HCPL-2503

HCPL-4502

DUAL-CHANNEL: HCPL-2530

HCPL-2531

ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER Input Forward Voltage	($I_F = 16$ mA, $T_A = 25^\circ\text{C}$)	V_F			1.45	1.7	V
	($I_F = 16$ mA)				1.8		
Input Reverse Breakdown Voltage	($I_R = 10$ μA)	B_{VR}		5.0			V
Temperature coefficient of forward voltage	($I_F = 16$ mA)	$(\Delta V_F / \Delta T_A)$			-1.6		mV/ $^\circ\text{C}$
DETECTOR Logic high output current	($I_F = 0$ mA, $V_O = V_{CC} = 5.5$ V) ($T_A = 25^\circ\text{C}$)	I_{OH}	All		0.001	0.5	μA
	($I_F = 0$ mA, $V_O = V_{CC} = 15$ V) ($T_A = 25^\circ\text{C}$)		6N135 6N136 HCPL-4502 HCPL-2503		0.005	1	
	($I_F = 0$ mA, $V_O = V_{CC} = 15$ V)		All			50	
Logic low supply current	($I_F = 16$ mA, $V_O = \text{Open}$) ($V_{CC} = 15$ V)	I_{CCL}	6N135 6N136 HCPL-4502 HCPL-2503		120	200	μA
	($I_{F1} = I_{F2} = 16$ mA, $V_O = \text{Open}$) ($V_{CC} = 15$ V)		HCPL-2530 HCPL-2531		200	400	
Logic high supply current	($I_F = 0$ mA, $V_O = \text{Open}$, $V_{CC} = 15$ V) ($T_A = 25^\circ\text{C}$)	I_{CCH}	6N135 6N136 HCPL-4502 HCPL-2503			1	μA
	($I_F = 0$ mA, $V_O = \text{Open}$) ($V_{CC} = 15$ V)		6N135 6N136 HCPL-4502 HCPL-2503			2	
	($I_F = 0$ mA, $V_O = \text{Open}$) ($V_{CC} = 15$ V)		HCPL-2530 HCPL-2531		0.02	4	

** All Typical at $T_A = 25^\circ\text{C}$

SINGLE-CHANNEL: 6N135

6N136

HCPL-2503

HCPL-4502

DUAL-CHANNEL: HCPL-2530

HCPL-2531

TRANSFER CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit		
COUPLED Current transfer ratio (Note 5)	$(I_F = 16 \text{ mA}, V_O = 0.4 \text{ V})$ $(V_{CC} = 4.5 \text{ V}, T_A = 25^\circ\text{C})$	CTR	6N135 HCPL-2530	7	18	50	%		
			6N136 HCPL-4502 HCPL-2531	19	27	50	%		
			HCPL-2503	12	27		%		
	$V_{OL}=0.4\text{V}$ $V_{OL}=0.5\text{V}$		6N135 HCPL-2530	5	21		%		
	$(I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V})$ $V_{OL}=0.4\text{V}$ $V_{OL}=0.5\text{V}$ $V_{OL}=0.4\text{V}$							6N136 HCPL-4502 HCPL-2531	15
			HCPL-2503	9	30		%		
	Logic low output voltage output voltage		$(I_F = 16 \text{ mA}, I_O = 1.1 \text{ mA})$ $(V_{CC} = 4.5 \text{ V}, T_A = 25^\circ\text{C})$	V _{OL}	6N135		0.18	0.4	V
					HCPL-2530		0.18	0.5	
			6N136 HCPL-2503			0.25	0.4		
			HCPL-2531			0.25	0.5		
$(I_F = 16 \text{ mA}, I_O = 0.8 \text{ mA})$ $(V_{CC} = 4.5 \text{ V})$		6N135 HCPL-2530				0.5			
$(I_F = 16 \text{ mA}, I_O = 2.4 \text{ mA})$ $(V_{CC} = 4.5 \text{ V})$		HCPL-4502 HCPL-2531				0.5			

** All Typicals at $T_A = 25^\circ\text{C}$

SINGLE-CHANNEL: 6N135

6N136

HCPL-2503

HCPL-4502

DUAL-CHANNEL: HCPL-2530

HCPL-2531

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C unless otherwise specified., $V_{CC} = 5\text{ V}$)							
Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low	$T_A = 25^\circ\text{C}$, ($R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)	T_{PHL}	6N135 HCPL-2530		0.45	1.5	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7) $T_A = 25^\circ\text{C}$		6N136 HCPL-4502 HCPL-2503 HCPL-2531		0.45	0.8	μs
	$(R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)		6N135 HCPL-2530			2.0	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7)		6N136 HCPL-4502 HCPL-2503 HCPL-2531			1.0	μs
Propagation delay time to logic high	$T_A = 25^\circ\text{C}$, ($R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)	T_{PLH}	6N135 HCPL-2530		0.5	1.5	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7) $T_A = 25^\circ\text{C}$		6N136 HCPL-4502 HCPL-2503 HCPL-2531		0.3	0.8	μs
	$(R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 6) (Fig. 7)		6N135 HCPL-2530			2.0	μs
	$(R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$) (Note 7) (Fig. 7)		6N136 HCPL-4502 HCPL-2503 HCPL-2531			1.0	μs
Common mode transient immunity at logic high	$(I_F = 0\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$) (Note 8) (Fig. 8) $T_A = 25^\circ\text{C}$	ICM_{HI}	6N135 HCPL-2530		10,000		$\text{V}/\mu\text{s}$
	$(I_F = 0\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$) $T_A = 25^\circ\text{C}$, ($R_L = 1.9\text{ k}\Omega$) (Note 8) (Fig. 8)		6N136 HCPL-4502 HCPL-2503 HCPL-2531		10,000		$\text{V}/\mu\text{s}$
Common mode transient immunity at logic low	$(I_F = 16\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$) (Note 8) (Fig. 8) $T_A = 25^\circ\text{C}$	ICM_{LI}	6N135 HCPL-2530		10,000		$\text{V}/\mu\text{s}$
	$(I_F = 16\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$) ($R_L = 1.9\text{ k}\Omega$) (Note 8) (Fig. 8)		6N136 HCPL-4502 HCPL-2503 HCPL-2531		10,000		$\text{V}/\mu\text{s}$

** All Typical at $T_A = 25^\circ\text{C}$

SINGLE-CHANNEL: 6N135

6N136

HCPL-2503

HCPL-4502

DUAL-CHANNEL: HCPL-2530

HCPL-2531

ISOLATION CHARACTERISTICS ($T_A = 0$ to 70°C Unless otherwise specified)						
Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) ($T_A = 25^\circ\text{C}$, $t = 5$ s) ($V_{I-O} = 3000$ VDC) (Note 9)	I_{I-O}			1.0	μA
Withstand insulation test voltage	($\text{RH} \leq 50\%$, $T_A = 25^\circ\text{C}$) (Note 9) ($t = 1$ min.)	V_{ISO}	2500			V_{RMS}
Resistance (input to output)	(Note 9) ($V_{I-O} = 500$ VDC)	R_{I-O}		10^{12}		Ω
Capacitance (input to output)	(Note 9) ($f = 1$ MHz)	C_{I-O}		0.6		pF
DC Current gain	($I_O = 3$ mA, $V_O = 5$ V)	HFE		150		
Input-Input Insulation leakage current	($\text{RH} \leq 45\%$, $V_{I-I} = 500$ VDC) (Note 10) $t = 5$ s, (HCPL-2530/2531 only)	I_{I-I}		0.005		μA
Input-Input Resistance	($V_{I-I} = 500$ VDC) (Note 10) (HCPL-2530/2531 only)	R_{I-I}		10^{11}		Ω
Input-Input Capacitance	($f = 1$ MHz) (Note 10) (HCPL-2530/2531 only)	C_{I-I}		0.03		pF

Notes

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/ $^\circ\text{C}$.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/ $^\circ\text{C}$.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/ $^\circ\text{C}$.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/ $^\circ\text{C}$.
5. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
6. The 4.1 k Ω load represents 1 LSTTL unit load of 0.36 mA and 6.1 k Ω pull-up resistor.
7. The 1.9 k Ω load represents 1 TTL unit load of 1.6 mA and 5.6 k Ω pull-up resistor.
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0$ V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8$ V).
9. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
10. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

HCPL-2503

HCPL-4502

Fig. 1 Normalized CTR vs. Forward Current

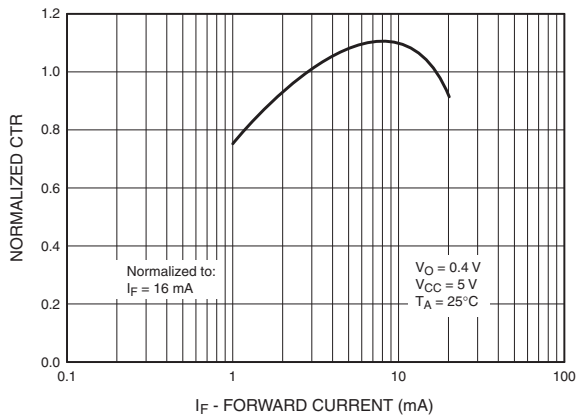


Fig. 2 Normalized CTR vs. Temperature

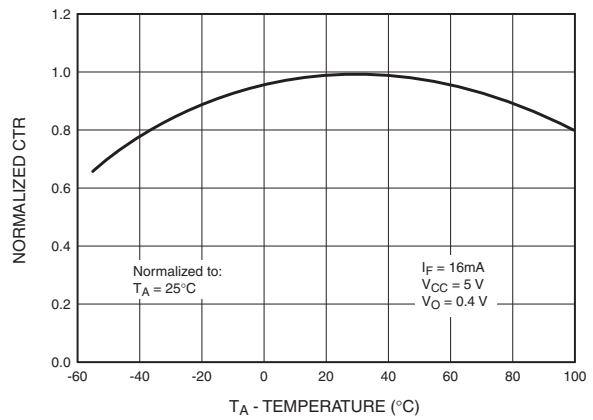


Fig. 3 Output Current vs. Output Voltage

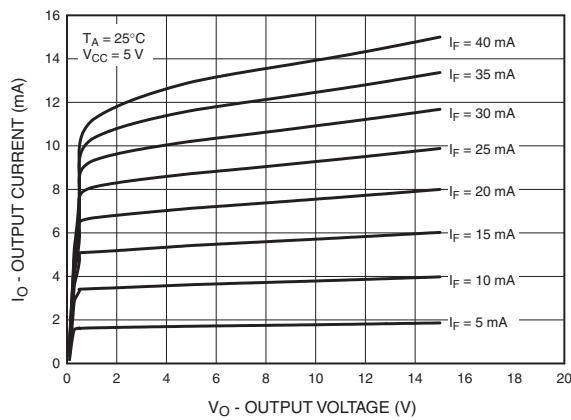


Fig. 4 Logic High Output Current vs. Temperature

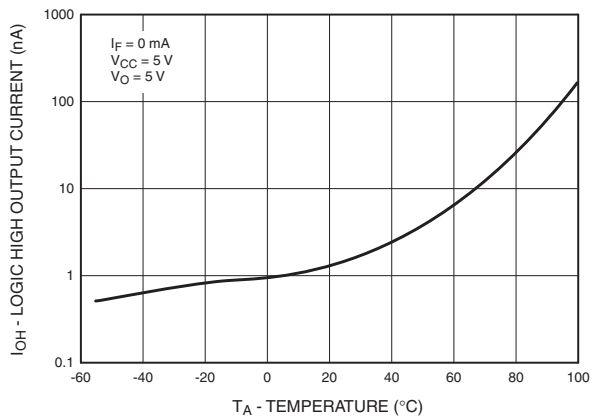


Fig. 5 Propagation Delay vs. Temperature

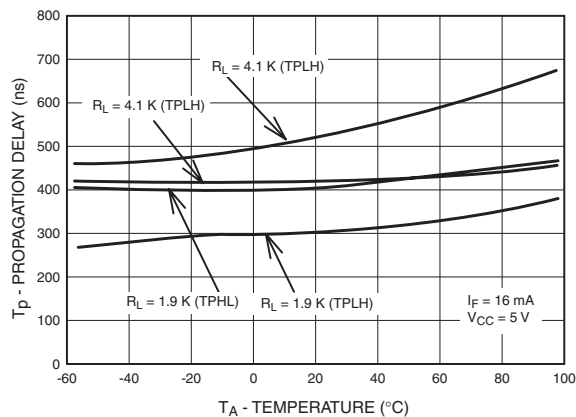
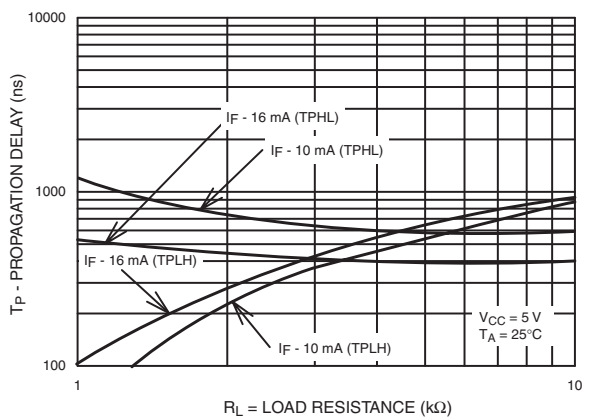


Fig. 6 Propagation Delay vs. Load Resistance

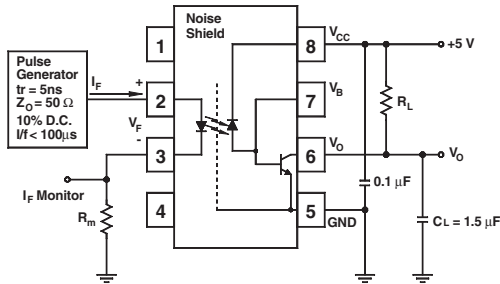


SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

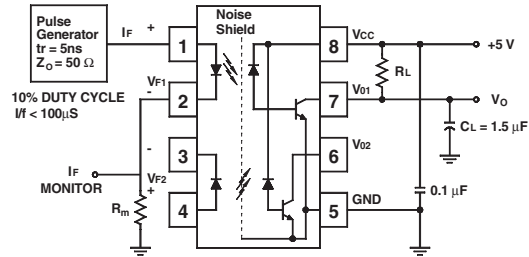
6N136
HCPL-2531

HCPL-2503

HCPL-4502



Test Circuit for 6N135, 6N136, HCPL-2503 and HCPL-4502



Test Circuit for HCPL-2530 and HCPL-2531

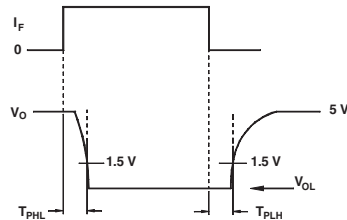
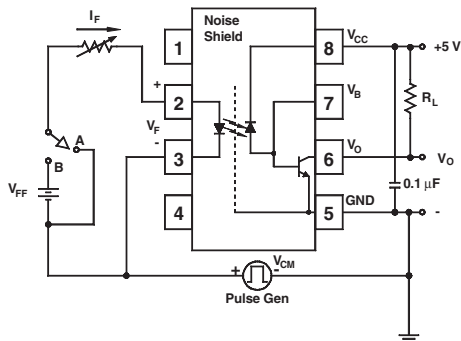
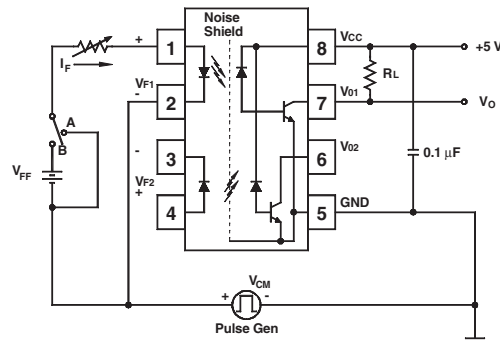


Fig. 7 Switching Time Test Circuit



Test Circuit for 6N135, 6N136, HCPL-2503 and HCPL-4502



Test Circuit for HCPL-2530 and HCPL-2531

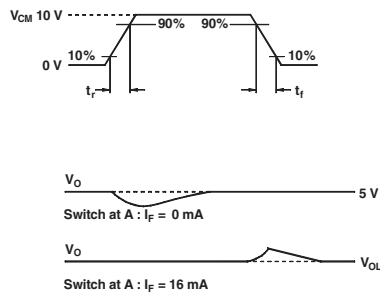


Fig. 8 Common Mode Immunity Test Circuit

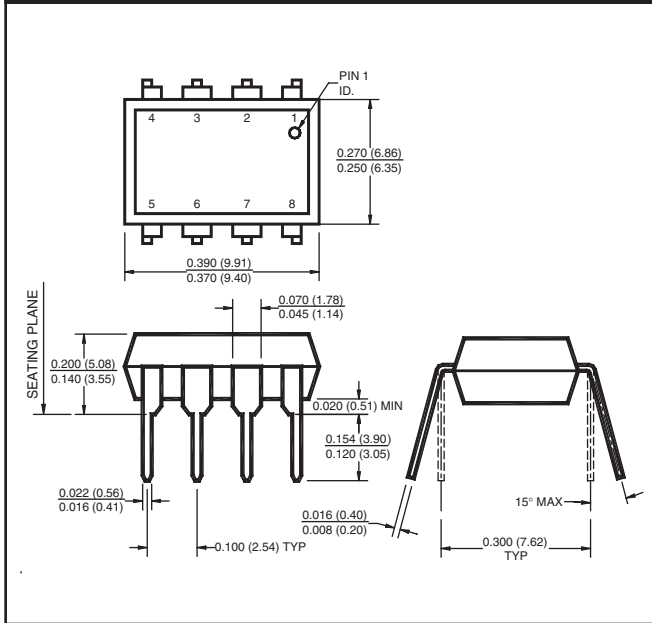
SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

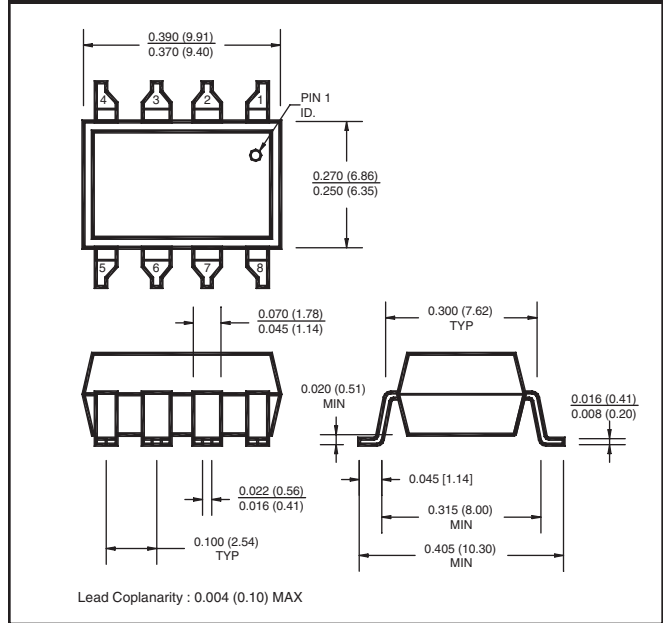
HCPL-2503

HCPL-4502

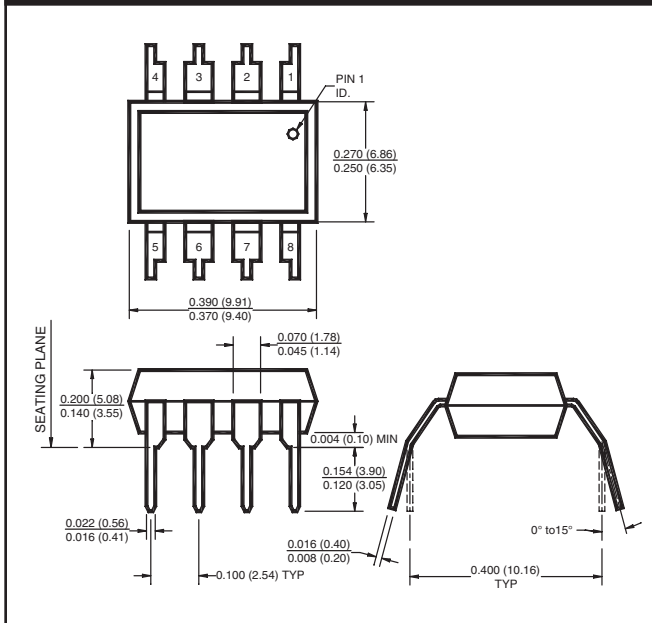
Package Dimensions (Through Hole)



Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



NOTE
All dimensions are in inches (millimeters)

SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

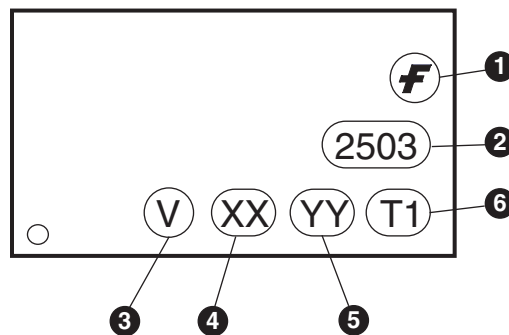
HCPL-2503

HCPL-4502

ORDERING INFORMATION

Option	Example Part Number	Description
S	6N135S	Surface Mount Lead Bend
SD	6N135SD	Surface Mount; Tape and reel
T	6N135T	0.4" Lead Spacing
V	6N135V	VDE0884
TV	6N135TV	VDE0884; 0.4" lead spacing
SV	6N135SV	VDE0884; surface mount
SDV	6N135SDV	VDE0884; surface mount; tape and reel

MARKING INFORMATION



Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '03'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

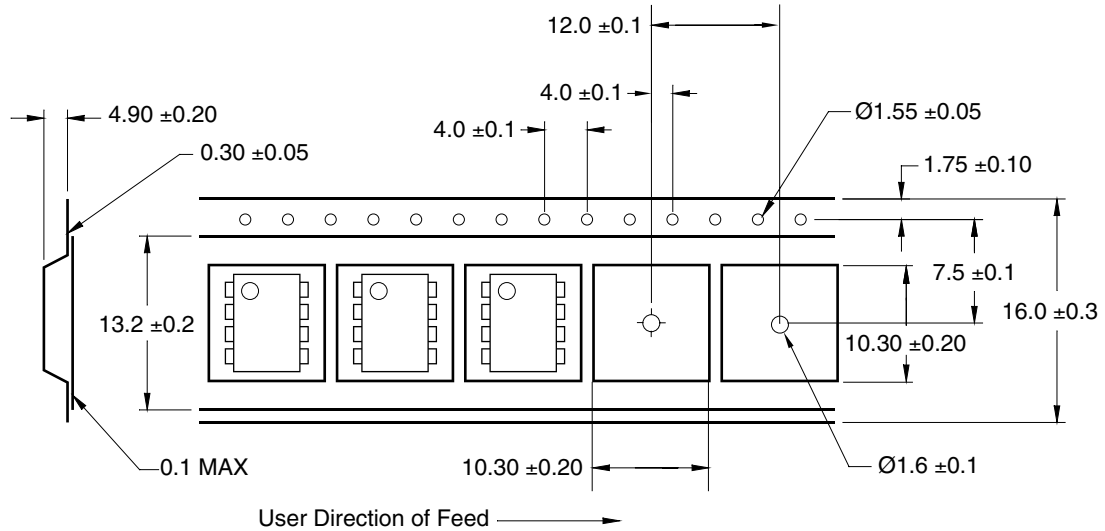
SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

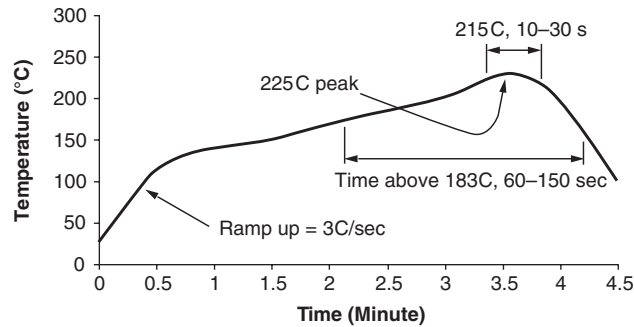
HCPL-2503

HCPL-4502

Carrier Tape Specifications



Reflow Profile



- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60–150 seconds
- One time soldering reflow is recommended

SINGLE-CHANNEL: 6N135
DUAL-CHANNEL: HCPL-2530

6N136
HCPL-2531

HCPL-2503

HCPL-4502

DISCLAIMER

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.