February 1994 Revised March 2001

FAIRCHILD

SEMICONDUCTOR

74LCX646 Low Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX646 consists of registered bus transceiver circuits, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA) (see Functional Description).

The LCX646 is designed for low voltage (2.5V or 3.3V) $\rm V_{CC}$ applications with capability of interfacing to a 5V signal environment.

The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V 3.6V V_{CC} specifications provided
- 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 μ A I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- \pm 24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

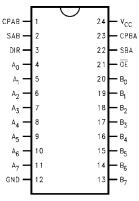
74LCX646 Low Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

Ordering Code:

Order Number	Package Number	Package Description
74LCX646WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LCX646MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX646MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

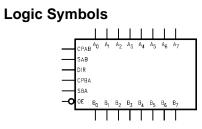
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

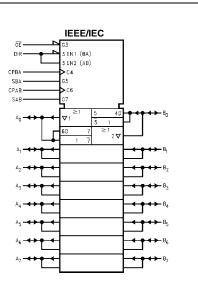
Connection Diagram



Pin Descriptions

Pin Names	Description
A ₀ -A ₇	Data Register A Inputs
	Data Register A Outputs
B ₀ –B ₇	Data Register B Inputs
	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
OE	Output Enable Input
DIR	Direction Control Input





Truth Table

(Note 2)

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	Inputs					Data	a I/O	Function
OE	DIR	CPAB	СРВА	SAB	SBA	A ₀ –A ₇	B ₀ –B ₇	Function
Н	Х	H or L	H or L	Х	Х			Isolation
Н	Х	~	Х	Х	Х	Input	Input	Clock A _n Data into A Register
н	Х	Х	~	Х	Х			Clock B _n Data into B Register
L	Н	Х	Х	L	Х			A _n to B _n —Real Time (Transparent Mode)
L	Н	~	Х	L	Х	Input	Output	Clock A _n Data into A Register
L	н	H or L	Х	Н	Х			A Register to B _n (Stored Mode)
L	Н	~	Х	н	Х			Clock A_n Data into A Register and Output to B_n
L	L	Х	Х	Х	L			B _n to A _n —Real Time (Transparent Mode)
L	L	Х	~	Х	L	Output	Input	Clock B _n Data into B Register
L	L	Х	H or L	Х	н			B Register to A _n (Stored Mode)
L	L	Х	~	Х	н			Clock B_n Data into B Register and Output to A_n

Note 2: The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

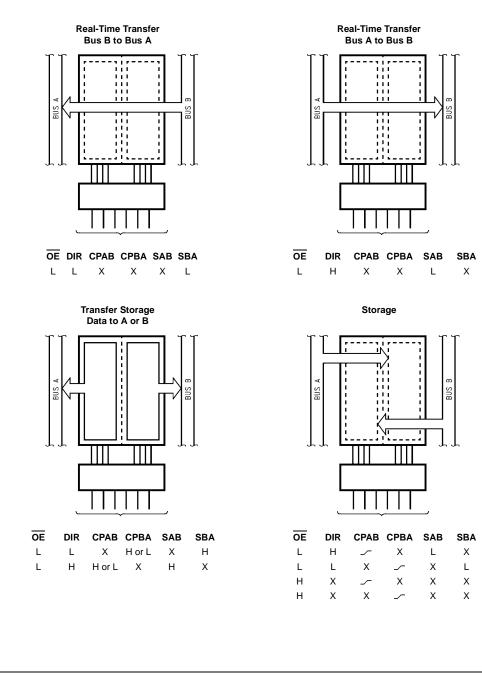
Functional Description

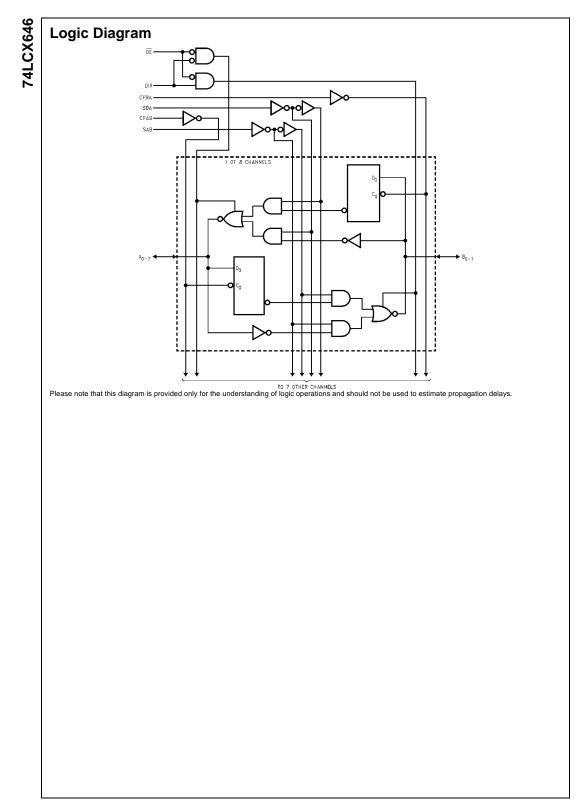
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time. The examples shown below demonstrate the four fundamental bus-management functions that can be performed.

receive data when \overline{OE} is LÓW. In the isolation mode (\overline{OE} HIGH), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time.

The direction control (DIR) determines which bus will







Symbol	Parameter	Value	Conditions	Units	
V _{CC}	Supply Voltage	-0.5 to +7.0		V	
VI	DC Input Voltage	-0.5 to +7.0		V	
Vo	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	4) V	
		-0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 4)		
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA	
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA	
		+50	$V_{O} > V_{CC}$	ША	
lo	DC Output Source/Sink Current	±50		mA	
I _{CC}	DC Supply Current per Supply Pin	±100		mA	
I _{GND}	DC Ground Current per Ground Pin	±100		mA	
T _{STG}	Storage Temperature	-65 to +150		°C	

Recommended Operating Conditions (Note 5)

Symbol	Parameter		Min	Max	Units
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	v
VI	Input Voltage		0	5.5	V
Vo	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		3-STATE	0	5.5	v
I _{OH} /I _{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$		±24	
		$V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$		±12	mA
		$V_{CC}=2.3V-2.7V$		±8	
T _A	Free-Air Operating Temperature		-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Unused inputs or I/Os must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{cc}	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units
-		Conditions	(V)	Min	Max	Onits
/ _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 - 3.6	2.0		v
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	v
			2.7 - 3.6		0.8	· · ·
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} - 0.2		
		I _{OH} = -8 mA	2.3	1.8		•
		I _{OH} = -12 mA	2.7	2.2		V
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2	
		I _{OL} = 8 mA	2.3		0.6	•
		I _{OL} = 12 mA	2.7		0.4	V
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.3 - 3.6		±5.0	μΑ
I _{OZ}	3-STATE I/O Leakage	$0 \le V_O \le 5.5V$	2.3 – 3.6		±5.0	μA
		$V_I = V_{IH} \text{ or } V_{IL}$	2.5 - 5.0		±0.0	μΛ
IOFF	Power-Off Leakage Current	$V_1 \text{ or } V_0 = 5.5 \text{ V}$	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC}	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units
Cymbol	i arameter	Conditions	(V)	Min	Max	onits
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 3.6		10	μA
		$3.6V \le V_I, V_O \le 5.5V$ (Note 6)	2.3 - 3.6		±10	μΛ
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 - 3.6		500	μΑ

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

			TA	=-40°C to +	85°C, R _L = 5	00 Ω		
Symbol	Parameter	$V_{CC}=3.3V\pm0.3V$		V _{CC} = 2.7V		$V_{CC}=2.5V\pm0.2V$		Units
	Falanietei	C _L =	50 pF	C _L = 50 pF		C _L = 30 pF		Units
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	150						MHz
t _{PHL}	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t _{PLH}	Bus to Bus	1.5	7.0	1.5	8.0	1.5	8.4	115
t _{PHL}	Propagation Delay	1.5	8.5	1.5	9.5	1.5	10.5	
t _{PLH}	Clock to Bus	1.5	8.5	1.5	9.5	1.5	10.5	ns
t _{PHL}	Propagation Delay	1.5	8.5	1.5	9.5	1.5	10.5	
t _{PLH}	Select to Bus	1.5	8.5	1.5	9.5	1.5	10.5	ns
t _{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t _{PZH}		1.5	8.5	1.5	9.5	1.5	10.5	115
t _{PLZ}	Output Disable Time	1.5	8.5	1.5	9.5	1.5	10.5	
t _{PHZ}		1.5	8.5	1.5	9.5	1.5	10.5	ns
ts	Setup Time	2.5		2.5		4.0		ns
t _H	Hold Time	1.5		1.5		2.0		ns
t _W	Pulse Width	3.3		3.3		4.0		ns
toshl	Output to Output Skew		1.0					
t _{OSLH}	(Note 7)		1.0					ns

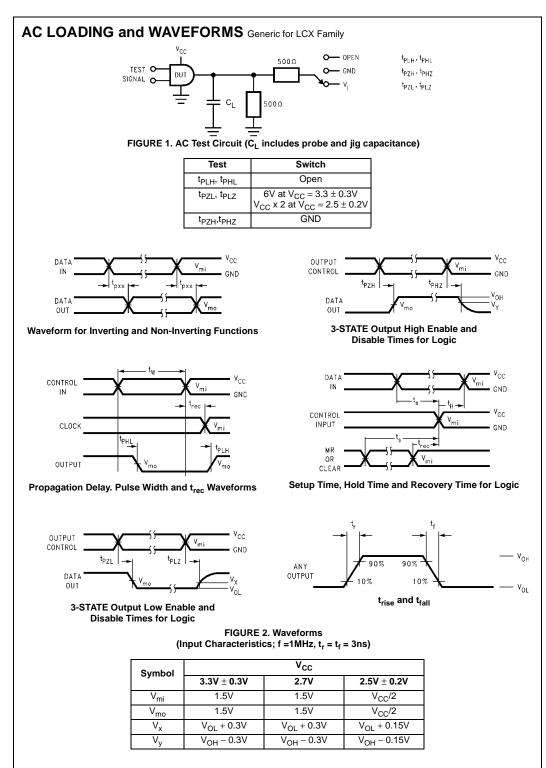
specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

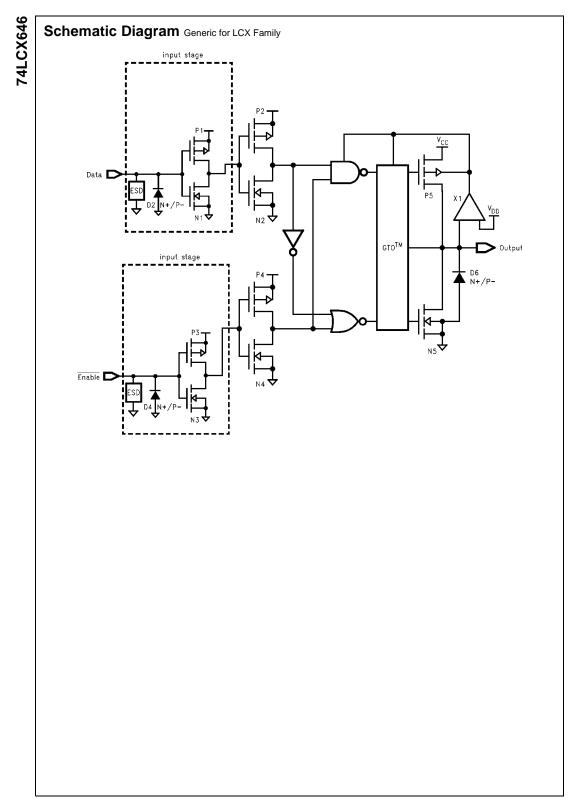
Dynamic Switching Characteristics

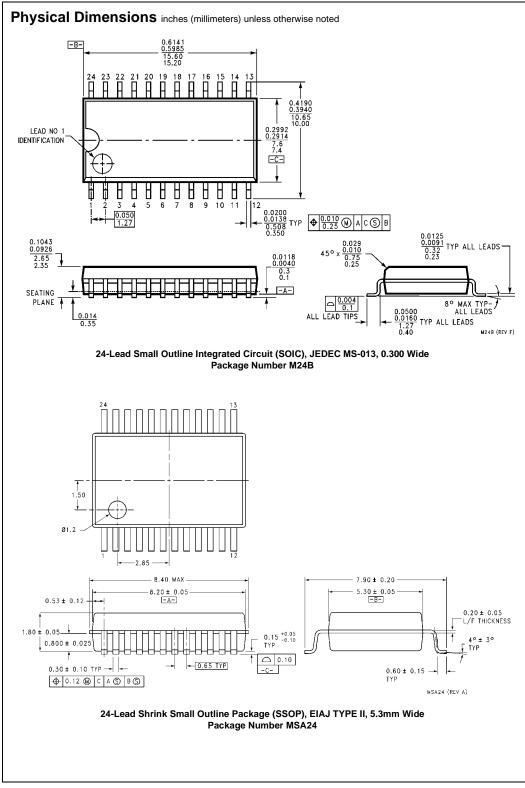
Symbol	Parameter	Conditions	v _{cc}	$T_A = 25^{\circ}C$	Units
		Conditions	(V)	Typical	0
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	$C_L = 50 \text{ pF}, \text{ V}_{IH} = 3.3 \text{ V}, \text{ V}_{IL} = 0 \text{ V}$	3.3	0.8	V
		$C_L=30 \text{ pF}, V_{IH}=2.5 \text{V}, V_{IL}=0 \text{V}$	2.5	0.6	v
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	-0.8	V
		$C_L=30 \text{ pF}, V_{IH}=2.5 \text{ V}, V_{IL}=0 \text{ V}$	2.5	-0.6	v

Capacitance

Symbol	Parameter	Conditions	Typical	Units
CIN	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7	pF
C _{I/O}	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC} , f = 10 MHz	25	pF







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