

# FDZ4010

## Integrated Load Switch

### Features

- Input Voltage Range from 2 V to 5 V
- 10 mA output current
- Ultra Thin and Small Package WL-CSP  
0.8 X 1.2 mm<sup>2</sup>, Height 0.5 mm
- RoHS Compliant



### General Description

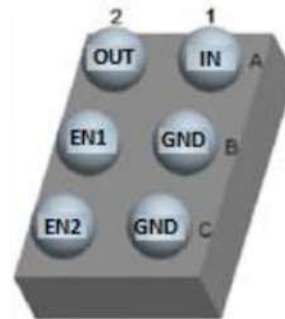
The FDZ4010 is a 10 mA high side Pch MOSFET switch that can be controlled by two enable signals. It is an AND function switch activated by asserting both enable signals high. Input voltage range operates from 2 V to 5 V to align with the requirement of portable devices power requirement. FDZ4010 is uniquely designed for optimized low power dissipation and precise driver requirement. FDZ4010 comes in a tiny 0.8 mm X 1.2 mm WLCSP, 6 bumps, with 0.4 mm pitch.

### Application

- Smart Phone / Table Accessory



TOP View



BOTTOM View

6 Balls, 0.8 X 1.2 mm<sup>2</sup> WL-CSP

### Package Marking and Ordering Information

Part Number	Device Marking	Ball Pitch	Package	Reel Size	Tape Width	Quantity
FDZ4010	Z5	0.4 mm	0.8 mm x 1.2 mm WL-CSP, 6 Bumps	7 "	8 mm	3000

For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html)

**Application Diagram**

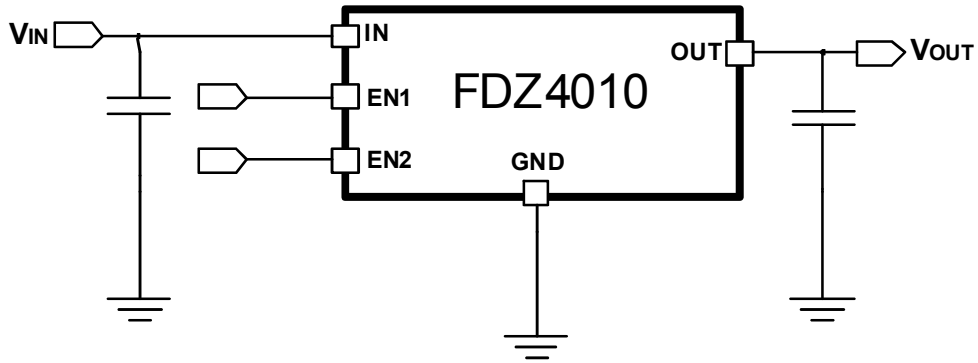


Figure 1. Typical Application

**Block Diagram**

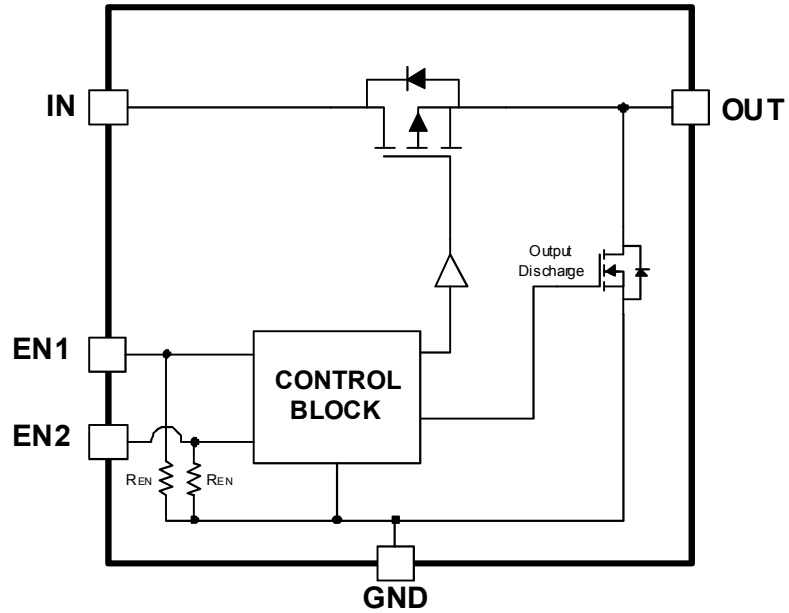


Figure 2. Functional Block Diagram

**Truth Table**

$V_{IN}$ (2 V to 5 V)	EN1	EN2	PCH MOSFET Status	$V_{OUT}$ Status
YES	HIGH	HIGH	ON	$V_{IN}$
YES	LOW	LOW	OFF	LOW
YES	HIGH	LOW	OFF	LOW
YES	LOW	HIGH	OFF	LOW

Table 1. Truth Table for OUT Status

## Pin Configuration



Figure 3. Pin Assignments

## Pin Definitions

Pin #	Name	Description
A1	IN	Input of the Pch MOSFET Switch
A2	OUT	Output of the Pch MOSFET Switch. Internally, this pin is pulled down through an output discharge FET to Ground when EN pins are low and $V_{IN}$ is present.
B1, C1	GND	Ground
B2	EN1	ON/OFF control input, Active High.
C2	EN2	ON/OFF control input, Active High.

### Absolute Maximum Ratings

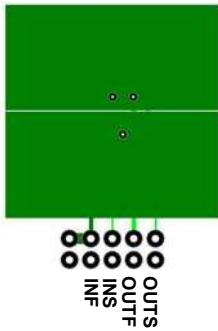
Characteristics		Min.	Max.	Unit
$V_{IN}, V_{OUT}$ to GND		-0.3	6	V
$V_{EN1}, V_{EN2}$ to GND		-0.3	6	V
Continuous Output Current			20	mA
Junction Temperature ( $T_J$ )			150	$^{\circ}\text{C}$
Storage Temperature Range ( $T_{STG}$ )		-65	150	$^{\circ}\text{C}$
Thermal Resistance, Junction to Ambient ( $\theta_{JA}$ )		(Note 1b)		$^{\circ}\text{C}/\text{W}$
Electrostatic Discharge	Human Body Model, ANSI/ESDA/ JEDEC JS-001-2012	5		kV
	Charged Device Model, JESD22-C101	2		

### Recommended Operating Conditions

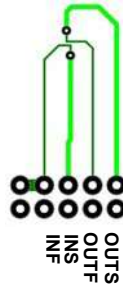
Characteristics	Symbol	Min.	Max.	Unit
IN Voltage	$V_{IN}$	2	5	V
OUT Current, $V_{IN} = 3.3\text{ V}$ , $V_{EN1} = V_{EN2} = 3.3\text{ V}$	$I_{OUT}$		10	mA
EN1, EN2 Voltage	$V_{EN1}, V_{EN2}$		5	V
Operating Temperature Range		-40	85	$^{\circ}\text{C}$

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 115  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



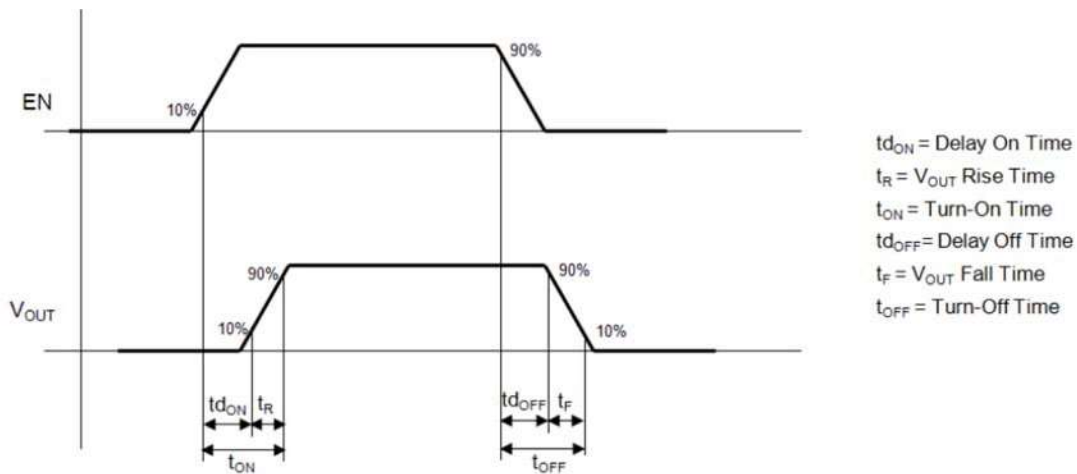
b. 312  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

**Electrical Characteristics**  $V_{IN} = 2\text{ V to }5\text{ V}$ ,  $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{IH}$	Input High Voltage, EN1, EN2	$V_{IN} = 2.5\text{ V to }5\text{ V}$ and across temperature range	1.375			V
$V_{IH}$	Input High Voltage, EN1, EN2	$V_{IN} = 2\text{ V}$ and across temperature range	1.525			V
$V_{IL}$	Input Low Voltage, EN1, EN2	$V_{IN} = 2\text{ V to }5\text{ V}$ and across temperature range			0.95	V
$R_{EN}$	Pull Down Resistance at EN1, EN2	$V_{EN1} = V_{EN2} = 1\text{ V}$ and across temperature range	70	100	130	$k\Omega$
$C_{EN}$	Input Capacitance of EN1, EN2	$f = 1\text{ MHz}$ and across temperature range (Note 2)			10	pF
$R_{DS(ON)}$	On-Resistance of Pch MOSFET	$I_{OUT} = 10\text{ mA}$ , $V_{IN} = 2\text{ V to }5\text{ V}$			1.5	$\Omega$
$I_Q$	Quiescent Current	$V_{IN} = 5\text{ V}$ , $V_{EN1} = V_{EN2} = 5\text{ V}$ , $V_{OUT}$ floating ( $I_{OUT} = 0$ ), Across temperature range			500	$\mu\text{A}$
$I_{SD}$	Shutdown Current	$V_{IN} = 3.3\text{ V}$ , $V_{EN1} = V_{EN2} = 0\text{ V}$ , $V_{OUT}$ floating ( $I_{OUT} = 0$ ), Across temperature range			1	$\mu\text{A}$
		$V_{IN} = 3.3\text{ V}$ , $V_{EN1} = 825\text{ mV}$ & $V_{EN2} = 425\text{ mV}$ , $V_{EN1} = 425\text{ mV}$ & $V_{EN2} = 825\text{ mV}$ , $V_{OUT}$ floating ( $I_{OUT} = 0$ ), Across temperature range			10	$\mu\text{A}$
$R_{OUT}$	Pull Down Resistance at OUT Pin	$V_{EN1} = V_{EN2} = 0\text{ V}$		1	1.3	$k\Omega$
$t_{on}$	Turn-On Time	Load Impedance,			1	$\mu\text{s}$
$t_r$	Turn-On Rise Time	$V_{IN} = 3.3\text{ V}$ ,			0.95	$\mu\text{s}$
$t_{off}$	Turn-Off Time	$C_L = 50\text{ pF}$ , $R_L = 500\text{ }\Omega$ ,			2	$\mu\text{s}$
$t_f$	Turn-Off Fall Time	$V_{EN1} = V_{EN2} = 0\text{ V to }2.3\text{ V}$ , (500 ns rise time)			2	$\mu\text{s}$

**Notes:**

2. Guaranteed by characterization and design



**Figure 4. Timing Diagram**

Typical Characteristics (Continued)

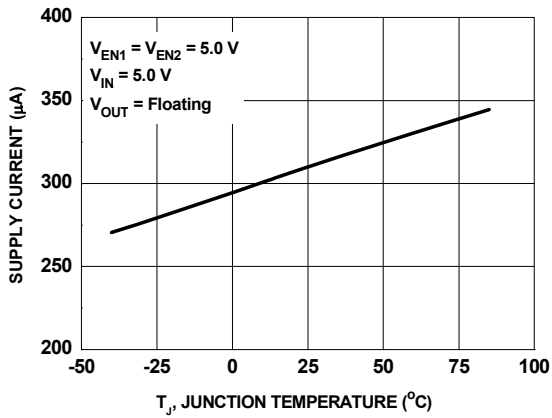


Figure 5. Quiescent Current vs Temperature

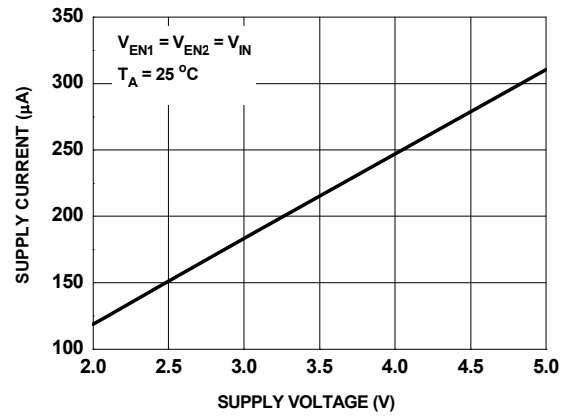


Figure 6. Quiescent Current vs Supply Voltage

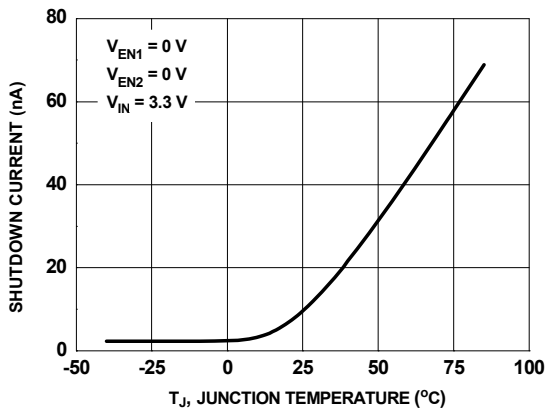


Figure 7. Shutdown Current vs Temperature

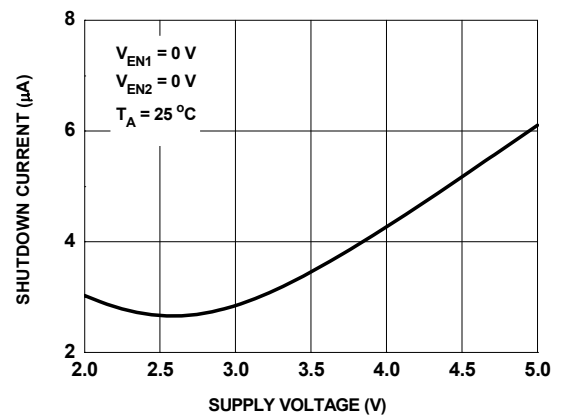


Figure 8. Shutdown Current vs Supply Voltage

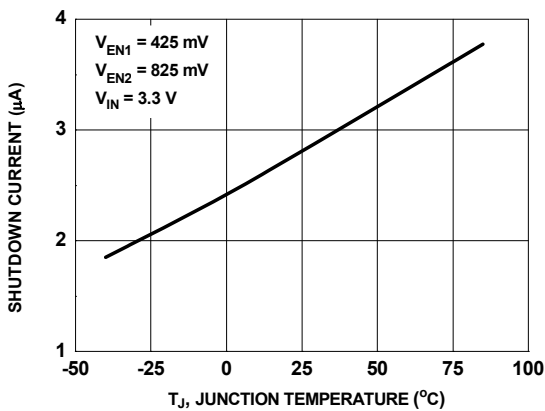


Figure 9. Shutdown Current vs Temperature

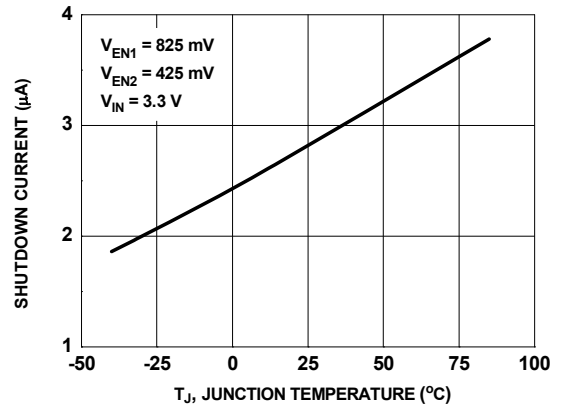


Figure 10. Shutdown Current vs Temperature

Typical Characteristics (Continued)

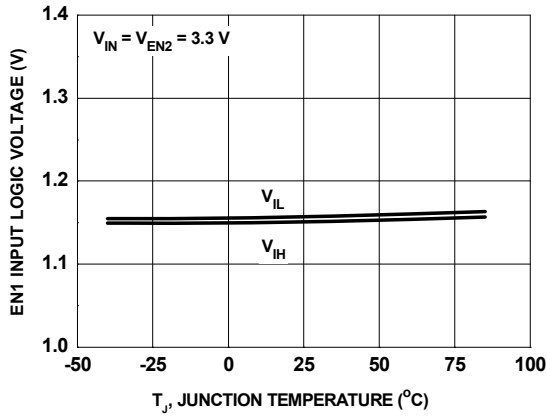


Figure 11. EN1 Logic Voltage vs Temperature

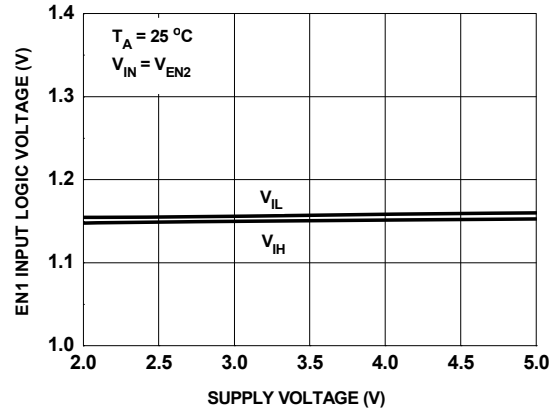


Figure 12. EN1 Logic Voltage vs Supply Voltage ( $V_{IN}$ )

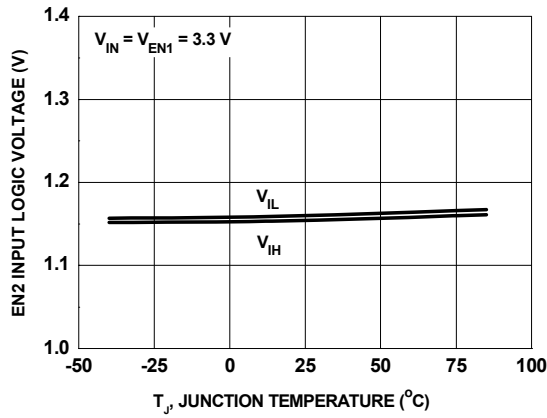


Figure 13. EN2 Logic Voltage vs Temperature

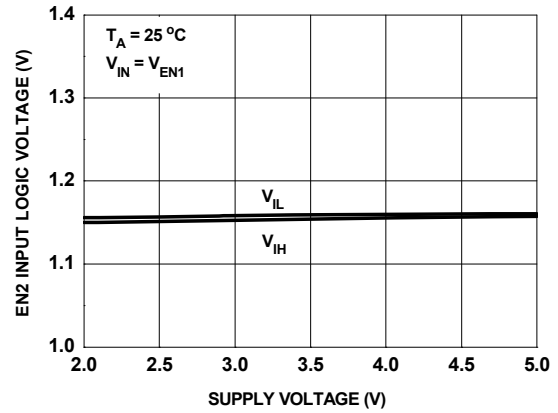


Figure 14. EN2 Logic Voltage vs Supply Voltage ( $V_{IN}$ )

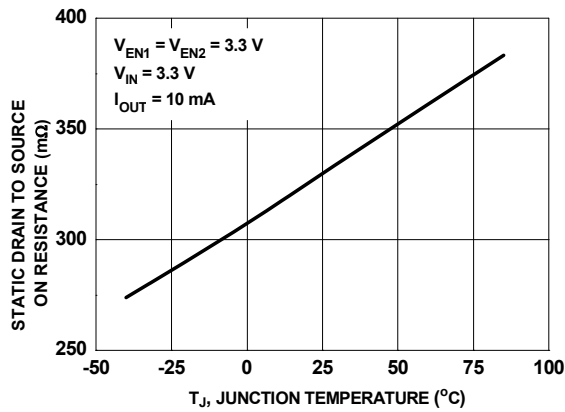


Figure 15. Static Drain to Source ON Resistance vs Temperature

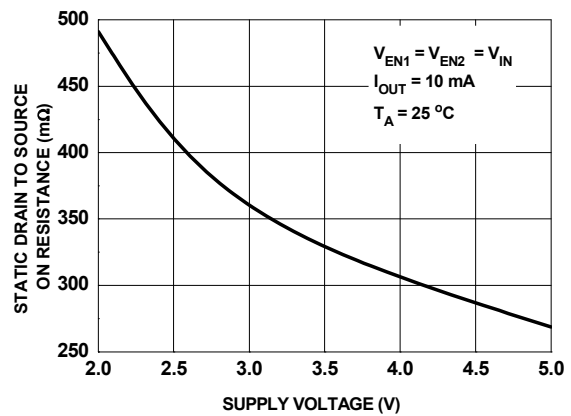


Figure 16. Static Drain to Source ON Resistance vs Supply Voltage

Typical Characteristics (Continued)

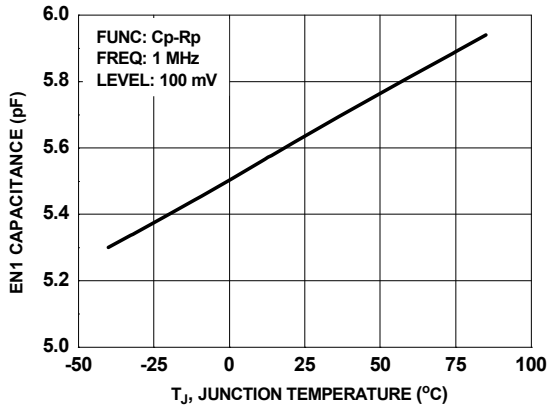


Figure 17. EN1 Capacitance vs Temperature

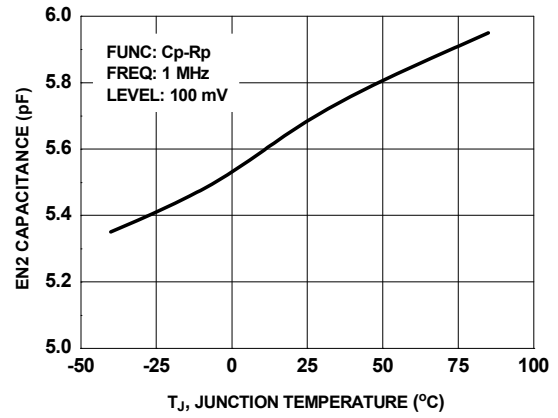


Figure 18. EN2 Capacitance vs Temperature



Typical Characteristics (Continued)

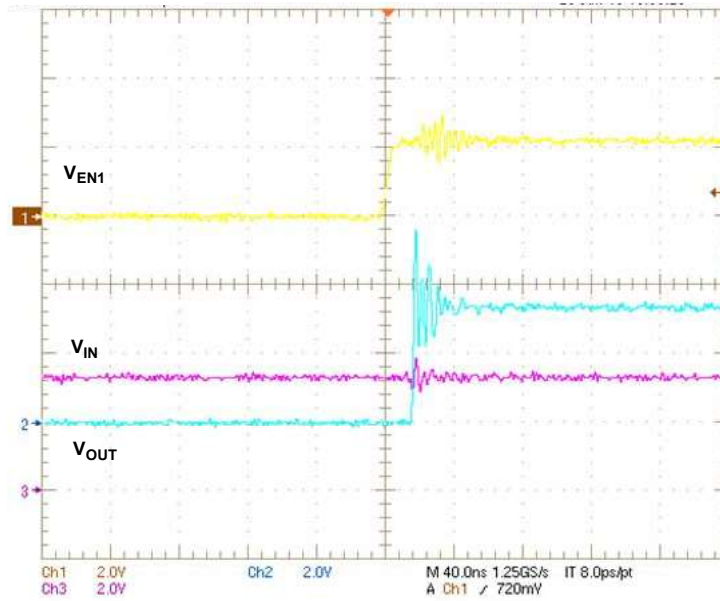


Figure 19. Turn-On Time ( $V_{IN} = 3.3\text{ V}$ ,  $V_{EN2} = 2.3\text{ V}$ ,  $V_{EN1} = 0$  to  $2.3\text{ V}$ ,  $C_{OUT} = 50\text{ pF}$ ,  $R_L = 500\ \Omega$ , timescale =  $40\ \mu\text{s}/\text{div}$ )

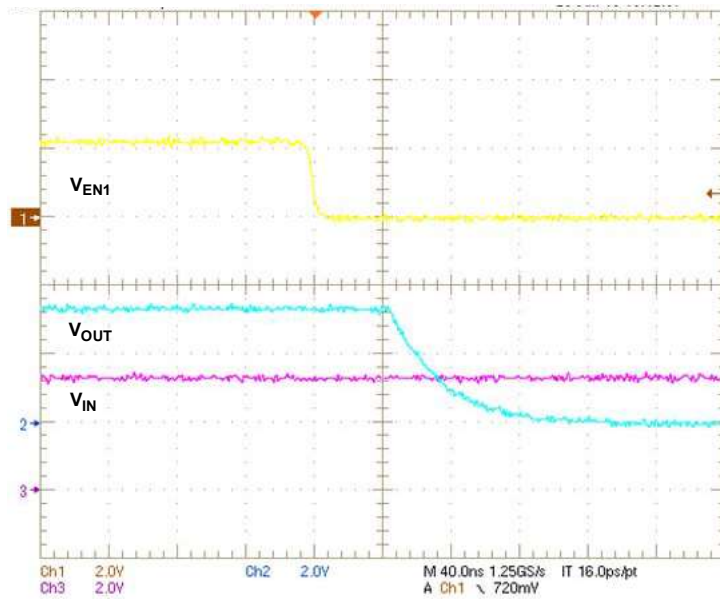


Figure 20. Turn-Off Time ( $V_{IN} = 3.3\text{ V}$ ,  $V_{EN2} = 2.3\text{ V}$ ,  $V_{EN1} = 2.3$  to  $0\text{ V}$ ,  $C_{OUT} = 50\text{ pF}$ ,  $R_L = 500\ \Omega$ , timescale =  $40\ \mu\text{s}/\text{div}$ )

Typical Characteristics (Continued)

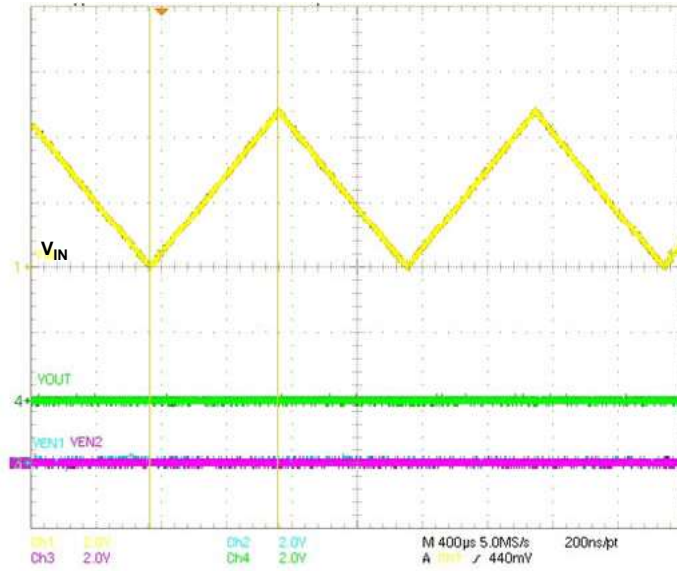


Figure 21.  $V_{IN}$  Ramp Up and Down ( $V_{IN} = 0$  to 4.8 V (6100 V/sec),  $EN1$  and  $EN2$  are floating (Internally GND),  $C_{OUT} = 50$  pF,  $R_L = 500 \Omega$ , timescale = 400  $\mu$ s/div)

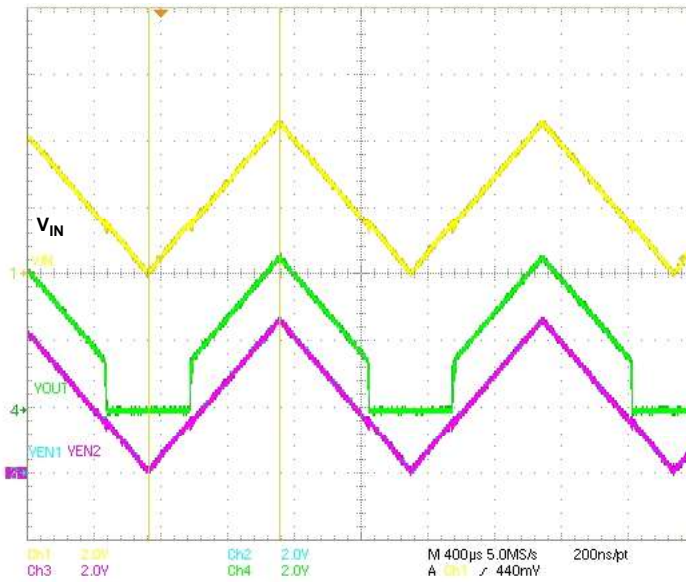


Figure 22.  $V_{IN}$  Ramp Up and Down ( $EN1 = EN2 = V_{IN} = 0$  to 4.8 V (6100 V/sec),  $C_{OUT} = 50$  pF,  $R_L = 500 \Omega$ , timescale = 400  $\mu$ s/div)

## Application Information

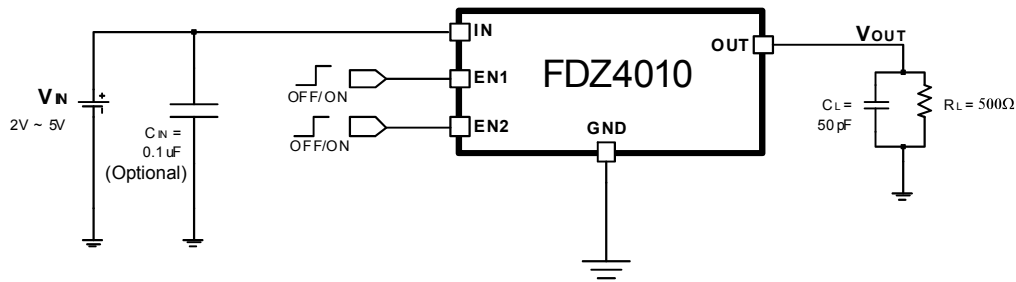


Figure 23. Typical Application Circuit

### Input Voltage

Input Voltage ( $V_{IN}$ ) is set from 2 V to 5 V.

### Input Capacitor

To prevent the input voltage being pulled below the minimum operating voltage, a reservoir capacitor can be connected from IN to GND. 0.1  $\mu$ F ceramic type is suitable.

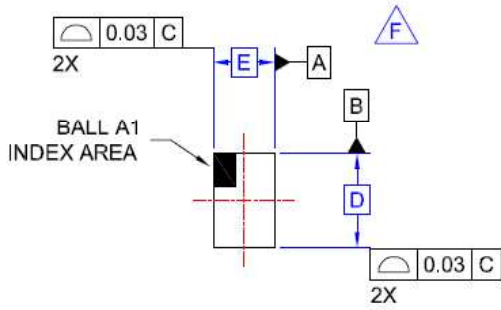
### Enable/Shutdown Operation

To turn on the switch, both the EN pins need to be asserted high. To ensure proper operation, Enable signals must be able to swing above and below the specified turn-on/off voltage threshold described in the Electrical Characteristics table under  $V_{IL}$  and  $V_{IH}$  for the selected input voltage.

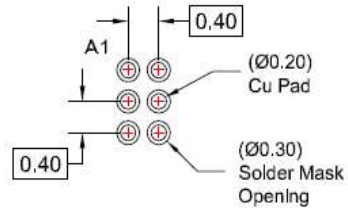
### Power up Sequence

Turn on input voltage ( $V_{IN}$ ) within range from 2 V to 5 V then turn on EN1 or/and EN2 signal.  $V_{OUT}$  status changed by EN1 or/and EN2 signal input and defined the status in Table 1 Truth Table.

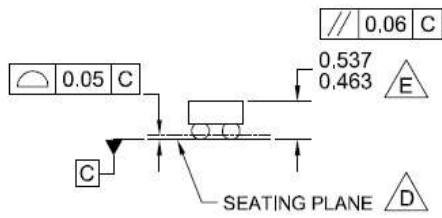
### Dimensional Outline and Pad Layout



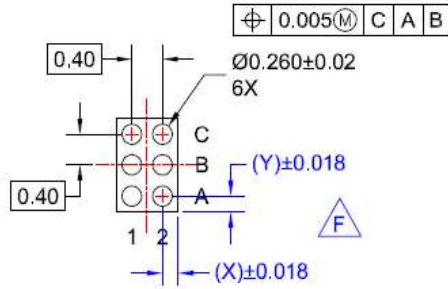
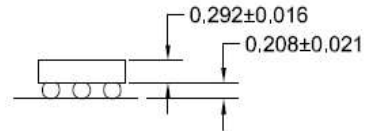
TOP VIEW



RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

**NOTES:**

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 1994.
- D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE TYPICAL HEIGHT IS 463 MICRONS ±37 MICRONS (463-537 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.






### Product-Specific Dimensions

Product	D	E	X	Y
FDZ4010	1.16 mm	0.76 mm	0.18 mm	0.18 mm



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| AX-CAP®*  | FRFET®  | PowerXS™  | TinyBoost™  |
| BitSiC™   | Global Power Resource™                          | Programmable Active Droop™  | TinyBuck™   |
| Build it Now™   | Green Bridge™                                   | QFET®   | TinyCalc™   |
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| FAST®   | OptoHiT™  | SupreMOS®   | VoltagePlus™  |
| FastvCore™  | OPTOLOGIC®                                      | SyncFET™  | XS™   |
| FETBench™   | OPTOPLANAR®                                     |   |   |

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**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.