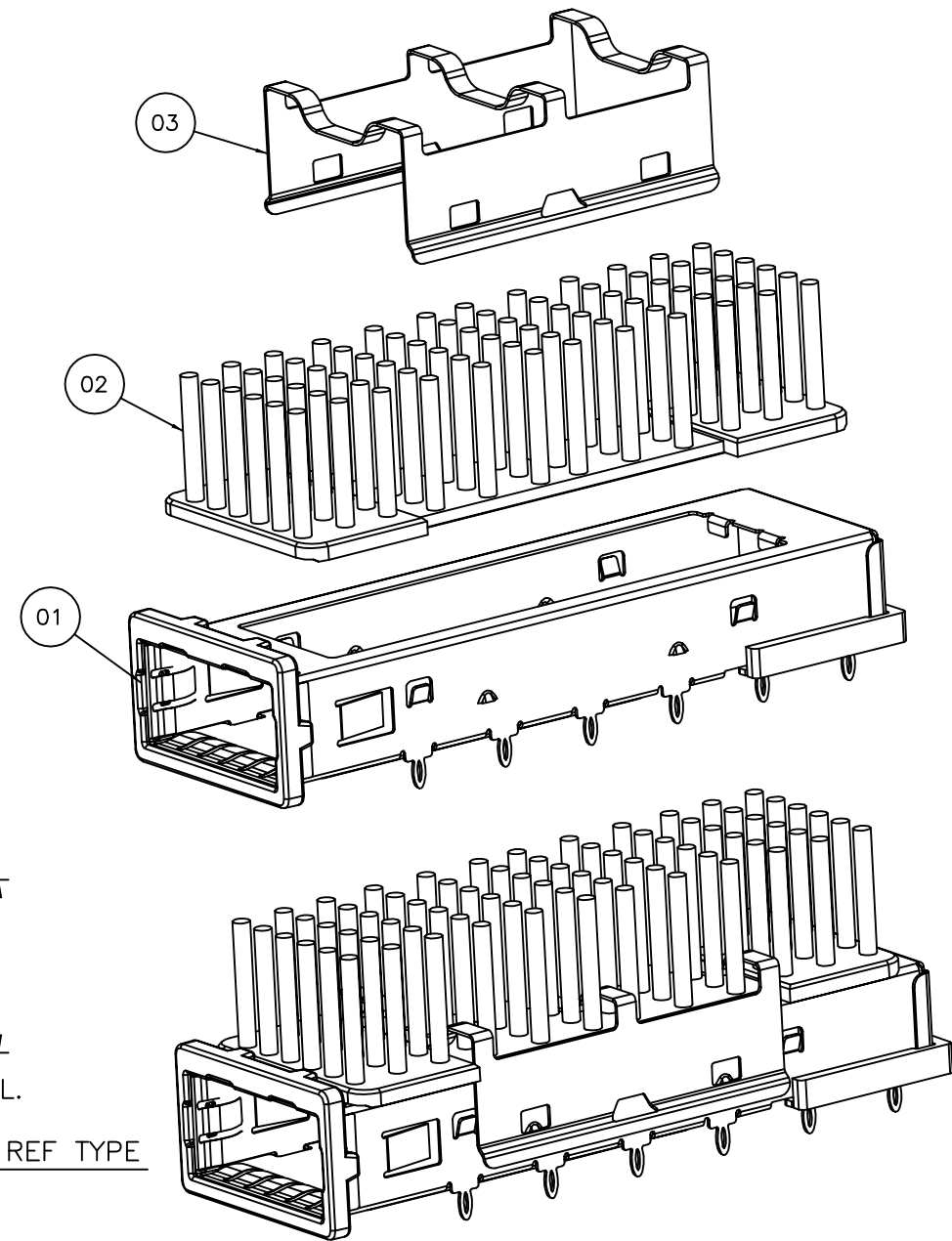
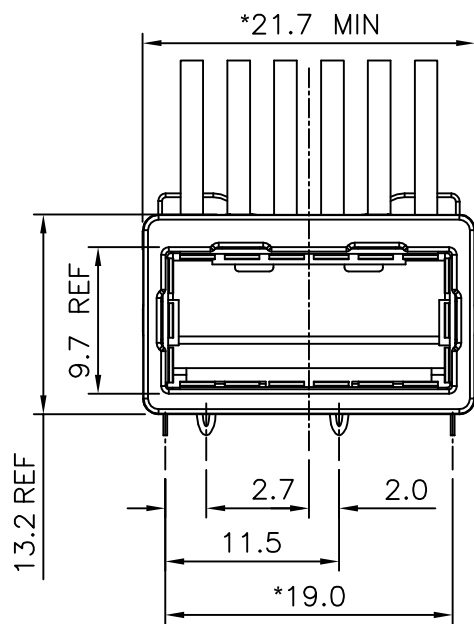
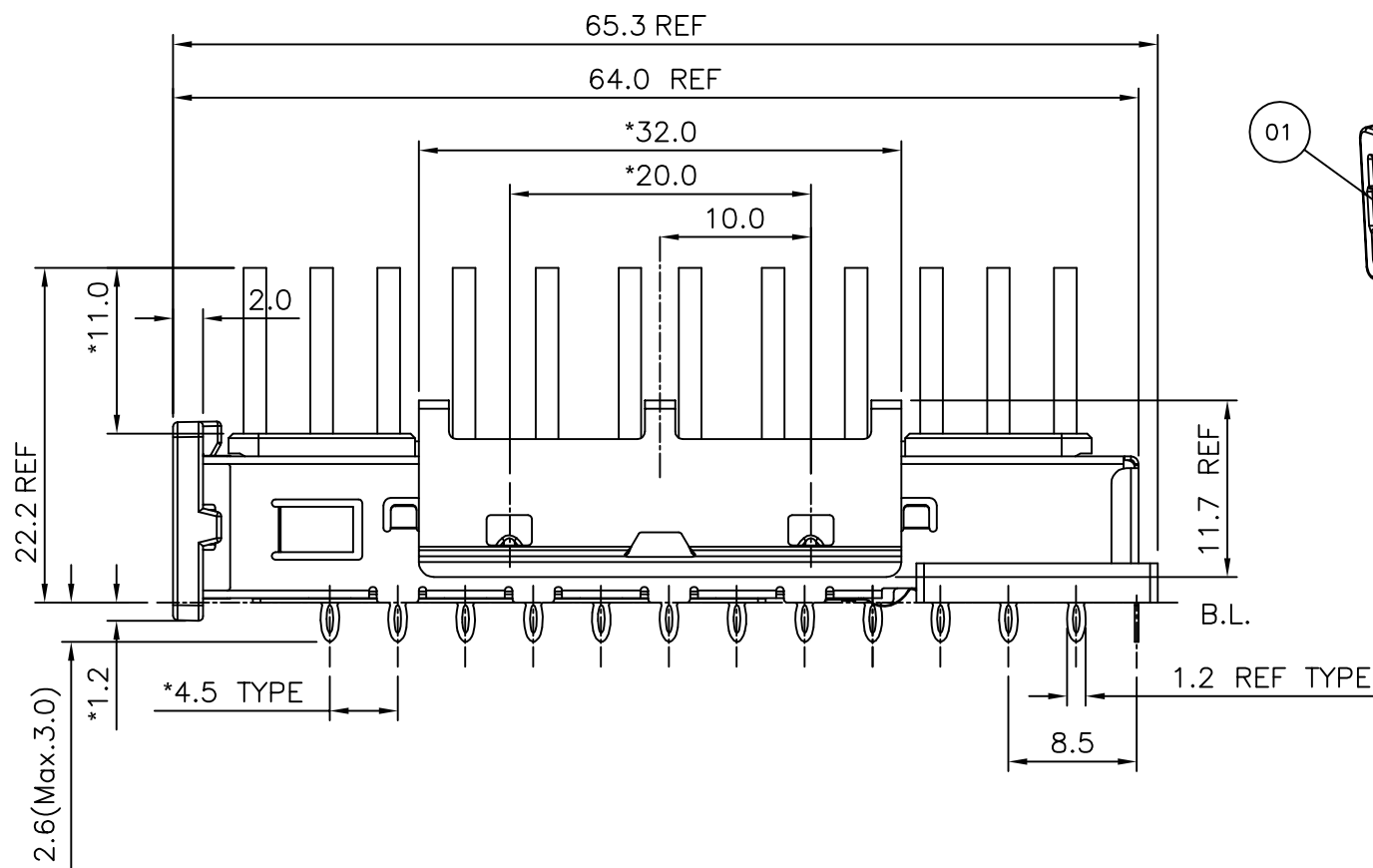
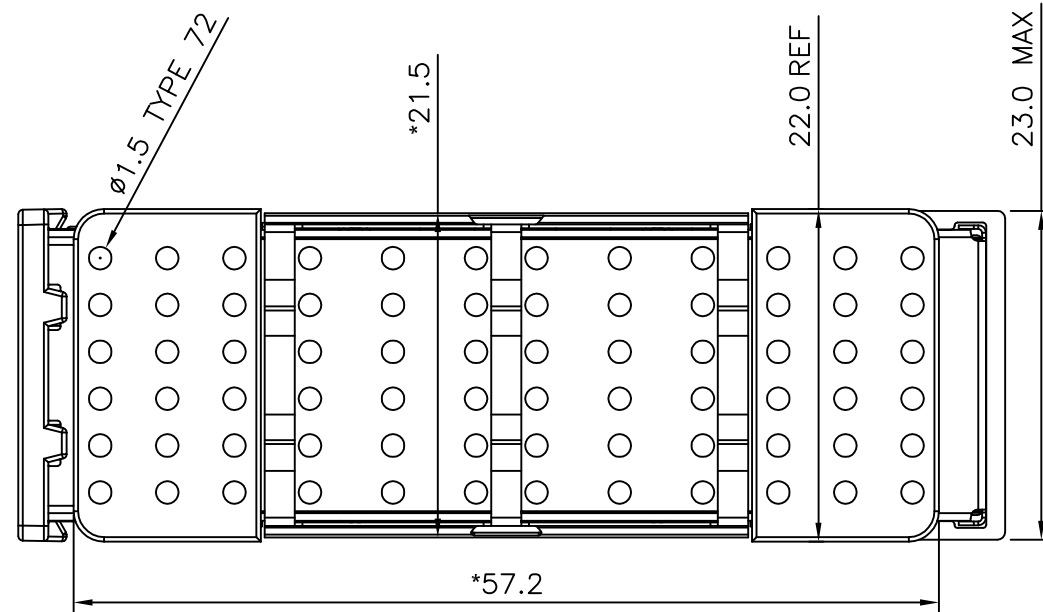


A1RFRD10

REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	CHKD



PART NUMBER: XFP003-L

No.	DESCRIPTION	Q'ty	MATERIAL	PLATING	REMARK
01	XFP CAGE ASSEMBLY (Non-Logo)	1			
02	XFP HEAT SINK (11.00mm)	1	AL	Ni	
03	XFP HEAT SINK CLIP	1	SUS		

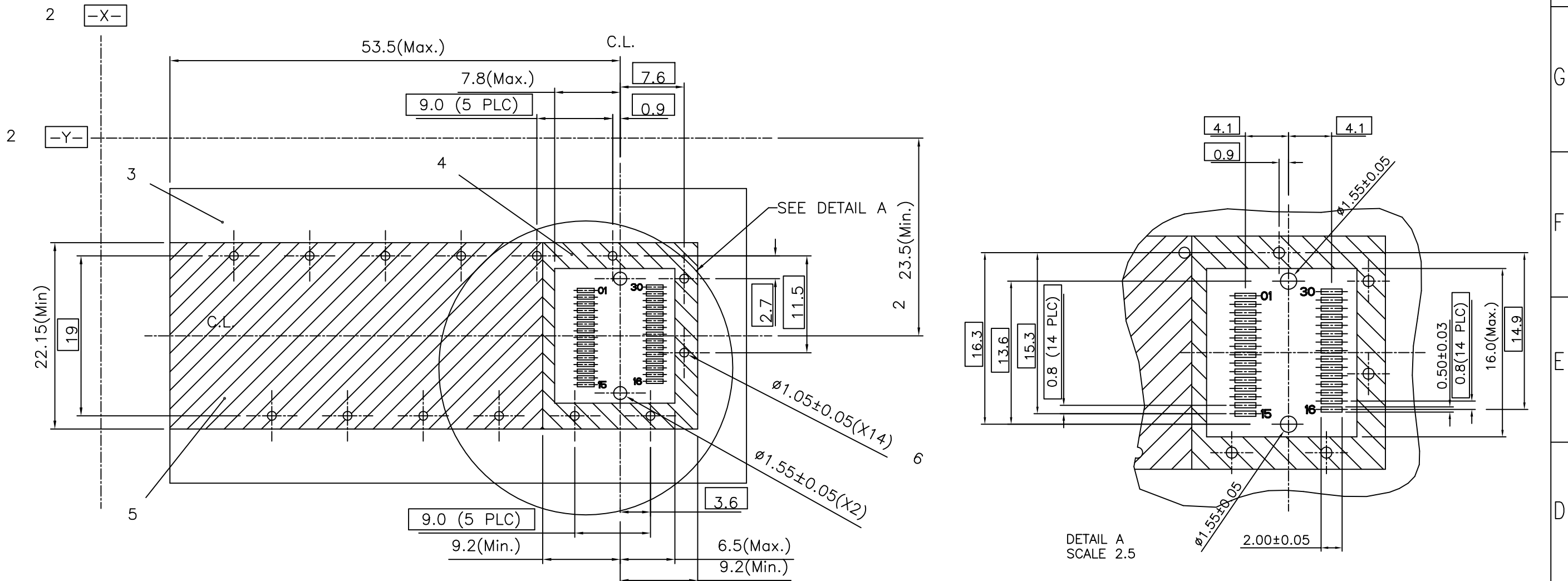
DETACHED LISTS	MM (INCH)	DFTO tzou	DATE 06/02/06'
	TOLERANCES EXCEPT AS NOTED	CHKD	DATE
		MFO	DATE
		APPVL	DATE
	MM	±	
	.0 ± 0.2	±	
	.00 ± 0.15	±	
	.000 ± 0.075	±	
	ANGLES ± 0.5	QT'Y :	
	THIRD ANGLE PROJECTION	FINISH :	
		SCALE :	1 : 2

FULL RISE ELECTRONIC CO., LTD

TITLE (Non-Logo)
XFP CAGE WITH PCI HEAT SINK KIT

DRAWING NO. XFP003-L	SIZE A3	REV 0
/PART NO. SEE NOTE		
DO NOT SCALE DRAWING	SHEET 1	OF 2

REVISION RECORD				
REV	ECO	DESCRIPTION	DRFT	CHKD



RECOMMEND P.C.B. LAYOUT

Note:

- | | |
|--|---|
| <p>1 DESIGN MEETS REQUIREMENTS OF XFPMSA SPECIFICATION REV. 3.1 (10 GIGABIT SMALL FROM FACTOR PLUGGABLE MODULE).</p> <p>2 DATUM $\boxed{-X-}$ AND $\boxed{-Y-}$ ESTABLISHED BY CUSTOMER.</p> <p>3 DATUM $\boxed{-A-}$ IS TOP SURFACE OF HOST BOARD.</p> <p>4 INDICATED SURFACES TO BE CONDUCTIVE AND CONNECTED TO CHASSIS GROUND.</p> | <p>5 CROSS-HATCHED AREA DENOTES COMPONENT AND TRACE KEEP-OUT (EXCEPT CHASSIS GROUND)</p> <p>6 RECOMMENDATION FOR P.C.BOARD HOLES:
 A. HOLE ϕ AFTER DRILLING : 1.15 ± 0.02 mm.
 B. HOLE ϕ Sn PLATE : 1.05 ± 0.05 mm.
 C. 25um ~ 50um COPPER UNDERPLATE.</p> <p>7 -CAUTION- REFLOW PROCESS WILL DAMAGE CAGE ASSEMBLY.</p> |
|--|---|

DETACHED LISTS	MM (INCH)	DFTO tzou	DATE 06/02/06'	FULL RISE ELECTRONIC CO., LTD (Non-Logo) XFP CAGE WITH PCI HEAT SINK KIT	
	TOLERANCES EXCEPT AS NOTED	CHKD	DATE		
		MFO	DATE		
		APPVL	DATE		
	MATERIAL :	QT'Y :			
	ANGLES ± 0.5	FINISH :	DRAWING NO. XFPO03-L		SIZE A3
	 THIRD ANGLE PROJECTION	SCALE : 1 : 2	/PART NO. SEE NOTE		REV 0
DO NOT SCALE DRAWING			SHEET 2 OF 2		