TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC590AP, TC74HC590AF

8-Bit Binary Counter/Register with 3-State Outputs

The TC74HC590A is a high speed CMOS 8-BIT COUNTER/REGISTER fabricated with silicon gate C^2MOS technology.

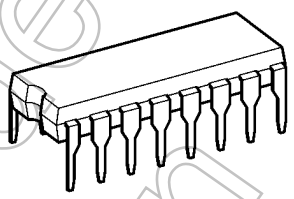
It achieves the high speed operation similar to epuivalent LSTTL while maintaining the CMOS low power dissipation.

The internal counter counts on the positive going edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is low. When Counter Clear ($\overline{CCLR}$) is low, the internal counter is cleared asynchronously to the clock.

Data in the internal counter are loaded into the register at positive going edge of Register Clock (RCK), and the register outputs are controlled by enable input ($\overline{G}$).

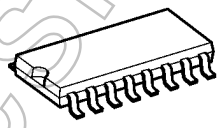
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC590AP



DIP16-P-300-2.54A

TC74HC590AF



SOP16-P-300-1.27A

Weight

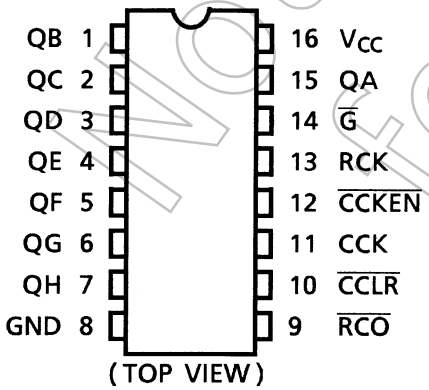
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Features

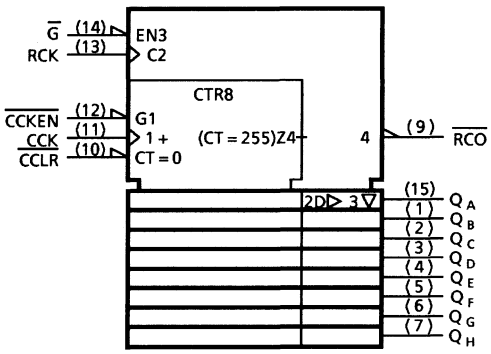
- High speed: f_{max} = 62 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 15 LSTTL loads for QA to QH
  10 LSTTL loads for $\overline{RCO}$
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
  For QA to QH
  $|I_{OH}| = I_{OL}$ = 4 mA (min)
  For $\overline{RCO}$
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS590

Pin Assignment

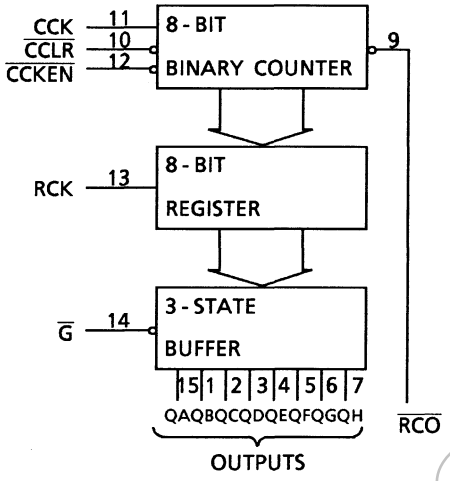


Start of commercial production
1988-05

IEC Logic Symbol



Block Diagram



Truth Table

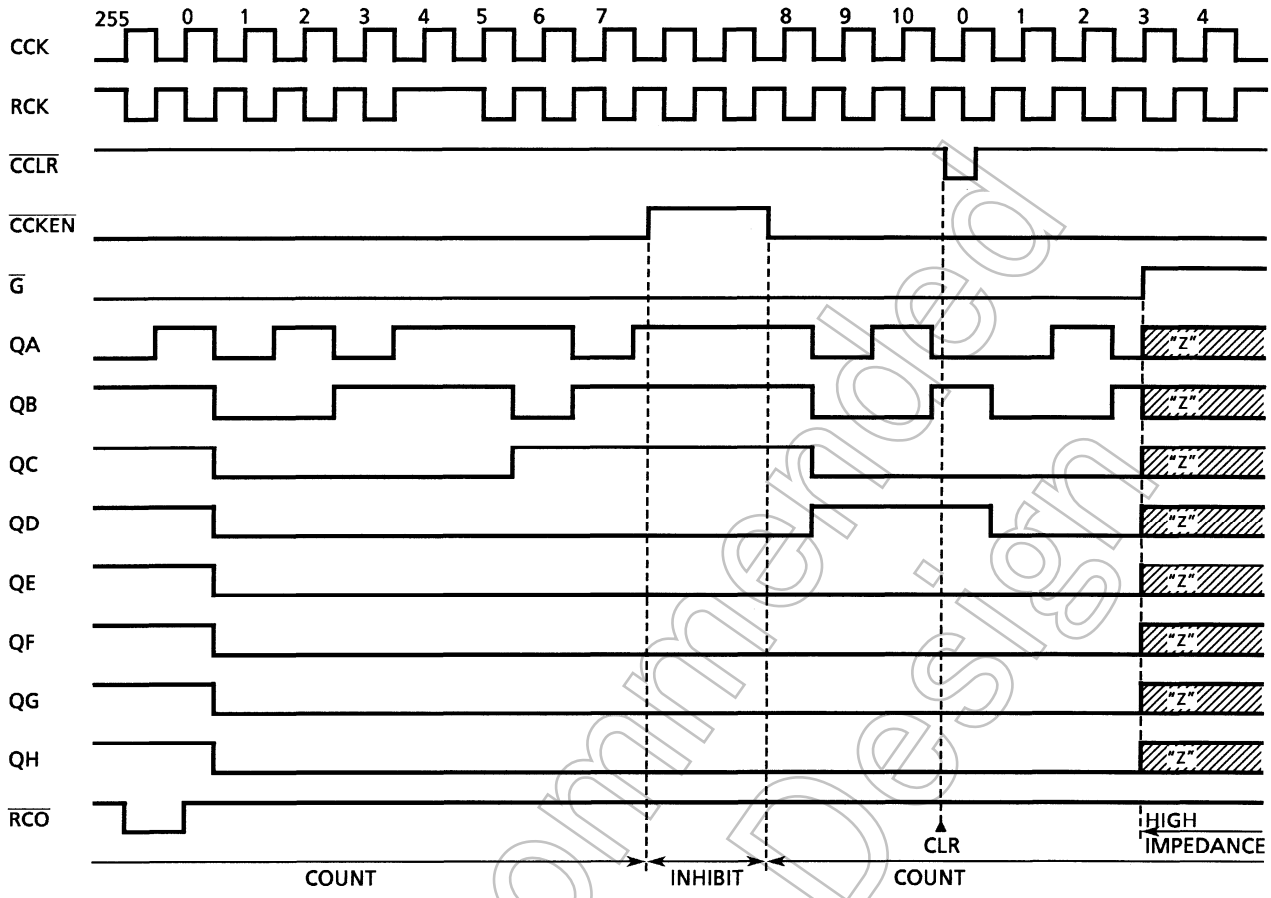
Inputs					Function
G	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q Outputs Disable
L	X	X	X	X	Q Outputs Enable
X	↑	X	X	X	Counter Data is Stored into Register
X	↓	X	X	X	Register State is not Changed
X	X	L	X	X	Counter Clear
X	X	H	L	↑	Advance One Count
X	X	H	L	↓	No Count
X	X	H	H	X	No Count

X: Don't care

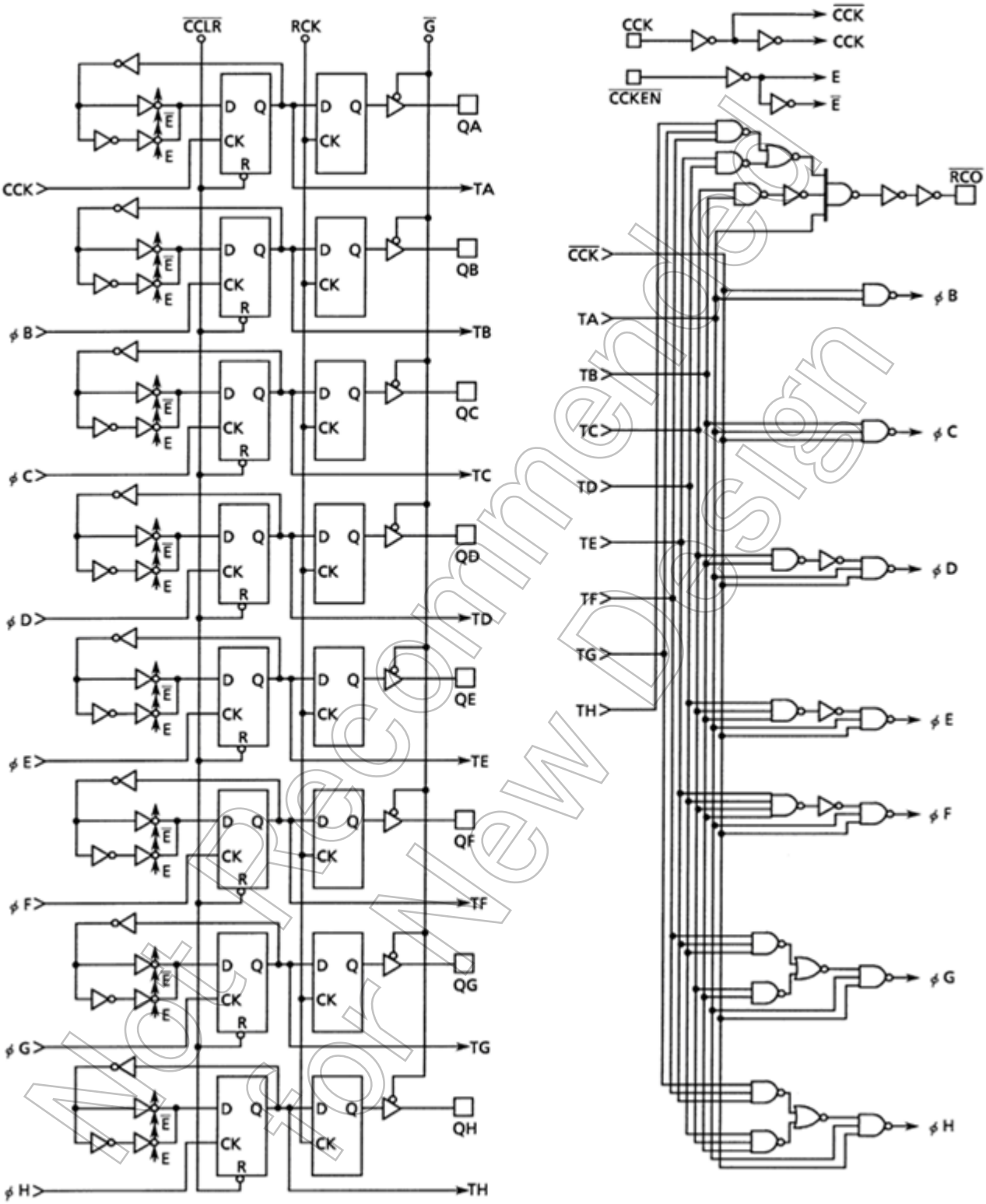
$\overline{RCO} = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA' to QH': internal outputs of the counter)

Timing Chart



Logic Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current ($\overline{RCO}$)	I_{OUT}	±25	mA
DC output current (QA to QH)	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V)	ns
		0 to 500 (V_{CC} = 4.5 V)	
		0 to 400 (V_{CC} = 6.0 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition			V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—			2.0	1.50	—	—	1.50	—	V
					4.5	3.15	—	—	3.15	—	
					6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—			2.0	—	—	0.50	—	0.50	V
					4.5	—	—	1.35	—	1.35	
					6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}		I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
					4.5	4.4	4.5	—	4.4	—	
					6.0	5.9	6.0	—	5.9	—	
			$\overline{RCO}$	I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
				I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
			QA to QH	I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
				I_{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
					4.5	—	0.0	0.1	—	0.1	
					6.0	—	0.0	0.1	—	0.1	
			$\overline{RCO}$	I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
				I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
			QA to QH	I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
				I_{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND			6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND			6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND			6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CCK, RCK)	$t_{W(H)}$ $t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{CCLR}$)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{CCKEN}$-CCK)	t_s	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum set-up time (CCK-RCK)	t_s	—	2.0	—	200	250	ns
			4.5	—	40	50	
			6.0	—	34	43	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{CCLR}$)	t_{rem}	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	33	26	
			6.0	—	39	31	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time ($\overline{RCO}$)	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (CCK-$\overline{RCO}$)	t_{pLH} t_{pHL}	—	—	18	28	ns
Propagation delay time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pLH}	—	—	20	30	ns
Maximum clock frequency	f_{max}	—	32	62	—	MHz

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time (Qn)	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output transition time ($\overline{RCO}$)	t_{TLH} t_{THL}	—	50	2.0	—	30	75	—	95	ns
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation delay time ($CCK-\overline{RCO}$)	t_{pLH} t_{pHL}	—	50	2.0	—	75	163	—	205	ns
				4.5	—	22	33	—	41	
				6.0	—	17	28	—	35	
Propagation delay time ($\overline{CCLR}-\overline{RCO}$)	t_{pLH}	—	50	2.0	—	78	175	—	220	ns
				4.5	—	23	35	—	44	
				6.0	—	18	30	—	37	
Propagation delay time (RCK-Qn)	t_{pLH} t_{pHL}	—	50	2.0	—	62	145	—	180	ns
				4.5	—	19	29	—	36	
				6.0	—	15	25	—	31	
			150	2.0	—	78	185	—	230	
				4.5	—	24	37	—	46	
				6.0	—	19	31	—	39	
Output enable time	t_{pZL} t_{pZH}	$R_L = 1\ k\Omega$	50	2.0	—	43	105	—	130	ns
				4.5	—	14	21	—	26	
				6.0	—	12	18	—	22	
			150	2.0	—	58	150	—	190	
				4.5	—	19	30	—	38	
				6.0	—	16	26	—	33	
Output disable time	t_{pLZ} t_{pHZ}	$R_L = 1\ k\Omega$	50	2.0	—	33	105	—	130	ns
				4.5	—	16	21	—	26	
				6.0	—	12	18	—	22	
Maximum clock frequency	f_{max}	—	50	2.0	6	12	—	5	—	MHz
				4.5	30	51	—	24	—	
				6.0	35	80	—	28	—	
Input capacitance	C_{IN}	—			—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—			—	34	—	—	—	pF

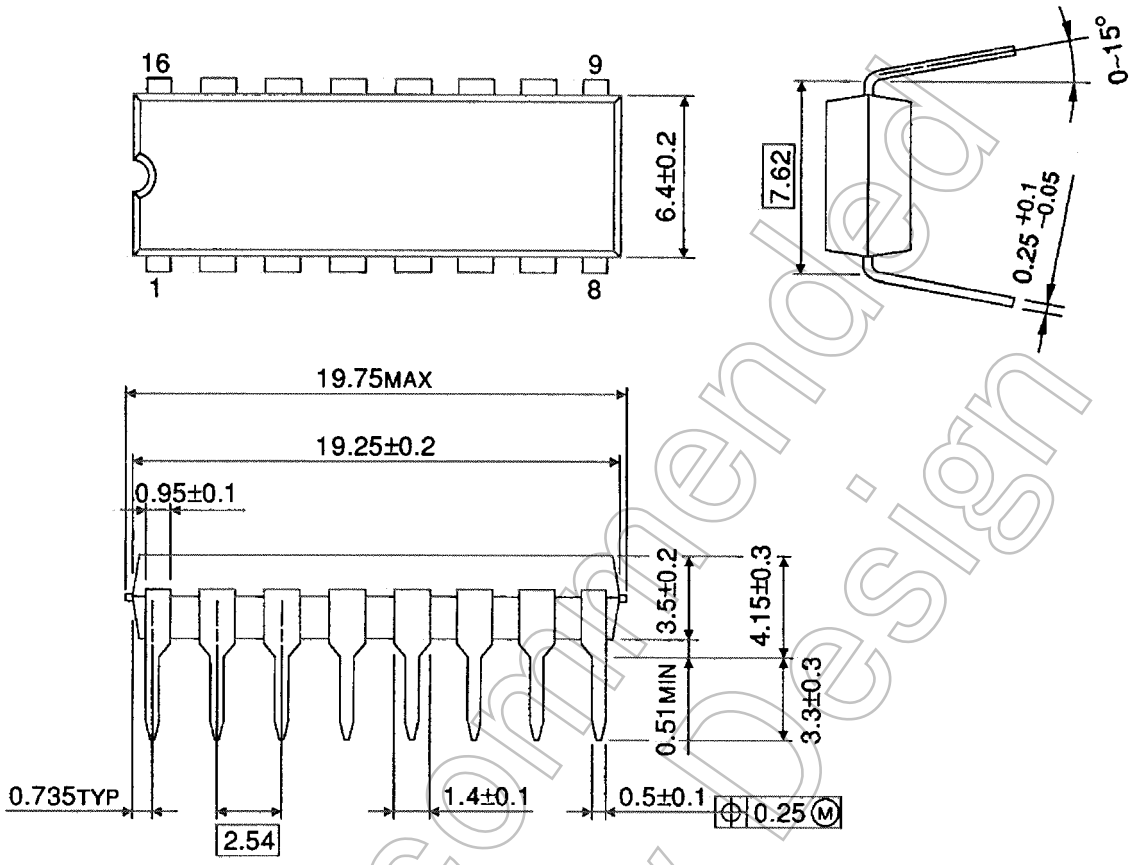
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions

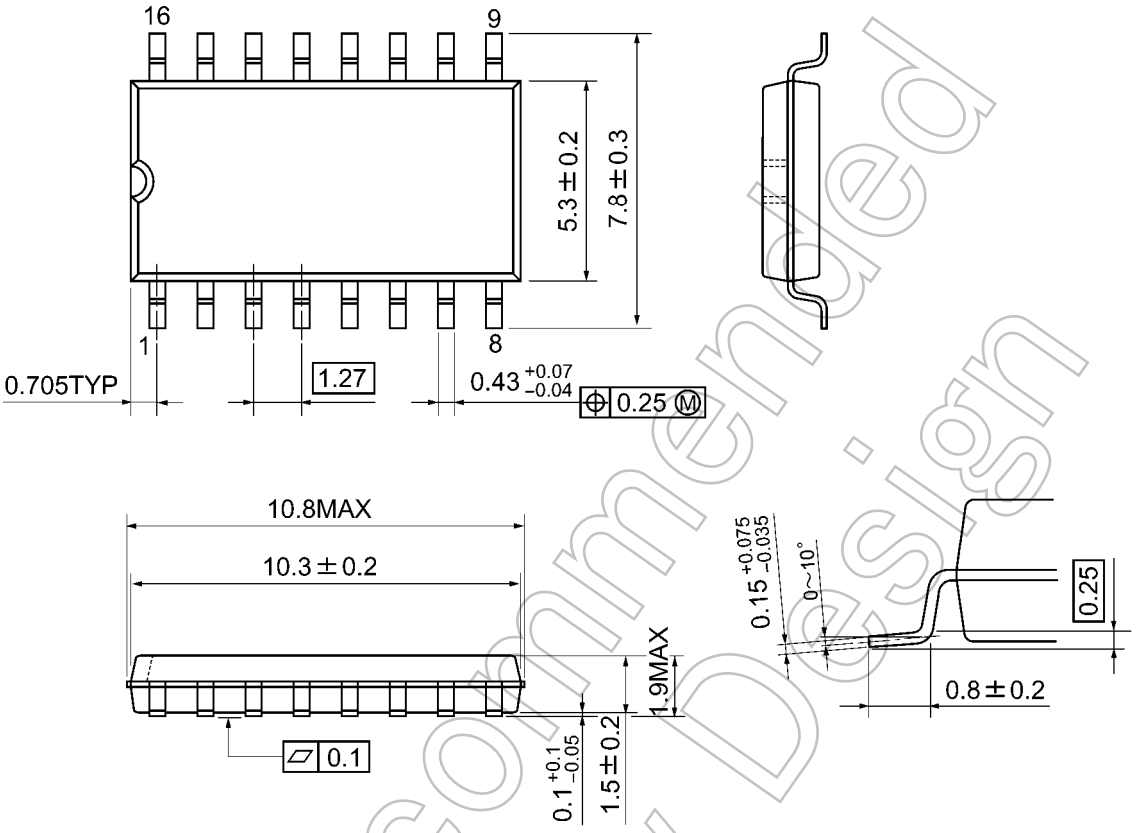
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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