

TC74LVX174F, TC74LVX174FT

Hex D-Type Flip-Flop with Clear

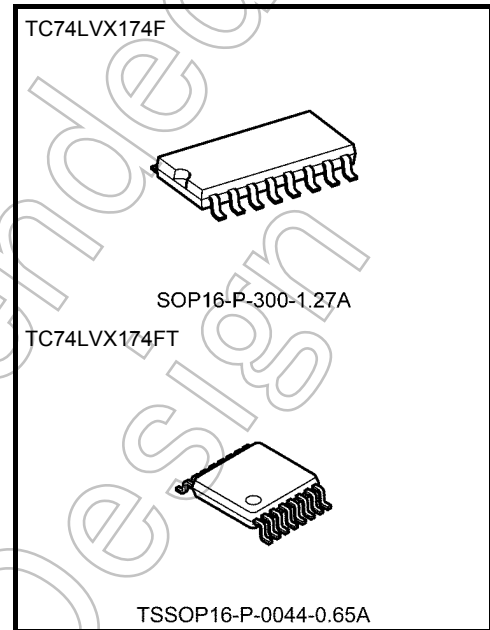
The TC74LVX174F/FT is a high-speed CMOS hex D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

Information signals applied to D inputs are transferred to the Q output on the positivegoing edge of the clock pulse. When the CLR input is held low, the Q output are in the low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High-speed: $f_{max} = 180 \text{ MHz (typ.) (VCC = 3 V)}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A (max) (Ta = 25^\circ\text{C})}$
- Input voltage level: $V_{IL} = 0.8 \text{ V (max) (VCC = 3 V)}$
 $V_{IH} = 2.0 \text{ V (min) (VCC = 3 V)}$
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 0.5 \text{ V (max)}$
- Pin and function compatible with 74HC174

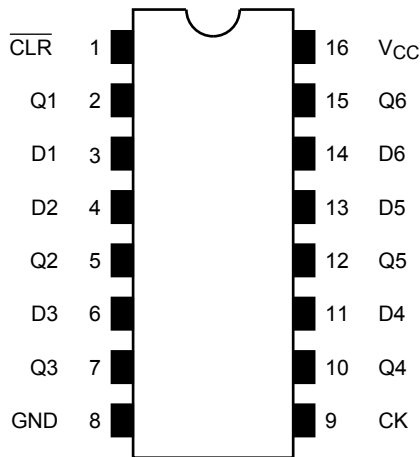


Weight

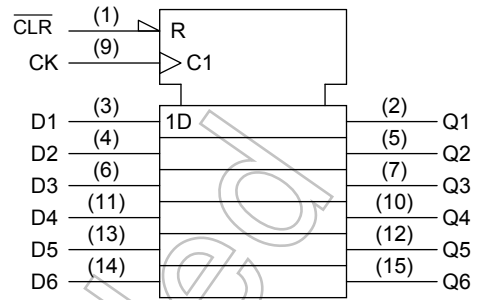
SOP16-P-300-1.27A	: 0.18 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)

Start of commercial production
1993-01

Pin Assignment (top view)



IEC Logic Symbol

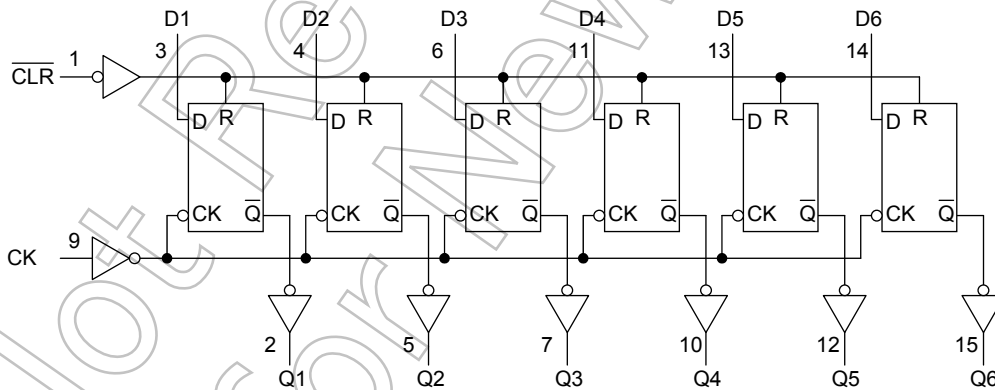


Truth Table

Inputs			Outputs	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L	\uparrow	L	—
H	H	\uparrow	H	—
H	X	\downarrow	Qn	No change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^{\circ}C$			$T_a = -40 \text{ to } 85^{\circ}C$		Unit						
			V_{CC} (V)	Min	Typ.	Max	Min		Max					
Input voltage	H-level	—	V_{IH}	2.0	1.5	—	—	1.5	—	V				
				3.0	2.0	—	—	2.0	—					
				3.6	2.4	—	—	2.4	—					
	L-level			V_{IL}	2.0	—	—	0.5	—		0.5	V		
					3.0	—	—	0.8	—		0.8			
					3.6	—	—	0.8	—		0.8			
Output voltage	H-level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}		$I_{OH} = -50 \mu A$	2.0	1.9	2.0	—	1.9	—		V	
					$I_{OH} = -50 \mu A$	3.0	2.9	3.0	—	2.9	—			
					$I_{OH} = -4 \text{ mA}$	3.0	2.58	—	—	2.48	—			
	L-level			V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	2.0	—	0.0	0.1	—	0.1		V
						$I_{OL} = 50 \mu A$	3.0	—	0.0	0.1	—	0.1		
						$I_{OL} = 4 \text{ mA}$	3.0	—	—	0.36	—	0.44		
Input leakage current	I_{IN}	$V_{IN} = 5.5 \text{ V or GND}$	3.6			—	—	± 0.1	—	± 1.0	μA			
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	3.6			—	—	4.0	—	40.0	μA			

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Limit	Limit	
Minimum pulse width (CK)	t _{W(L)}	—	2.7	6.5	7.5	ns
	t _{W(H)}		3.3 ± 0.3	5.0	5.0	
Minimum pulse width ($\overline{\text{CLR}}$)	t _{W(L)}	—	2.7	6.5	7.5	ns
			3.3 ± 0.3	5.0	5.0	
Minimum set-up time	t _s	—	2.7	7.5	8.5	ns
			3.3 ± 0.3	5.0	6.0	
Minimum hold time	t _h	—	2.7	0	0	ns
			3.3 ± 0.3	0	0	
Minimum removal time ($\overline{\text{CLR}}$)	t _{rem}	—	2.7	4.5	4.5	ns
			3.3 ± 0.3	3.0	3.0	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max		Min	Max
Propagation delay time (CK-Q)	t _{pLH}	—	2.7	15	—	7.6	14.5	1.0	17.5	ns
				50	—	10.1	18.0	1.0	21.0	
	t _{pHL}		3.3 ± 0.3	15	—	5.9	9.3	1.0	11.0	
				50	—	8.4	12.8	1.0	14.5	
Propagation delay time ($\overline{\text{CLR}}$ -Q)	t _{pHL}	—	2.7	15	—	7.9	15.0	1.0	18.5	ns
				50	—	10.4	18.5	1.0	22.0	
			3.3 ± 0.3	15	—	6.2	9.7	1.0	11.5	
				50	—	8.7	13.2	1.0	15.0	
Maximum clock frequency	f _{max}	—	2.7	15	65	130	—	55	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	115	180	—	95	—	
				50	65	95	—	55	—	
Output to output skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}									
Input capacitance	C _{IN}			(Note 2)	—	4	10	—	10	pF
Power dissipation capacitance	C _{PD}			(Note 3)	—	29	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

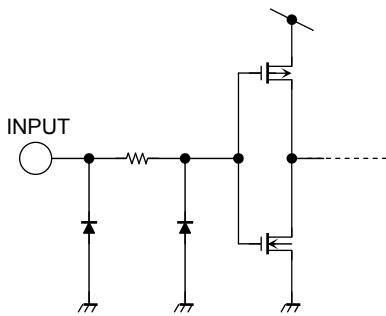
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 19 + 10 \cdot n$$

Noise Characteristics (Ta = 25°C, input: tr = tf = 3 ns, CL = 50 pF)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Limit	Unit
Quiet output maximum dynamic VOL	VOLP	—	3.3	0.3	0.5	V
Quiet output minimum dynamic VOL	VOLV	—	3.3	-0.3	-0.5	V
Minimum high level dynamic input voltage VIH	VIHD	—	3.3	—	2.0	V
Maximum low level dynamic input voltage VIL	VILD	—	3.3	—	0.8	V

Input Equivalent Circuit

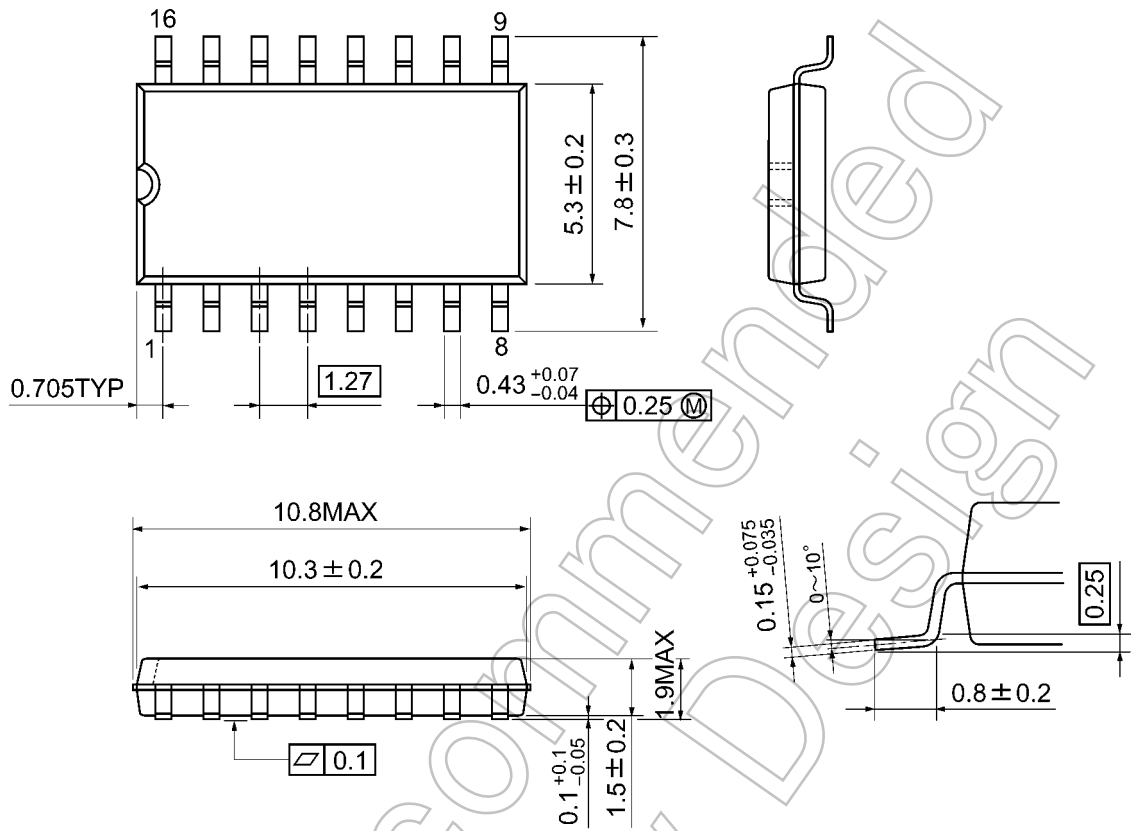


Not Recommended for New Design

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



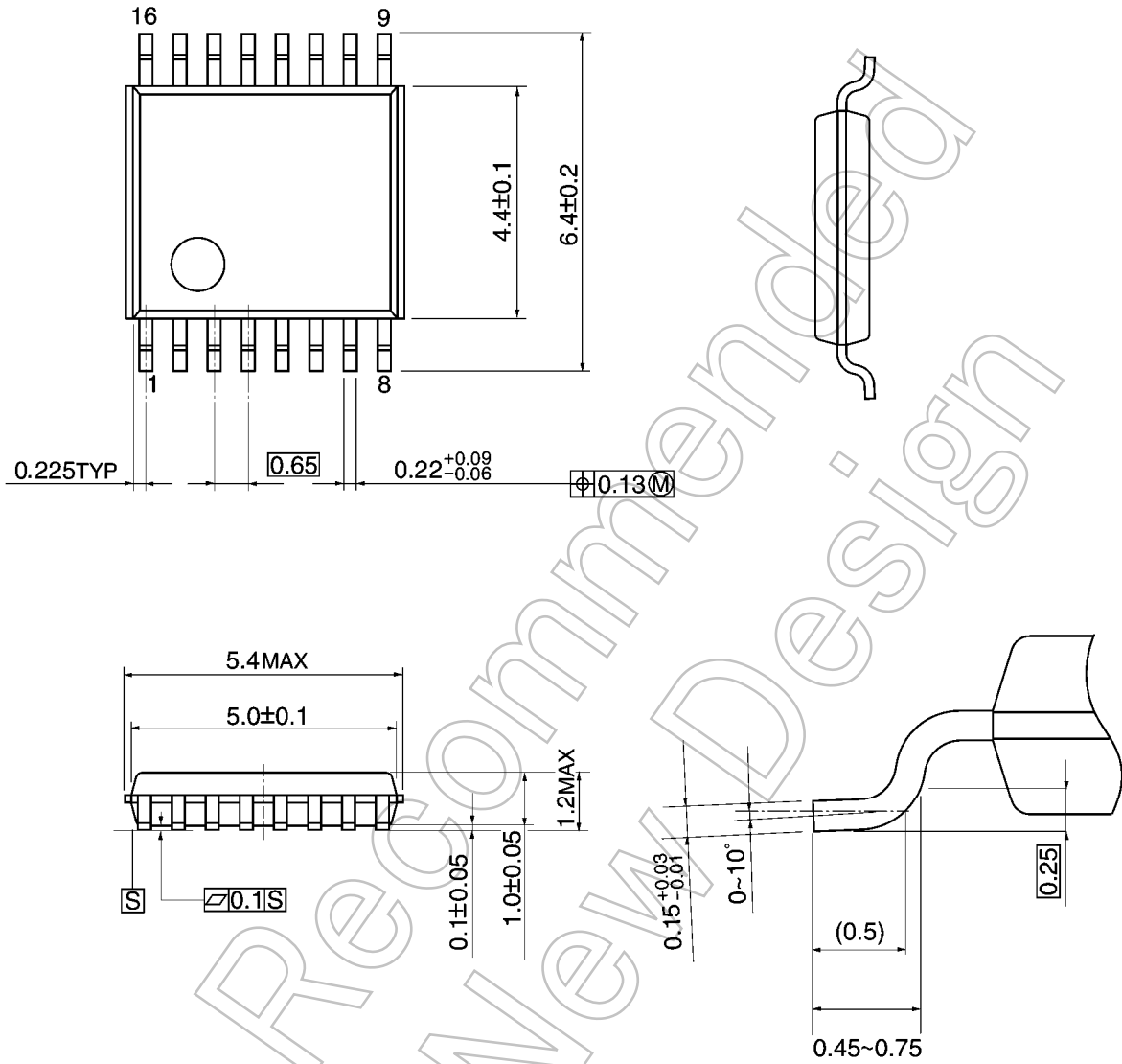
Weight: 0.18 g (typ.)

Not Recommended for New Design

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

Not Recommended for New Design

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