

19MHz to 800MHz Low Phase-Noise VCXO PIN CONFIGURATION

FEATURES

- < 0.5ps RMS phase jitter (12kHz to 20MHz) at 622.08MHz (LVPECL/LVDS)
- 30ps max peak to peak period jitter
- Ultra Low-Power Consumption
 - < 90mA @622MHz PECL output
 - <10 μA at Power Down (PDB) Mode
- Input Frequency:
 - Fundamental Crystal: 19MHz to 44MHz
- Output Frequency:
 - 19MHz to 800MHz output.
- Output types: LVPECL, LVDS, or LVCMOS.
- High Linearity VCXO: <10% linearity
- Pullability: ±150 ppm
- Programmable OE input polarity,
 o Programmable Hi-Z or Active Low disabled
 state (CMOS output only)
- Power Supply: 3.3V, ±10%
- Operating Temperature Ranges:
 - Commercial: 0°C to 70°C
 Industrial: -40°C to 85°C
 Available in TSSOP package

XIN **XOUT** 16 l **VCON** 2 15] VDDANA VDDDIG DNC 3 14 OE/PDB 4 7 VDDBUF 13 DNC [12 ∃ QB GNDANA [11 **GNDDIG** 10 ΠQ **GNDBUF** 9 DNC TSSOP-16L

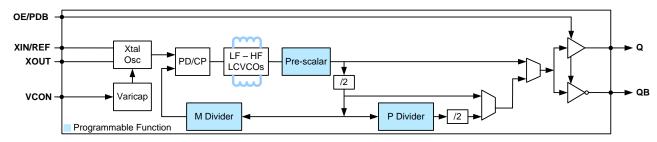
DESCRIPTION

The PL585 is a Dual LC core monolithic IC VCXO, capable of maintaining sub-picoseconds RMS phase jitter, while covering a wide frequency output range up to 800MHz, without the use of external components. The high performance and high frequency output is achieved using a low cost fundamental crystal of between 19MHz and 44 MHz. The PL585 is designed to address the demanding requirements of high performance applications such Fiber Channel, serial ATA, Ethernet, SAN, SONET/SDH, etc.

OUTPUT ENABLE CONTROL

OE Options (Programmable)	OE	State
Conventional	0 (Default)	Output enabled
Polarity	1	Tri-state
Reverse	0	Tri-state
Polarity	1 (Default)	Output enabled

BLOCK DIAGRAM





PIN ASSIGNMENT

Name	Pin #	Type	Description
XIN	1	I	Crystal input connection.
VCON	2	I	Analog voltage control pin.
DNC	3, 5, 9	-	Do Not Connect.
OE/PDB	4	I	This pin may be programmed as output enable (OE), or power-down (PDB) pin. This pin incorporates an Internal pull-up resistor of $60K\Omega$ for OE, and PDB, operations.
GND_ANA	6	Р	GND connection for analog circuitry.
GND_DIG	7	Р	GND connection for digital circuitry.
GND_BUF	8	Р	GND connection for buffer circuitry.
Q	10	0	True Output buffer.
QB	12	0	Complementary Output buffer.
VDD_BUF	11, 13	Р	VDD connection for buffer circuitry.
VDD_DIG	14	Р	VDD connection for digital circuitry.
VDD_ANA	15	Р	VDD connection for analog circuitry.
XOUT	16	Р	Output connection to crystal.

OPTION SELECTION TABLE

PL585 is a fully programmable VCXO IC. However, for ordering convenience, the following part numbers have been created for when simple multiplication is used, for your convenience. When other features of the IC are exercised (i.e. reverse polarity on OE, power down, etc.), another 3-digit code is used to identify the functionality.

Input Crystal	Multiplication	Output Frequen	cy Range (MHz)	- Part #
Frequency Range (MHz)	Factor	Low Limit	High Limit	- Fail#
33.750000 ~ 40.000000	X20	675.00	800.00	PL585-P8-020
33.333333 ~ 42.187500	X16	533.33	675.00	PL585-P8-168
32.142857 ~ 38.095238	X14	450.00	533.33	PL585-P8-148
33.333333 ~ 37.500000	X12	400.00	450.00	PL585-P8-128
33.750000 ~ 40.000000	X10	337.50	400.00	PL585-P8-108
33.333333 ~ 42.187500	X8	266.67	337.50	PL585-P8-088
32.142857 ~ 38.095238	X7	225.00	266.67	PL585-P8-078
33.333333 ~ 37.500000	X6	200.00	225.00	PL585-P8-068
33.750000 ~ 40.000000	X5	168.75	200.00	PL585-P8-058
33.333333 ~ 42.187500	X4	133.33	168.75	PL585-P8-048
32.142857 ~ 38.095238	X3.5	112.50	133.33	PL585-P8-358
33.333333 ~ 37.500000	X3	100.00	112.50	PL585-P8-038
33.750000 ~ 40.000000	X2.5	84.375	100.00	PL585-P8-258
32.812500 ~ 42.187500	X2	65.625	84.375	PL585-P8-028

Common functionality for packaged parts in the above table: OE function active high polarity. Please inform your Sales representative for active low OE functionality.



FUNCTIONAL DESCRIPTION

PL585 family of products is an advanced, programmable LCVCO VCXO IC that is designed to meet the most stringent performance specifications for phase noise, jitter, and power consumption.

There are two main types of VCOs, a) Ring Oscillator, b) LC Tank oscillator. An LCVCO is made up of LC tank oscillator. Although a Ring Oscillator has very good performance, and has a good tuning range, its phase noise and jitter performance, in particular at higher frequencies, degrades.

On the other hand, an LCVCO has an outstanding phase noise and jitter performance, even at higher frequencies. PL585 family of products takes advantage of this state of the art technology, and incorporates the LC tank on-chip, for optimal performance.

PL585 family of products exhibit very low phase noise/phase jitter and peak to peak jitter, wide tuning range, and very low-power. All members of the PL585 family accept a low-cost fundamental crystal input of 19MHz to 44MHz, and its flexible core is capable of producing any output frequency between 19MHz to 800MHz.

PLL Programming

The PLL in the PL585 family is fully programmable. Micrel programming software is used to configure and program the IC.

OE (Output Enable)

The OE pin in PL585 family, through programming, can be configured to support OE pin activation with a logic '1' or logic '0', to provide you with the desired enable polarity.

OE Options (Programmable)	OE	State
Conventional	0 (Default)	Output enabled
Polarity	1	Tri-state
Reverse	0	Tri-state
Polarity	1 (Default)	Output enabled

In addition, The OE feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode, for CMOS outputs. The programming control for the OE options is shown below:

OE Pin	Osc	PLL	Output			
0	On	On	Hi Z			
	On	On	Active '0' (CMOS Only)			
1	Normal Operation (Default)					

Note: Typical enable time is <50ns plus one clock period.

The OE pin incorporates a $60 \text{K}\Omega$ resistor to either pull-up or pull-down to the default state when the OE pin is left open.

Power-Down Control (PDB)

When activated, this programmable feature 'Disables the VCO, the oscillator circuitry, counters, and all other active circuitry. PDB activation disables all outputs and the IC consumes <15 μ A of power, in the power down mode, to conserve power. The PDB input incorporates a 10M Ω pull up resistor for normal operating condition.

The PDB feature can be programmed to allow the output to float (Hi Z), or to operate in the 'Active low' mode, in CMOS output. The logic for PDB is shown below:

PDB Pin	Osc.	PLL	Output			
	Off	Off	Hi Z			
0	Off	Off	Active '0' (CMOS Only)			
1	Normal Operation (Default)					

Note: Typical enable time is <10ms.



ELECTRICAL SPECIFICATIONS

1. ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	Vı	-0.5	V _{DD} +0.5	V
Output Voltage	Vo	-0.5	V _{DD} +0.5	V
Storage Temperature	Ts	-65	150	°C
Ambient Operating Temperature (industrial temperature)*	T _{AI}	-40	85	°C
Ambient Operating Temperature (commercial temperature)	T _{AC}	0	70	°C
Junction Temperature	TJ		125	°C
ESD Protection, Human Body Model		2		kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permane nt damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. GENERAL ELECTRICAL SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	I _{DDQ}	LVPECL, 622.08MHz, 3.3V			90	mA
Supply Current, PDB Enabled		PDB = 0, 3.3V			10	uA
Output Enable Time	toE	OE logic 0 to logic 1, Ta=25° C. Add one clock period to this measurement for a usable clock output.			50	ns
Power Up Time	T _{PU}	PDB logic 0 to logic 1, Ta=25° C.			10	ms
Operating Voltage	V_{DD}		2.97	3.3	3.63	V
Power Up Ramp Rate	t _{PU}	Time for V_{DD} to reach 90% V_{DD} . Power ramp must be monotonic.	0.1		100	ms
Auto-Calibration Time	t _{AC}	At power up			10	ms
Output Clock Duty Cycle		@ 50% of output waveform	45	50	55	%



3. VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCXO Pullability		VCON=1.65V, ± 1.65 V XTAL C ₁ >10fF and C ₀ /C ₁ <250		±150		ppm
VCXO Tuning Characteristic				100		ppm/V
Pull Range Linearity					10	%
VCON Pin Input Impedance			10			МΩ
VCON Modulation BW		$0V \le VCON \le 3.3V$, $-3dB$	18			kHz

4. CRYSTAL SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Resonator Frequency	F _{XIN}	Parallel Fundamental Mode	19		44	MHz
Crystal Cload	C _{L_Crystal}	V _{DD} = 3.3V, VCON = 1.65V		8.5		
Shunt Capacitance	C _{0_Crystal}				3.5	pF
Crystal Pullability	C ₀ /C ₁	AT cut	250			
Documented ESD	D	AT cut, up to 40MHz			45	Ω
Recommended ESR	R _E	AT cut, up to 44MHz			40	Ω

5. JITTER SPECIFICATIONS

PARAMETERS	FREQUENCY	CONDITIONS	MIN	TYP	MAX	UNITS
RMS Phase Jitter	622.08MHz	12kHz to 20MHz, XIN=38.88MHz		0.5		ps
Period Jitter, Pk-to-Pk	622.08MHz	10K cycles, LVPECL (-88) XIN=38.88MHz		25		nc
	212.5MHz	10K cycles, LVCMOS (-27), XIN=26.5625MHz		35		ps

6. PHASE NOISE SPECIFICATIONS

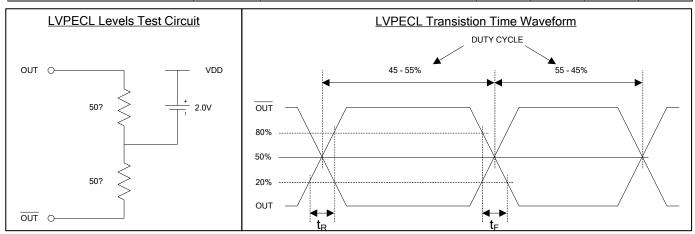
PARAMETERS	Freq. (MHz)	@ 10Hz	@ 100Hz	@ 1KHz	@ 10KHz	@ 100KHz	@ 1MHz	@ 10MHz	UNITS
Phase Noise, relative	155.52	-56	-86	-112	-123	-127	136	147	dBc/Hz
to carrier (typical)	622.08	-47	-77	-101	-111	-114	-127	-145	UDC/HZ

Note: Phase Noise measured at VCON = 1.65V



7. LVPECL OUTPUTS (Q, QB)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V _{OH}	Q, QB	2.275	2.350	2.420	٧
Output Low Voltage	V_{OL}	Standard LVPECL Termination, $V_{DD} = 3.3V$	1.490	1.600	1.680	V
Output Frequency	Fout	3.3V	19		800	MHz
Output Rise, Fall Times	t _r , t _f	20% - 80% of output waveform		300	500	ps
Output Voltage Swing	V _{pp}	Q, QB	550	800	930	mV



LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces (<1 inch) as "striplines" or "microstrips" with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

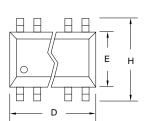
- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply
- Multiple V_{DD} pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are $0.1 \, \mu F$ for designs using frequencies < 50MHz and $0.01 \, \mu F$ for designs using frequencies > 50MHz.

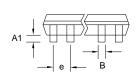


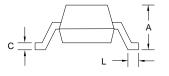
PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

TSSOP-16L

Cymphol	Dimension in MM		
Symbol	Min.	Max.	
Α	-	1.20	
A1	0.05	0.15	
b	0.19	0.30	
С	0.09	0.20	
D	4.90	5.10	
E	4.30	4.50	
Н	6.20	6.60	
Ĺ	0.45	0.75	
е	0.65 BSC		







ORDERING INFORMATION

For part ordering, please contact our Sales Department:

2180 Fortune Drive, San Jose, CA 95131, USA Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following: Part number, Package type, Thickness and Operating temperature range

Part PL585-XX-XXX XX
Number
Programming
Code
Packaging
Ontion

Temperature Range
C = Commercial (0°C to 70°C)
L = Industrial (-45°C to

I = Industrial (-45°C to +85°C)

Part Number/Order Number	Marking†	Package Option		
PL585-XX-XXXOC	P585-XX	16-Pin TSSOP (Tube)		
PL585-XX-XXOC-R	- XXX(I) LLLLL	16-Pin TSSOP (Tape and Reel)		

Marking Notes:

Micrel Inc., reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Micrel is believed to be accurate and reliable. However, Micrel makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: Micrel's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Micrel Inc.

¹⁾ The "I" after the 3 digit programming code will be marked for Industrial Temperature grade products only. Commercial grade products will not have a character in this position.