

**SY56216R**
**Low Voltage 1.2V/1.8V/2.5V CML Dual  
Channel Buffer 4.5GHz/6.4Gbps with  
Equalization**


Precision Edge®

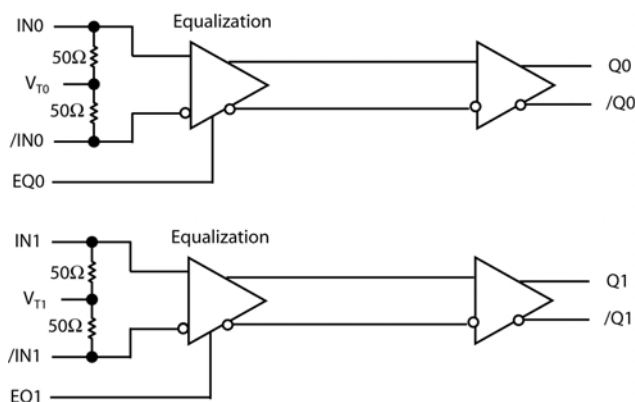
**General Description**

The SY56216R is a fully-differential, low-voltage 1.2V/1.8V/2.5V CML Dual Channel Buffer with input equalization. The SY56216R can process clock signals as fast as 4.5GHz or data patterns up to 6.4Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to CML differential signals, without any level-shifting or termination resistor networks in the signal path. The differential input can also accept AC-coupled LVPECL and LVDS signals. Input voltages as small as 200mV (400mV<sub>pp</sub>) are applied before the 9", 18" or 27" FR4 transmission line. For AC-coupled input interface applications, an internal voltage reference is provided to bias the V<sub>T</sub> pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY56216R operates from a 2.5V ±5% core supply and a 1.2V, 1.8V or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY56216R is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

**Functional Block Diagram**

Precision Edge is a registered trademarks of Micrel, Inc.

**Features**

- 1.2V/1.8V/2.5V CML Dual Channel Buffer
- Guaranteed AC performance over temperature and voltage:
  - DC-to > 6.4Gbps Data throughput
  - DC-to > 4.5GHz Clock throughput
  - <280ps propagation delay (IN-to-Q)
  - <20ps within-device skew
  - <80ps rise/fall times
- High-speed CML outputs
- 2.5V ±5% V<sub>CC</sub>, 1.2/1.8V/2.5V ±5% V<sub>CCO</sub> power supply operation
- Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

**Applications**

- Data Distribution:
- SONET clock and data distribution
- Fiber Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

**Markets**

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Metro area network equipment

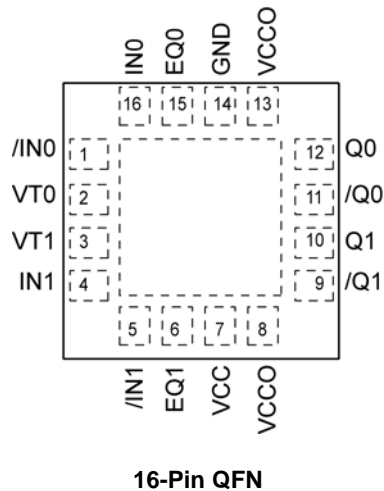
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY56216RMG	QFN-16	Industrial	R216 with Pb-Free bar-line indicator	NiPdAu / Pb-Free
SY56216RMGTR(2)	QFN-16	Industrial	R216 with Pb-Free bar-line indicator	NiPdAu / Pb-Free

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.

## Pin Configuration



## Truth Table

EQ Setting	EQUALIZATION FR4 6 mil Stripline
LOW	9"
FLOAT	18"
HIGH	27"

## Pin Description

Pin Number	Pin Name	Pin Function
16,1 4,5	IN0, /IN0 IN1, /IN1	Differential Inputs: Signals as small as 200mVpk (400mV <sub>PP</sub> ) applied to the input of 9, 18 or 27 inches 6 mil FR4 stripline transmission line are then terminated the differential input . Each input pin internally terminates with 50Ω to the VT pin.
2,3	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high-impedance resistor divider biases VT to allow input AC coupling. For AC coupling, bypass VT with 0.01μF low-ESR capacitor to VCC. See "Interface Applications" subsection and Figure 2a.
15,6	EQ0, EQ1	Three level inputs for equalization control. Low, Float, High
7	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low-ESR capacitors as close to the V <sub>CC</sub> pins as possible. Supplies input and core circuitry.
8,13	VCCO	Output Supply: Bypass with 0.1μF//0.01μF low-ESR capacitors as close to the V <sub>CCO</sub> pins as possible. Supplies the output buffers.
14	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
12,11 10,9	Q0, /Q0 Q1, /Q1	CML Differential Output Pairs: Differential buffered copy of the input signal. The output swing is typically 390mV. See "Interface Applications" subsection for termination information.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +3.0V  
 Supply Voltage ( $V_{CCO}$ ) ..... -0.5V to +3.0V  
 $V_{CC} - V_{CCO}$  ..... <1.8V  
 $V_{CCO} - V_{CC}$  ..... <0.5V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 CML Output Voltage ( $V_{OUT}$ ) ..... 0.6V to 3.0V  
 Current ( $V_T$ )  
     Source or sink on VT pin .....  $\pm 100$ mA  
 Input Current  
     Source or sink Current on (IN, /IN) .....  $\pm 50$ mA  
 Maximum Operating Junction Temperature ..... 125°C  
 Lead Temperature (soldering, 20sec.) ..... 260°C  
 Storage Temperature ( $T_s$ ) ..... -65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{CC}$ ) ..... 2.375V to 2.625V  
 ( $V_{CCO}$ ) ..... 1.14V to 2.625V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(3)</sup>  
 QFN  
     Still-air ( $\theta_{JA}$ ) ..... 75°C/W  
     Junction-to-board ( $\psi_{JB}$ ) ..... 33°C/W

### DC Electrical Characteristics<sup>(5)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{CC}$	Power Supply Voltage Range	$V_{CC}$	2.375	2.5	2.625	V
		$V_{CCO}$	1.14	1.2	1.26	
		$V_{CCO}$	1.7	1.8	1.9	
		$V_{CCO}$	2.375	2.5	2.625	
$I_{CC}$	Power Supply Current	Maximum $V_{CC}$ .		72	105	mA
$I_{CCO}$	Power Supply Current	No Load. Maximum $V_{CCO}$ .		32	42	mA
$R_{IN}$	Input Resistance (IN-to- $V_T$ , /IN-to- $V_T$ )		45	50	55	$\Omega$
$R_{DIFF\_IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	$\Omega$
$V_{IH}$	Input HIGH Voltage (IN, /IN)	IN, /IN	1.42		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (IN, /IN)	IN, /IN 1.22V=1.7-0.475	1.22		$V_{IH} - 0.2$	V
$V_{IN}$	Input Voltage Swing (IN, /IN)	See Figure 3a, applied to input of transmission line.	0.2		1.0	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing ( IN - /IN )	See Figure 3b, applied to input of transmission line.	0.4		2.0	V
$V_{T\_IN}$	Voltage from Input to $V_T$				1.28	V

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## CML Outputs DC Electrical Characteristics<sup>(6)</sup>

$V_{CCO} = 1.14V$  to  $1.26V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$ ,

$V_{CCO} = 1.7V$  to  $1.9V$ ,  $2.375V$  to  $2.625V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$  or  $100\Omega$  across the outputs,

$V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{OH}$	Output HIGH Voltage	$R_L = 50\Omega$ to $V_{CCO}$	$V_{CC} - 0.020$	$V_{CC} - 0.010$	$V_{CC}$	V
$V_{OUT}$	Output Voltage Swing	See Figure 3a	300	390	475	mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	See Figure 3b	600	780	950	mV
$R_{OUT}$	Output Source Impedance		45	50	55	$\Omega$

## Three Level EQ Input DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IH}$	Input HIGH Voltage		$V_{CC} - 0.3$			V
$V_{IL}$	Input LOW Voltage		0		$V_{EE} + 0.3$	V
$I_{IH}$	Input HIGH Current	$V_{IH} = V_{CC}$			400	$\mu A$
$I_{IL}$	Input LOW Current	$V_{IL} = GND$	-450			$\mu A$

### Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics

$V_{CCO} = 1.14V$  to  $1.26V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$ ,

$V_{CCO} = 1.7V$  to  $1.9V$ ,  $2.375V$  to  $2.625V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$  or  $100\Omega$  across the outputs,

$V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{MAX}$	Maximum Frequency	NRZ Data	6.4			Gbps
		$V_{OUT} > 200mV$ Clock	4.5			GHz
$t_{PD}$	Propagation Delay	IN-to-Q, Figure 1	100	180	280	ps
$t_{Skew}$	Within Device Skew	Note 7		4	20	ps
	Part-to-Part Skew	Note 8			100	ps
$t_{Jitter}$	Random Jitter	Note 9			1	$ps_{RMS}$
	Crosstalk Induced Jitter (Adjacent Channel)	Note 10			0.7	$ps_{PP}$
$t_R t_F$	Output Rise/Fall Times (20% to 80%)	At full output swing.	20	50	80	ps

### Notes:

7. Within device skew is the difference in  $t_{PD}$  between the two channels under identical input transition, temperature and power supply.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
9. Random jitter is measured with a K28.7 pattern, measured at  $\leq f_{MAX}$ .
10. Crosstalk induced jitter is defined as the added jitter that results from signals applied to the adjacent channel. It is measured at the output while applying a similar, differential clock frequency that is asynchronous with respect to each other at the adjacent input.

## Interface Applications

For Input Interface Applications see Figures 4a through 4e. For CML Output Termination see Figures 5a through 5d

### CML Output Termination with V<sub>CCO</sub> 1.2V

For V<sub>CCO</sub> of 1.2V, Figure 5a, terminate the output with 50Ω-to-1.2V, DC coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 5d, terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC couple with internally terminated receiver. For example, 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation. Any unused output pair needs to be terminated when V<sub>CCO</sub> is 1.2V, do not leave floating.

### CML Output Termination with 1.8V/2.5V V<sub>CCO</sub>

For V<sub>CCO</sub> of 1.8V or 2.5V, Figure 5a and Figure 5b, terminate with either 50Ω-to-V<sub>CCO</sub> or 100Ω differentially across the outputs. AC- or DC-coupling is fine. See Figure 5c for AC-coupling.

### Input AC-Coupling

The SY56216R input can accept AC-coupling from any driver. Bypass VT with a 0.1μF low ESR capacitor to VCC as shown in Figures 4b and 4c. VT has an internal high impedance resistor divider as shown in Figure 2a, to provide a bias voltage for AC-coupling.

### Input Termination

From 1.8V CML driver. Terminate with VT tied to 1.8V. Do not terminate 100 ohms differentially.

From 2.5V CML driver. Terminate with either VT tied to 2.5V or 100 ohms differentially.

The input cannot be DC-coupled from a 1.2V CML driver.

## Timing Diagrams

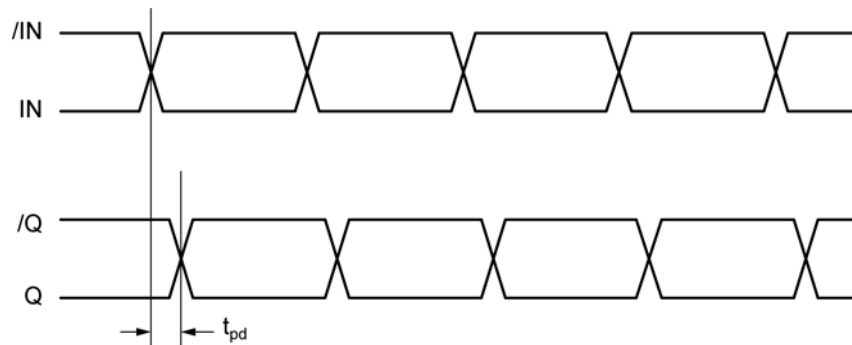
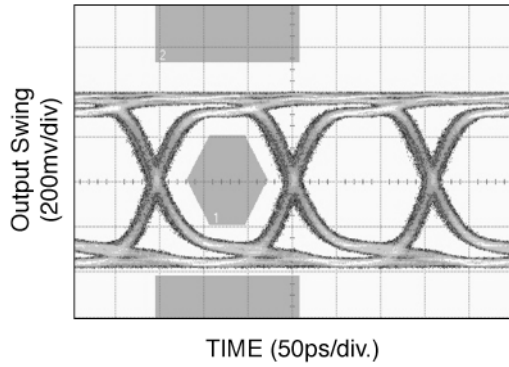


Figure 1. Propagation Delay

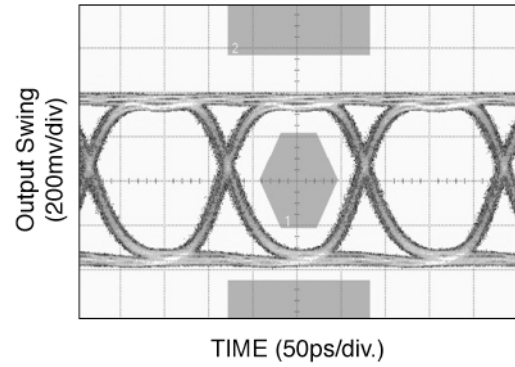
### Typical Characteristics

$V_{CC} = 2.5$ ,  $V_{CCO} = 1.2V$ ,  $GND = 0V$ ,  $V_{IN} = 160mV$ ,  $R_L = 50\Omega$  to  $1.2V$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

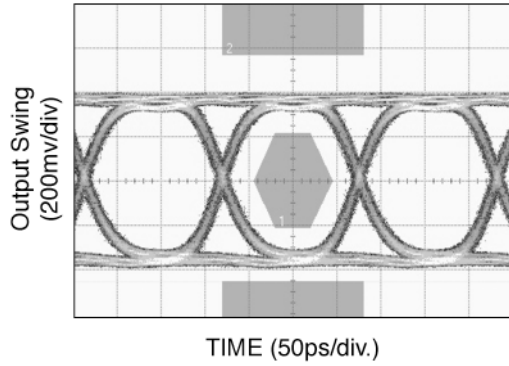
6.4Gbps, 24 inch FR4



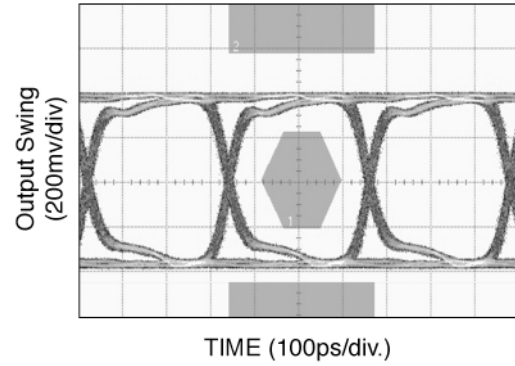
6.4Gbps, 18 inch FR4



6.4Gbps, 9 inch FR4



3.2Gbps, 24 inch FR4



### Input and Output Stage

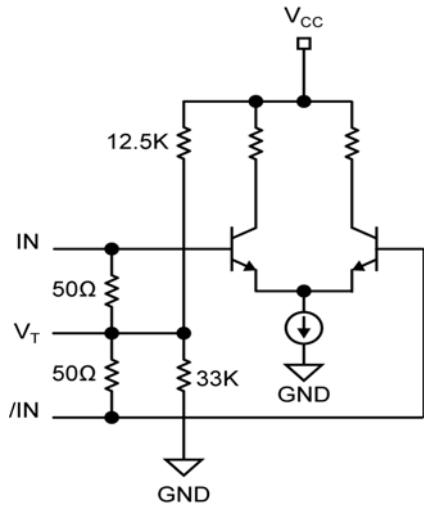


Figure 2a. Simplified Differential Input Buffer

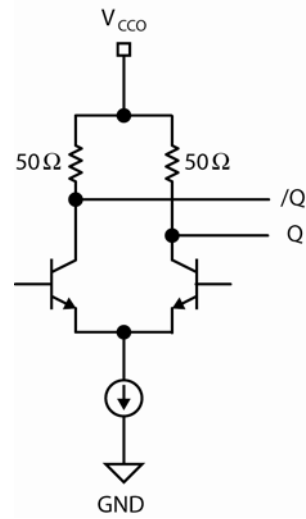


Figure 2b. Simplified CML Output Buffer

### Single-Ended and Differential Swings



Figure 3a. Single-Ended Swing

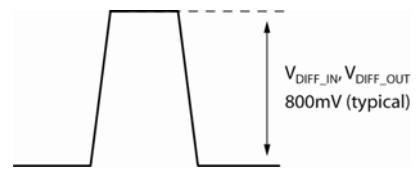
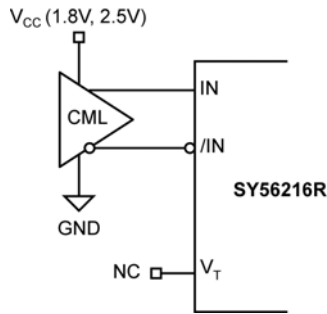


Figure 3b. Differential Swing

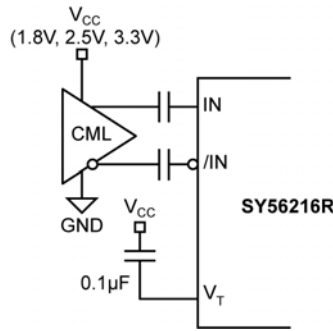


## Input Interface Applications

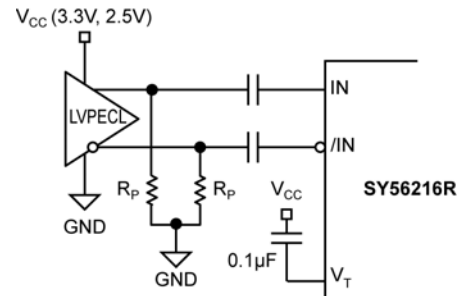


**Figure 4a. CML Interface (DC-Coupled, 1.8V, 2.5V)**

Option: May connect  $V_T$  to  $V_{CC}$

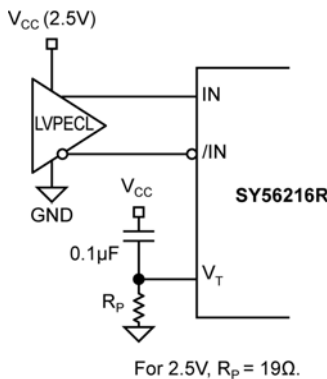


**Figure 4b. CML Interface (AC-Coupled)**



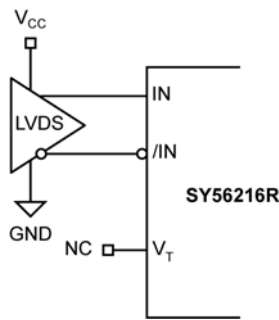
For 3.3V,  $R_p = 100\Omega$ .  
For 2.5V,  $R_p = 50\Omega$ .

**Figure 4c. LVPECL Interface (AC-Coupled)**



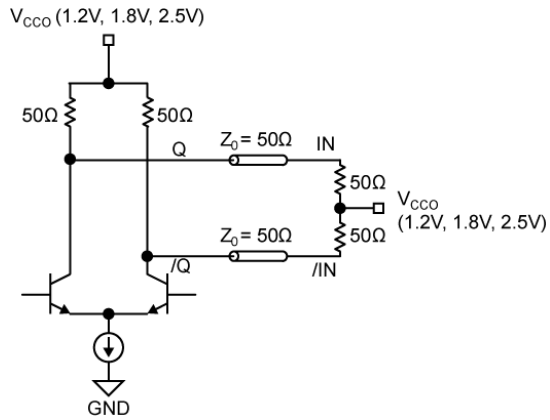
For 2.5V,  $R_p = 19\Omega$ .

**Figure 4d. LVPECL Interface (DC-Coupled)**

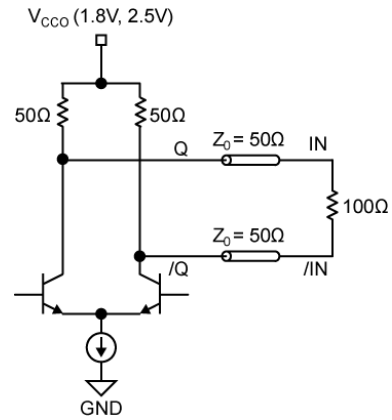


**Figure 4e. LVDS Interface**

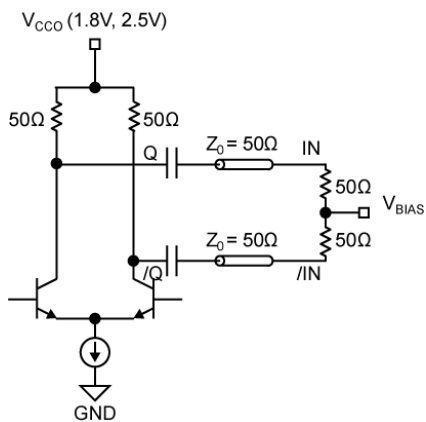
### CML Output Termination



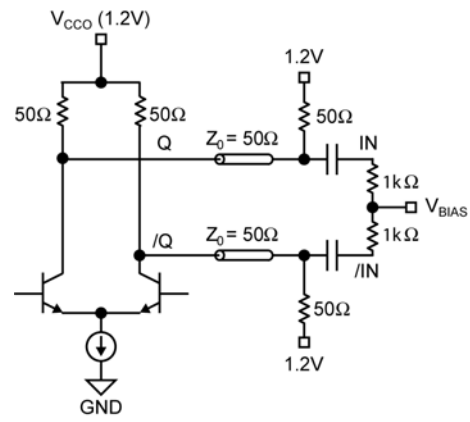
**Figure 5a. 1.2V 1.8V or 2.5V  
CML DC-Coupled Termination**



**Figure 5b. 1.8V or 2.5V  
CML DC-Coupled Termination**



**Figure 5c. CML AC-Coupled Termination  
(Vcc0 1.8V or 2.5V only)**

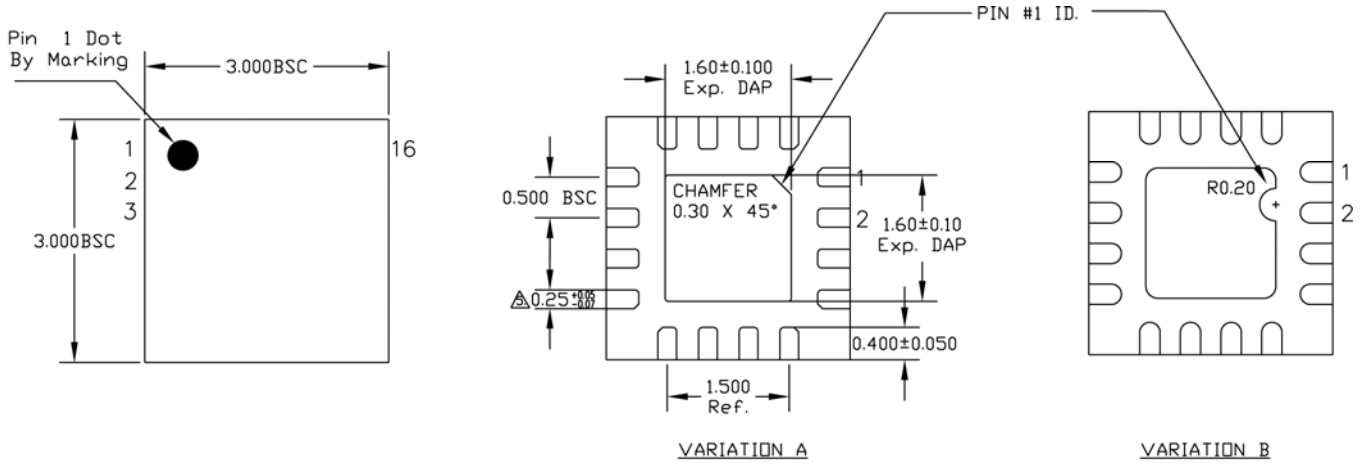


**Figure 5d. CML AC-Coupled Termination  
(Vcc0 1.2V only)**

### Related Product and Support Documents

Part Number	Function	Datasheet Link
HBW Solutions	New Products and Termination Application Notes	<a href="http://www.micrel.com/page.do?page=/product-info/as/HBWolutions.shtml">http://www.micrel.com/page.do?page=/product-info/as/HBWolutions.shtml</a>

**Package Information**



TOP VIEW

BOTTOM VIEW

SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- APPLIED ONLY FOR TERMINALS.
- APPLIED FOR EXPOSED PAD AND TERMINALS.

**16-Pin QFN**

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products, Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2008 Micrel, Incorporated.