# Low Power MEMS Jitter Attenuator

# ABMJB-902

# ESD Sensitive

## Moisture Sensitivity Level: MSL=1

#### **FEATURES**:

- Low power and miniature package programmable jitter attenuator
- Input/output frequency up to 200MHz
- I/Ô pins can be configured as output enable (OE), frequency switching (CSEL), power down (PDB) input, or CLK1 (2) output.
- <10µA current consumption with PDB active
- Operating temperature range from -40°C to +85°C
- 6-pin SOT23 RoHS-compliant packages
- Related devices:
  - ABMJB-903: Single-ended input, differential output, and phase noise cleaning

## **STANDARD SPECIFICATIONS:**

#### Absolute Maximum Ratings <sup>(1)</sup>

RoHS/RoHS II Compliant

## > APPLICATIONS:

- IEEE1588 GPIO clock cleanup
- FPGA-generated clock cleanup
- 1/10/40/100 Gigabit Ethernet (GbE)
- SONET/SDH
- PCI-Express
- CPRI/OBSAI wireless base stations
- Fibre Channel
- SAS/SATA
- DIMM

Parameters	Min.	Typ.	Max.	Units	Notes		
Supply Voltage (V <sub>DD</sub> )			+4.6	V			
Input Voltage (V <sub>IN</sub> )	-0.5		$V_{DD}$ +0.5	V			
Lead Temperature			+260	°C	Soldering, 20s		
Case Temperature			+115	°C			
Storage Temperature (T <sub>S</sub> )	-65		+150	°C			

#### **Operation Ratings**<sup>(2)</sup>

Parameters	Min.	Тур.	Max.	Units	Notes
Supply Voltage (V <sub>DD</sub> )	+2.25		+3.63	V	
Junction Thermal Resistance $(O_{JA})$			195	°C/W	SOT23, Still-Air
Ambient Temperature (T <sub>A</sub> )	-40		+85	°C	

#### **DC Electrical Characteristics**

 $V_{DD} = 3.3V \pm 10\%$  or 2.5V $\pm 10\%$ ; CL = 15pF; T<sub>A</sub> = 25°C

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Current dynamia (I)		12	18	mA	$V_{DD} = 3.3V, 30MHz, Load = 15pF$
Supply Current, dynamic (I <sub>DD</sub> )			<10	μA	When $PDB = 0$
Operating Voltage (V <sub>DD</sub> )	+2.25		+3.63	V	
Power Supply Ramp (t <sub>PU</sub> )	0.001		100	ms	Time for $V_{DD}$ to reach 90% $V_{DD}$ . Power ramp must be monotonic.
Output Current, low drive (I <sub>OLD</sub> )	4			mA	
Output Current, standard drive $(I_{OSD})$	8			mA	$V_{OL} = 0.4 V, V_{OH} = V_{DD} - 0.9 V, V_{DD} = 3.3 V$
Output Current, high drive (I <sub>OHD</sub> )	16			mA	5.5 (

Notes:

1. Exceeding the absolute maximum ratings may damage the device.

2. The device is not guaranteed to function outside tis operating ratings.







2.9 x 2.8 x 1.45 mm SOT23-6L

**ESD** Sensitive

(Pb) RoHS/RoHS II Compliant



2.9 x 2.8 x 1.45 mm SOT23-6L

#### **AC Electrical Characteristics**

 $V_{DD} = 3.3V \pm 10\%$  or 2.5V $\pm 10\%$ ; CL = 15pF; T<sub>A</sub> = 25°C

Parameters		Min.	Тур.	Max.	Units	Notes
Input (REFIN) Frequency	3.3V Operation	1		200	MIL	
	2.5V Operation	1		167	MITZ	
		0.8		V <sub>DD</sub>		Internally AC-coupled (high frequency)
Input Signal Amplitude		0.1		$V_{DD}$	$V_{PP}$	Internally AC-coupled (low frequency) For 3.3V operation, $F_{REFIN} \leq 50MHz$ For 2.5V operation, $F_{REFIN} \leq 40MHz$
		5		200		CLK0 and CLK1, 3.3V operation
Output Fraguanay		5		167	MUz	CLK0 and CLK1, 2.5V operation
Output Frequency		1.25		200	MITZ	CLK2, 3.3V operation
		1.25		167		CLK2, 2.5V operation
Settling Time				1	ms	At power up (after $V_{DD}$ increases over 2.25V)
Output Enable Time				10	ns	OE function: $T_A = 25^{\circ}C$ , 15pF load. Add one clock period to this measurement for a usable clock output
				1	ms	PDB function: $T_A = 25^{\circ}C$ , 15pF load
Output Rise Time			1.2	1.7	ns	15pF load, 10/90% $V_{\text{DD}},$ high drive, 3.3V
Output Fall Time			1.2	1.7	ns	15pF load, 10/90% $V_{\text{DD}},$ high drive, 3.3V
Duty Cycle		45	50	55	%	@2.5V and 3.3V over entire frequency range. Threshold = $V_{DD}/2$
Period Jitter (peak-	-to-peak) <sup>(3)</sup>		75		ps	10,000 samples measured
Jitter Attenuation Bandwidth			4		kHz	CLK0 = REFIN

Notes:

ABRACON IS

ISO9001:2008 CERTIFIED

3. Jitter performance can be considered the noise floor of the device. Jitter cannot be attenuated below this value.

### > **OPTIONS AND PART IDENTIFICATION:**

Please refer to the <u>ABMJB-902 Part Number and Configuration Guide</u> for available part numbers and configurations.





ESD Sensitive

(Pb) RoHS/RoHS II Compliant



**OUTLINE DIMENSION:** 



ABRACON IS ISO9001:2008 CERTIFIED



2 Faraday, Suite# B | Irvine | CA 92618 **Revised: 03.09.15** Ph. 949.546.8000 | Fax. 949.546.8001 Visit **www.abracon.com** for Terms and Conditions of Sale

**ESD** Sensitive

**(Pb)** RoHS/RoHS II Compliant



**PIN DESCRIPTION:** 

OE, PDB, CLK1 GND REFIN SOT23-6L package							
Pin No.	Pin Name	Pin Type	Pin Level	Function			
1	PDB, OE, CLK1	I/O	LVCMOS	Customizable pin: power down or output enable control input with pull-up or clock output			
2	GND	GND		Power supply ground			
3	REF_IN	I, (SE)	LVCMOS	Reference clock input			
4	VDD	PWR		Power supply			
5	CSEL, CLK2	I/O	LVCMOS	Customizable pin: configuration select control input with pull-up or clock output			
6	CLK0	0	LVCMOS	Clock output			

## **BLOCK DIAGRAM:**

ABRACON IS ISO9001:2008 CERTIFIED





ESD Sensitive



2.9 x 2.8 x 1.45 mm SOT23-6L

#### **FUNCTIONAL DESCRIPTION**

The ABMJB-902 series is a highly featured, very flexible, advanced programmable jitter filter design for high performance, low-power, small form-factor applications. The ABMJB-902 accepts a reference clock input between 1MHz and 200MHz and is capable of producing up to three outputs in the 5MHz to 200MHz range. The most common configuration will be comprised of the same input and output frequency, but this flexible design also allows frequency translation from one frequency to another frequency as long as both frequencies are within the specified ranges for input and output.

#### **Jitter Filter Programming**

Typically, the jitter filter settings will be optimized for one particular input and output frequency, but the flexible design also allows configurations for a certain frequency range, up to one octave wide.

The typical bandwidth of the jitter filter is 4kHz. This means that jitter frequency components above 4kHz will be attenuated. In case of frequency translation, the bandwidth may be slightly different.

#### Clock Output (CLK0)

CLK0 is the main clock output. The output drive level can be programmed to low drive (4mA), standard drive (8mA) or high drive (16mA). The maximum output frequency is 200MHz at 3.3V operation and 167MHz at 2.5V operation.

#### Clock Output (CLK1, CLK2)

The CLK1 and CLK2 feature allows the PL902xxx to have two additional clock outputs programmed to one of the following frequencies:

- CLK1 = CLK0
- CLK2 = CLK0, CLK0/2 or CLK0/4

CLK1 and CLK2 allow the same output drive level programming as CLK0. Because of the extra /2 and /4 settings, CLK2 is capable of going down to 1.25MHz. In case only an output clock of <5MHz is needed, CLK0 and CLK1 can be disabled.

#### **Output Enable (OE)**

The output enable feature allows the user to enable and disable the clock output(s) by toggling the OE pin. The OE pin incorporates a  $60k\Omega$  pull-up resistor, giving a default condition of logic "1".

#### **Power Down Control (PDB)**

The power down (PDB) feature allows the user to put the ABMJB-902 into sleep mode. When activated (logic "0"), PDB disables the synthesizer circuitry, counters, and all other active circuitry. In power down mode, the IC consumes  $<10\mu$ A of power. The PDB pin incorporates a 60k $\Omega$  pull-up resistor giving a default condition of logic "1".

#### **Configuration Select (CSEL)**

The configuration select (CSEL) feature allows the PL902xxx to switch between two pre-programmed configurations allowing the device on-the-fly frequency switching. The CSEL pin incorporates a  $60k\Omega$  pull-up resistor giving a default condition of logic "1".

Examples for this feature are:

- Select between two frequencies or two frequency ranges.
- Select between two frequency translations, like 1:1 and 1:2.



ESD Sensitive

(Pb) RoHS/RoHS II Compliant



2.9 x 2.8 x 1.45 mm SOT23-6L

#### **KEY PROGRAMMING PARAMETERS:**

CLK[0:2] Output Frequency	Output Drive Strength	Programmable Input/Output	
CLK0 = REFIN CLK1 = CLK0 CLK2 = CLK0, CLK0/2, or CLK0/4	Three optional drive strengths to choose from: • Low: 4mA	<ul> <li>One output pin can be configured as:</li> <li>OE – input</li> <li>PDB – input</li> </ul>	
Frequency translation is optional within the specified frequency range.	<ul><li>Standard: 8mA (default)</li><li>High: 16mA</li></ul>	<ul> <li>CSEL – input</li> <li>CLK1, 2 – output</li> </ul>	

#### > LAYOUT RECOMMENDATIONS

The following guidelines are designed to assist the user to create a performance-optimized PCB design.

#### Signal Integrity and Termination Considerations

Keep traces short for good signal integrity.

Trace = Inductor. With a capacitive load this causes ringing.

Long trace = Transmission line. Without proper termination, this will cause reflections that also look like ringing.

Design long traces (greater than 1 inch) as "striplines" or "microstrips" with defined impedance.

Match the trace at one side to avoid reflections bouncing back and forth.

#### **Decoupling and Power Supply Considerations**

Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply.

Multiple VDD pins should be decoupled separately for best performance.

The addition of a ferrite bead in series with VDD can help prevent noise from other board sources.

The value of the decoupling capacitor is frequency-dependent. Typical values to use are  $0.1\mu$ F for designs using frequencies >50MHz and  $0.01\mu$ F for designs using frequencies >50MHz.

Typical CMOS Termination Place series resistor as close to CMOS output as possible.

CMOS OUTPUT BUFFER (TYPICAL BUFFER IMPEDANCE 20Ω)	50Ω LINE	TO CMOS INPUT
		$\rightarrow$
SERIES RESI	STOR	
USE VALUE TO MAT	CH OUTPUT	
BUFFER IMPEDANCE	TO 50Ω TRACE.	
TYPICAL VALU	E 30Ω.	



# Low Power MEMS Jitter Attenuator

# ABMJB-902

#### PERIOD JITTER HISTOGRAM



10MHz input clock with bad period jitter - 460pcs peak-to-peak period jitter

**ESD** Sensitive

(Pb) RoHS/RoHS II Compliant

10MHz output clock from Jitter Attenuator - 75pcs peak-to-peak period jitter

Acquisition is stop 40.0 GSa/s 83 pts 12GHz Standard BW 3) On 4) On 1) 0n ⊽ ~ ∿ ∿ <sup>1</sup> 100.0000 ns •••\* H 200 ps/ **4** 0 ► T 2 mV stogram Color Grade Scales 99.99771462 10.6371 ps edian Mode 99.99666667 ns Hits 100.00111 ns Peak 10.81 khits 960 hits Y Scale 240 hits/ Y Offset 0 hits Std Dev 75.56 ps u±1σ p-p Min





2 Faraday, Suite# B | Irvine | CA 92618 **Revised: 03.09.15** Ph. 949.546.8000 | Fax. 949.546.8001 Visit www.abracon.com for Terms and Conditions of Sale



2.9 x 2.8 x 1.45 mm SOT23-6L

# Low Power MEMS Jitter Attenuator

## ABMJB-902





2.9 x 2.8 x 1.45 mm SOT23-6L

### **FIXING EXTREME JITTER IN 10MHZ IEEE1588 GPIO CLOCKS**

An IEEE1588 system can manufacture a 10MHz clock from 8ns pulses, but this creates extreme period jitter of about 24ns peak-to-peak in this case. The Jitter Attenuator cleans that up to 100ps peak-to-peak, allowing the clock to be used in more jitter-sensitive applications.

10MHZ clock from IEEE1588:



Jitter Attenuator Output Clock:







2 Faraday, Suite# B | Irvine | CA 92618 **Revised: 03.09.15** Ph. 949.546.8000 | Fax. 949.546.8001 Visit www.abracon.com for Terms and Conditions of Sale

ESD Sensitive

(Pb) RoHS/RoHS II Compliant



2.9 x 2.8 x 1.45 mm SOT23-6L

### **REFLOW PROFILE:**



## **▷** TAPE & REEL:



**ATTENTION:** Abracon Corporation's products are COTS – Commercial-Off-The-Shelf products; suitable for Commercial, Industrial and, where designated, Automotive Applications. Abracon's products are not specifically designed for Military, Aviation, Aerospace, Life-dependant Medical applications or any application requiring high reliability where component failure could result in loss of life and/or property. For applications requiring high reliability and/or presenting an extreme operating environment, written consent and authorization from Abracon Corporation is required. Please contact Abracon Corporation for more information.





2 Faraday, Suite# B | Irvine | CA 92618 **Revised: 03.09.15** Ph. 949.546.8000 | Fax. 949.546.8001 Visit www.abracon.com for Terms and Conditions of Sale