*Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor*

# Not for New Design

These parts are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: June 5, 2017

**Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, use ACS723.*

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

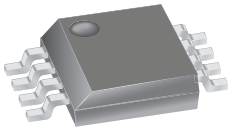
# *Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor*

## Features and Benefits

- Low-noise analog signal path
- Device bandwidth is set via the new FILTER pin
- 5 µs output rise time in response to step input current
- 80 kHz bandwidth
- Total output error 1.5% at $T_A$ = 25°C
- Small footprint, low-profile SOIC8 package
- 1.2 mΩ internal conductor resistance
- 2.1 kVRMS minimum isolation voltage from pins 1-4 to pins 5-8
- 5.0 V, single supply operation
- 133 to 185 mV/A output sensitivity
- Output voltage proportional to DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis
- Ratiometric output from supply voltage

TÜV America
Certificate Number:
U8V 06 05 54214 010

## Package: 8 Lead SOIC (suffix LC)



Approximate Scale 1:1

## Description

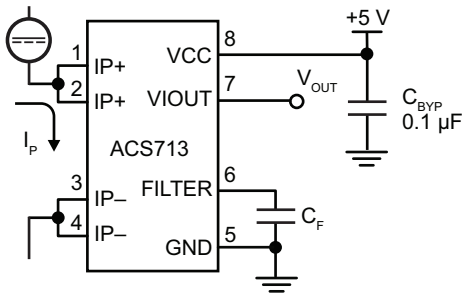
The Allegro™ ACS713 provides economical and precise solutions for DC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection. The device is not intended for automotive applications.

The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging.

The output of the device has a positive slope (>$V_{IOUT(Q)}$) when an increasing current flows through the primary copper conduction path (from pins 1 and 2, to pins 3 and 4), which is the path used for current sampling. The internal resistance of this conductive path is 1.2 mΩ typical, providing low power loss. The thickness of the copper conductor allows survival of

*Continued on the next page…*

## Typical Application




Application 1. The ACS713 outputs an analog signal, $V_{OUT}$, that varies linearly with the unidirectional DC primary sampled current, $I_P$, within the range specified. $C_F$ is recommended for noise management, with values that depend on the application.

## Description (continued)

the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 5 through 8). This allows the ACS713 to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The ACS713 is provided in a small, surface mount SOIC8 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

## Selection Guide

| Part Number | Packing* | $T_A$ (°C) | Optimized Range, $I_P$ (A) | Sensitivity, Sens (Typ) (mV/A) |
|---|---|---|---|---|
| ACS713ELCTR-20A-T | Tape and reel, 3000 pieces/reel | –40 to 85 | 0 to 20 | 185 |
| ACS713ELCTR-30A-T | Tape and reel, 3000 pieces/reel | –40 to 85 | 0 to 30 | 133 |

*Contact Allegro for additional packing options.

## Absolute Maximum Ratings

| Characteristic | Symbol | Notes | Rating | Units |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 8 | V |
| Reverse Supply Voltage | $V_{RCC}$ | | –0.1 | V |
| Output Voltage | $V_{IOUT}$ | | 8 | V |
| Reverse Output Voltage | $V_{RIOUT}$ | | –0.1 | V |
| Reinforced Isolation Voltage | $V_{ISO}$ | Pins 1-4 and 5-8; 60 Hz, 1 minute, $T_A$=25°C | 2100 | VAC |
| | | Maximum working voltage according to UL60950-1 | 184 | $V_{peak}$ |
| Basic Isolation Voltage | $V_{ISO(bsc)}$ | Pins 1-4 and 5-8; 60 Hz, 1 minute, $T_A$=25°C | 1500 | VAC |
| | | Maximum working voltage according to UL60950-1 | 354 | $V_{peak}$ |
| Output Current Source | $I_{OUT(Source)}$ | | 3 | mA |
| Output Current Sink | $I_{OUT(Sink)}$ | | 10 | mA |
| Overcurrent Transient Tolerance | $I_P$ | 1 pulse, 100 ms | 100 | A |
| Nominal Operating Ambient Temperature | $T_A$ | Range E | –40 to 85 | ºC |
| Maximum Junction Temperature | $T_J$(max) | | 165 | ºC |
| Storage Temperature | $T_{stg}$ | | –65 to 170 | ºC |

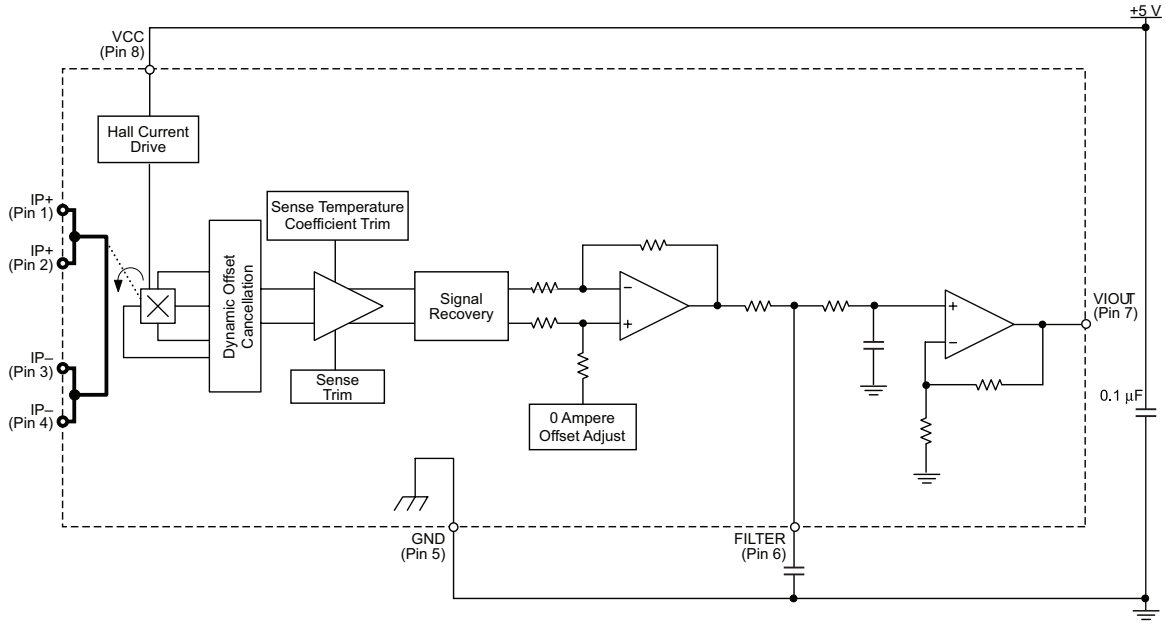
## Isolation Characteristics

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Dielectric Strength Test Voltage* | $V_{ISO}$ | Agency type-tested for 60 seconds per UL standard 60950-1, 1st Edition | 2100 | VAC |
| Working Voltage for Basic Isolation | $V_{WFSI}$ | For basic (single) isolation per UL standard 60950-1, 1st Edition | 354 | VDC or $V_{pk}$ |
| Working Voltage for Reinforced Isolation | $V_{WFRI}$ | For reinforced (double) isolation per UL standard 60950-1, 1st Edition | 184 | VDC or $V_{pk}$ |

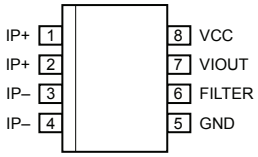
* Allegro does not conduct 60-second testing. It is done only during the UL certification process.

| Parameter | Specification |
|---|---|
| Fire and Electric Shock | CAN/CSA-C22.2 No. 60950-1-03<br>UL 60950-1:2003; EN 60950-1:2001 |

## Functional Block Diagram




## Pin-out Diagram




### Terminal List Table

| Number | Name | Description |
|---|---|---|
| 1 and 2 | IP+ | Input terminals for current being sampled; fused internally |
| 3 and 4 | IP– | Output terminals for current being sampled; fused internally |
| 5 | GND | Signal ground terminal |
| 6 | FILTER | Terminal for external capacitor that sets bandwidth |
| 7 | VIOUT | Analog output signal |
| 8 | VCC | Device power supply terminal |

## COMMON OPERATING CHARACTERISTICS[1] over full range of $T_A$, and $V_{CC}$ = 5 V, unless otherwise specified

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | | |
| Supply Voltage | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| Supply Current | $I_{CC}$ | $V_{CC}$ = 5.0 V, output open | – | 10 | 13 | mA |
| Output Capacitance Load | $C_{LOAD}$ | VIOUT to GND | – | – | 10 | nF |
| Output Resistive Load | $R_{LOAD}$ | VIOUT to GND | 4.7 | – | – | kΩ |
| Primary Conductor Resistance | $R_{PRIMARY}$ | $T_A$ = 25°C | – | 1.2 | – | mΩ |
| Rise Time | $t_r$ | $I_P = I_P$(max), $T_A$ = 25°C, $C_{OUT}$ = 10 nF | – | 3.5 | – | µs |
| Frequency Bandwidth | f | –3 dB, $T_A$ = 25°C; $I_P$ is 10 A peak-to-peak | – | 80 | – | kHz |
| Nonlinearity | $E_{LIN}$ | Over full range of $I_P$, $I_P$ applied for 5 ms | – | ±1.5 | – | % |
| Zero Current Output Voltage | $V_{IOUT(Q)}$ | Unidirectional; $I_P$ = 0 A, $T_A$ = 25°C | – | $V_{CC}$ × 0.1 | – | V |
| Power-On Time | $t_{PO}$ | Output reaches 90% of steady-state level, no capacitor on FILTER pin; $T_J$ = 25; 20 A present on leadframe | – | 35 | – | µs |
| Magnetic Coupling[2] | | | – | 12 | – | G/A |
| Internal Filter Resistance[3] | $R_{F(INT)}$ | | | 1.7 | | kΩ |

[1]Device may be operated at higher primary current levels, $I_P$, and ambient, $T_A$, and internal leadframe temperatures, $T_A$, provided that the Maximum Junction Temperature, $T_J$(max), is not exceeded.

[2]1G = 0.1 mT.

[3]$R_{F(INT)}$ forms an RC circuit via the FILTER pin.

## COMMON THERMAL CHARACTERISTICS[1]

| | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Internal Leadframe Temperature | $T_A$ | E range | –40 | – | 85 | °C |
| | | | | | Value | Units |
| Junction-to-Lead Thermal Resistance[2] | $R_{\theta JL}$ | Mounted on the Allegro ASEK 713 evaluation board | | | 5 | °C/W |
| Junction-to-Ambient Thermal Resistance[2,3] | $R_{\theta JA}$ | Mounted on the Allegro 85-0322 evaluation board, includes the power consumed by the board | | | 23 | °C/W |

[1]Additional thermal information is available on the Allegro website.

[2]The Allegro evaluation board has 1500 mm$^2$ of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website. Further information about board design and thermal performance also can be found in the Applications Information section of this datasheet.

[3]$R_{\theta JA}$ values shown in this table are typical values, measured on the Allegro evaluation board. The actual thermal performance depends on the actual application board design, the airflow in the application, and thermal interactions between the device and surrounding components through the PCB and the ambient air. To improve thermal performance, see our applications material on the Allegro website.

**x20A PERFORMANCE CHARACTERISTICS** $T_A$ = –40°C to 85°C[1]; $V_{CC}$ = 5 V, unless otherwise specified

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Optimized Accuracy Range | $I_P$ | | 0 | – | 20 | A |
| Sensitivity | Sens | Over full range of $I_P$, $T_A$ = 25°C | 178 | 185 | 190 | mV/A |
| Noise | $V_{NOISE(PP)}$ | Peak-to-peak, $T_A$ = 25°C, 2 kHz external filter, 185 mV/A programmed Sensitivity, $C_F$ = 47 nF, $C_{OUT}$ = 10 nF, 2 kHz bandwidth | – | 21 | – | mV |
| Zero Current Output Slope | $\Delta V_{OUT(Q)}$ | $T_A$ = –40°C to 25°C | – | 0.08 | – | mV/°C |
| | | $T_A$ = 25°C to 150°C | – | 0.16 | – | mV/°C |
| Sensitivity Slope | ΔSens | $T_A$ = –40°C to 25°C | – | 0.035 | – | mV/A/°C |
| | | $T_A$ = 25°C to 150°C | – | 0.019 | – | mV/A/°C |
| Total Output Error[2] | $E_{TOT}$ | $I_P$ = 20 A, $I_P$ applied for 5 ms; $T_A$ = 25°C | – | ±1.5 | – | % |

[1]Device may be operated at higher primary current levels, $I_P$, and ambient temperatures, $T_A$, provided that the Maximum Junction Temperature, $T_J$(max), is not exceeded.
[2]Percentage of $I_P$, with $I_P$ = 20 A. Output filtered.

**x30A PERFORMANCE CHARACTERISTICS** $T_A$ = –40°C to 85°C[1]; $V_{CC}$ = 5 V, unless otherwise specified

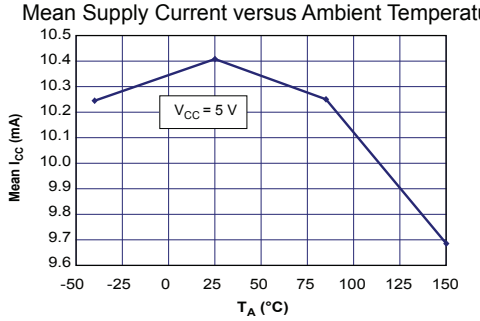
| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Optimized Accuracy Range | $I_P$ | | 0 | – | 30 | A |
| Sensitivity | Sens | Over full range of $I_P$, $T_A$ = 25°C | 129 | 133 | 137 | mV/A |
| Noise | $V_{NOISE(PP)}$ | Peak-to-peak, $T_A$ = 25°C, 2 kHz external filter, 133 mV/A programmed Sensitivity, $C_F$ = 47 nF, $C_{OUT}$ = 10 nF, 2 kHz bandwidth | – | 15 | – | mV |
| Zero Current Output Slope | $\Delta V_{OUT(Q)}$ | $T_A$ = –40°C to 25°C | – | 0.06 | – | mV/°C |
| | | $T_A$ = 25°C to 150°C | – | 0.1 | – | mV/°C |
| Sensitivity Slope | ΔSens | $T_A$ = –40°C to 25°C | – | 0.007 | – | mV/A/°C |
| | | $T_A$ = 25°C to 150°C | – | –0.025 | – | mV/A/°C |
| Total Output Error[2] | $E_{TOT}$ | $I_P$ = 30 A, $I_P$ applied for 5 ms; $T_A$ = 25°C | – | ±1.5 | – | % |

[1]Device may be operated at higher primary current levels, $I_P$, and ambient temperatures, $T_A$, provided that the Maximum Junction Temperature, $T_J$(max), is not exceeded.
[2]Percentage of $I_P$, with $I_P$ = 30 A. Output filtered.

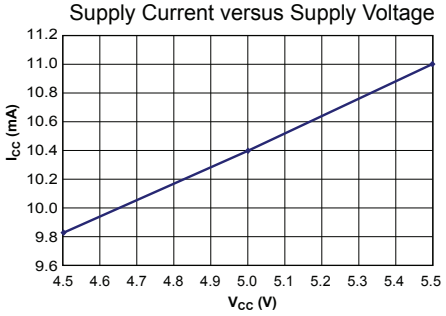
## Characteristic Performance

$I_P$ = 20 A, unless otherwise specified

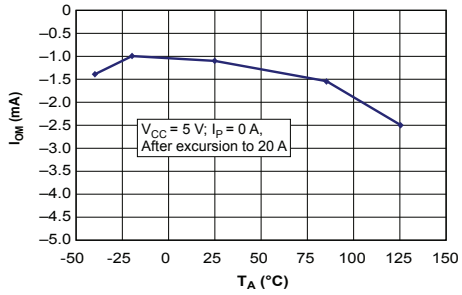
Mean Supply Current versus Ambient Temperature



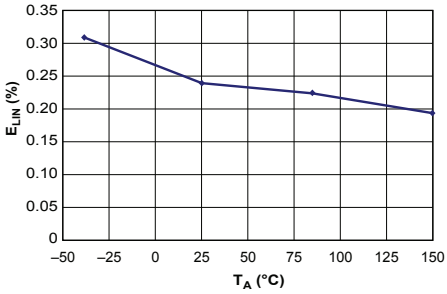

Supply Current versus Supply Voltage



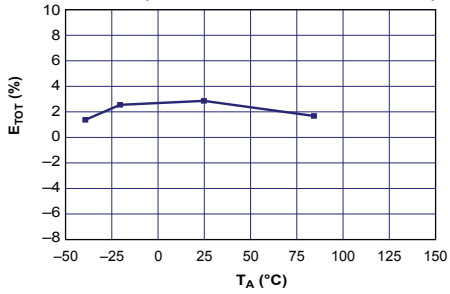

Magnetic Offset versus Ambient Temperature



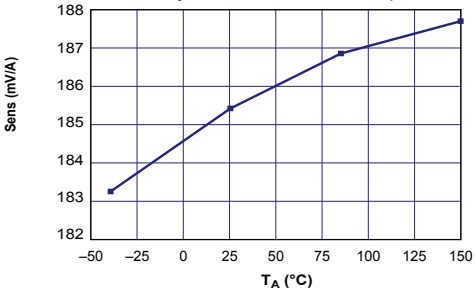

Nonlinearity versus Ambient Temperature



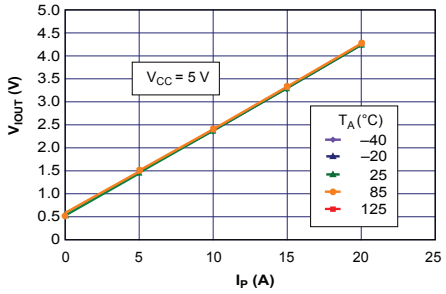

Mean Total Output Error versus Ambient Temperature



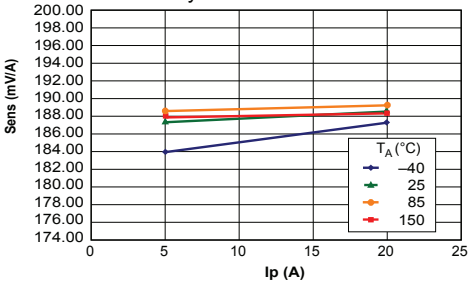

Sensitivity versus Ambient Temperature



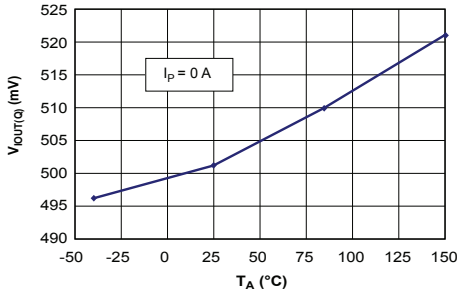

Output Voltage versus Sensed Current



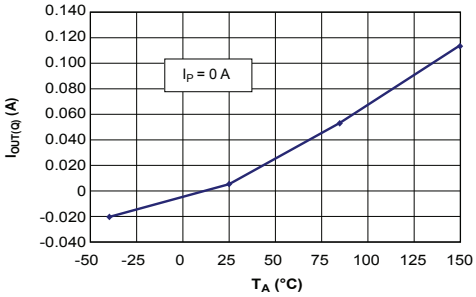

Sensitivity versus Sensed Current




0 A Output Voltage versus Ambient Temperature



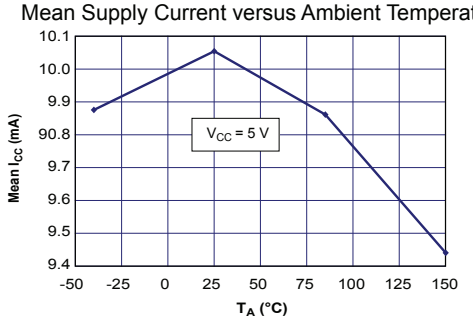

0 A Output Voltage Current versus Ambient Temperature



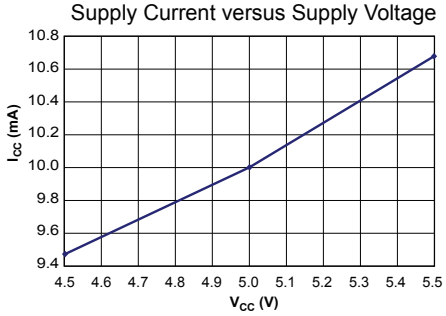
## Characteristic Performance

$I_P$ = 30 A, unless otherwise specified

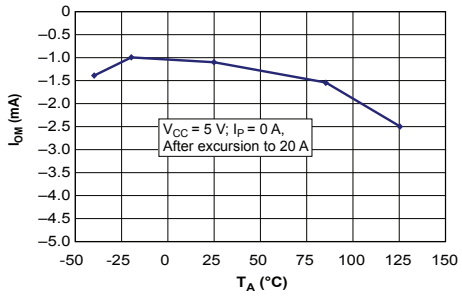
Mean Supply Current versus Ambient Temperature



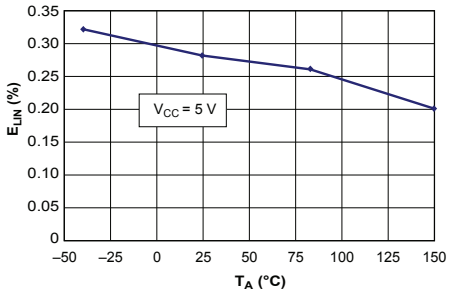

Supply Current versus Supply Voltage



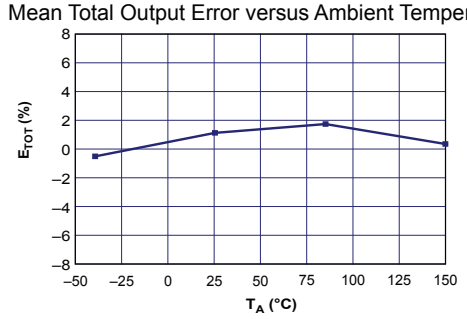

Magnetic Offset versus Ambient Temperature



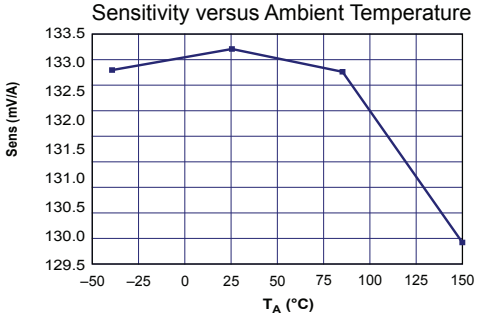

Nonlinearity versus Ambient Temperature



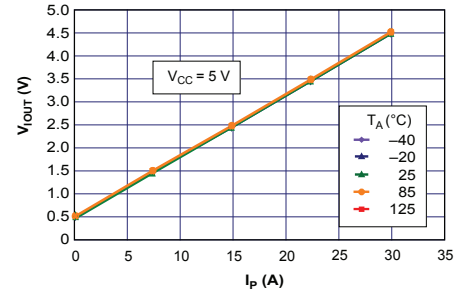

Mean Total Output Error versus Ambient Temperature



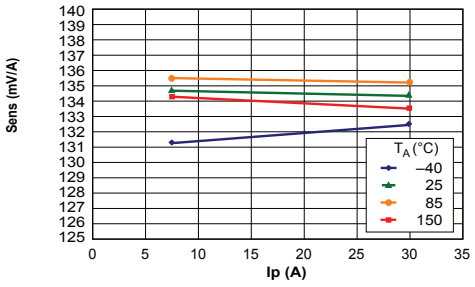

Sensitivity versus Ambient Temperature



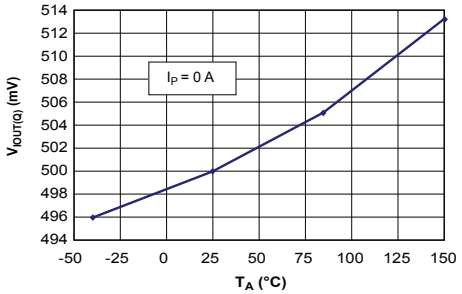

Output Voltage versus Sensed Current



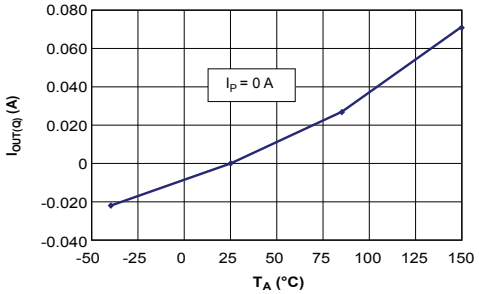

Sensitivity versus Sensed Current




0 A Output Voltage versus Ambient Temperature




0 A Output Voltage Current versus Ambient Temperature



## Definitions of Accuracy Characteristics

**Sensitivity (Sens).** The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

**Noise ($V_{NOISE}$).** The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

**Linearity ($E_{LIN}$).** The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{(V_{\text{IOUT\_full-scale amperes}}-V_{\text{IOUT(Q)}})}{2\,(V_{\text{IOUT\_half-scale amperes}}-V_{\text{IOUT(Q)}})}\right]\right\}$$

where $V_{\text{IOUT\_full-scale amperes}}$ = the output voltage (V) when the sampled current approximates full-scale $\pm I_P$.

**Quiescent output voltage ($V_{IOUT(Q)}$).** The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC} \times 0.1$. Thus, $V_{CC}$ = 5 V translates into $V_{IOUT(Q)}$ = 0.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

**Electrical offset voltage ($V_{OE}$).** The deviation of the device output from its ideal quiescent value of $V_{CC} \times 0.1$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

**Accuracy ($E_{TOT}$).** The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

**Ratiometry**. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC} \times 0.1$ ) and sensitivity, Sens, are proportional to its supply voltage, $V_{CC}$. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%).

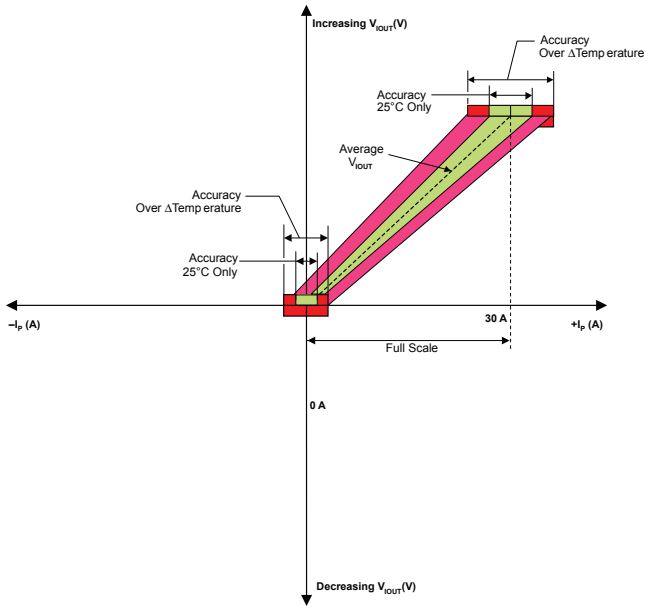
$$100\left(\frac{V_{\text{IOUT(Q)VCC}}/V_{\text{IOUT(Q)5V}}}{V_{CC}/5\text{ V}}\right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

$$100\left(\frac{Sens_{VCC}/\,Sens_{5V}}{V_{CC}/5\text{ V}}\right)$$

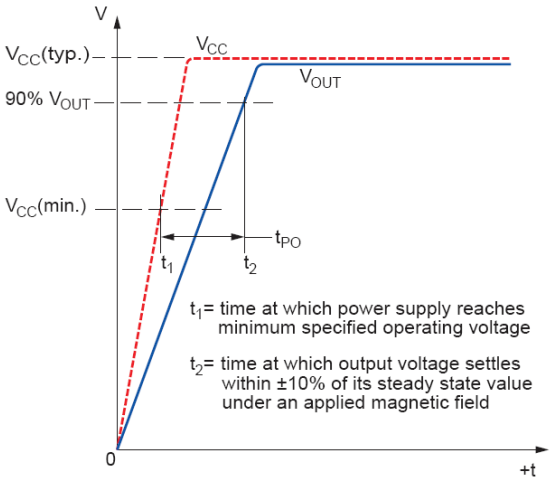
### Output Voltage versus Sampled Current

Accuracy at 0 A and at Full-Scale Current

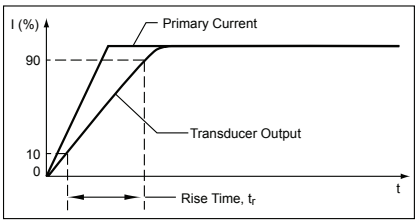


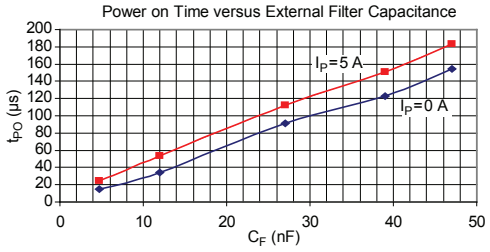
## Definitions of Dynamic Response Characteristics

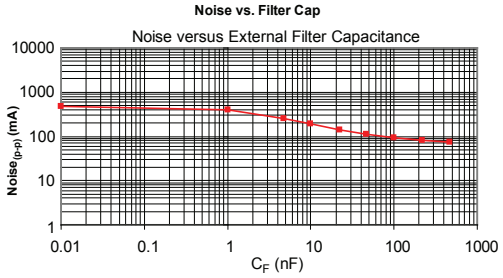
**Power-On Time ($t_{PO}$).** When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, $t_{PO}$ , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, $V_{CC}$(min), as shown in the chart at right.

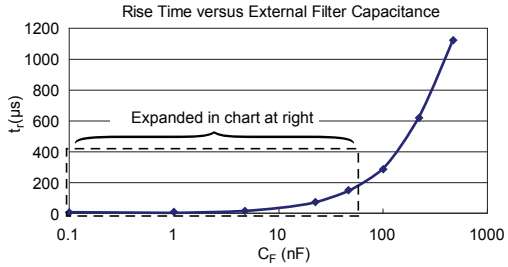



**Rise time ($t_r$).** The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ dB) = 0.35 / t_r$. Both $t_r$ and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

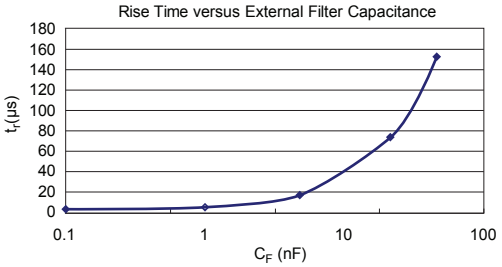


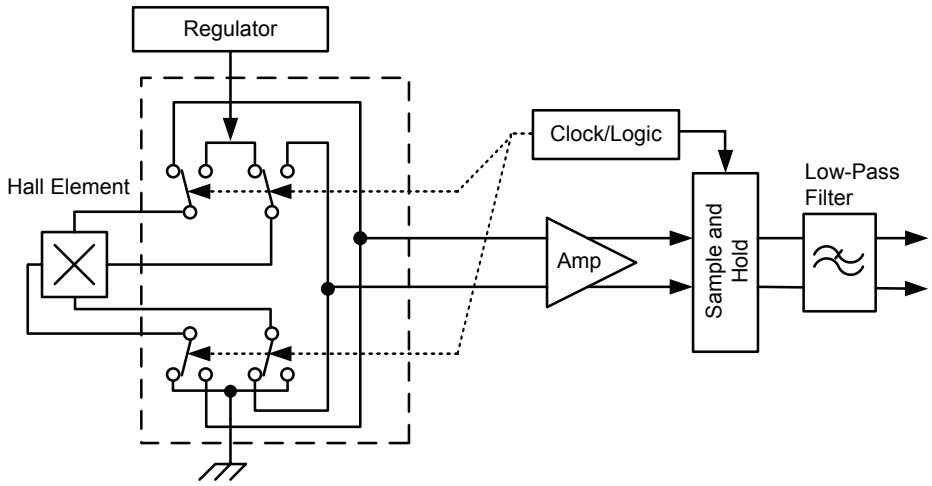

| $C_F$ (nF) | $t_r$ (µs) |
|---|---|
| Open | 3.5 |
| 1 | 5.8 |
| 4.7 | 17.5 |
| 22 | 73.5 |
| 47 | 88.2 |
| 100 | 291.3 |
| 220 | 623 |
| 470 | 1120 |



## Chopper Stabilization Technique

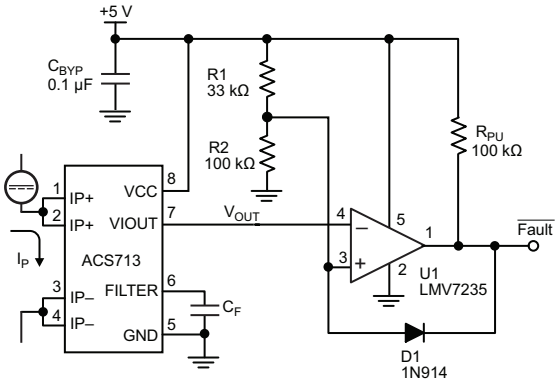
Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro has a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.

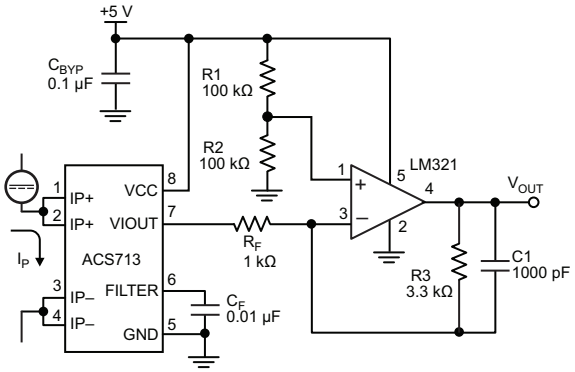



Concept of Chopper Stabilization Technique

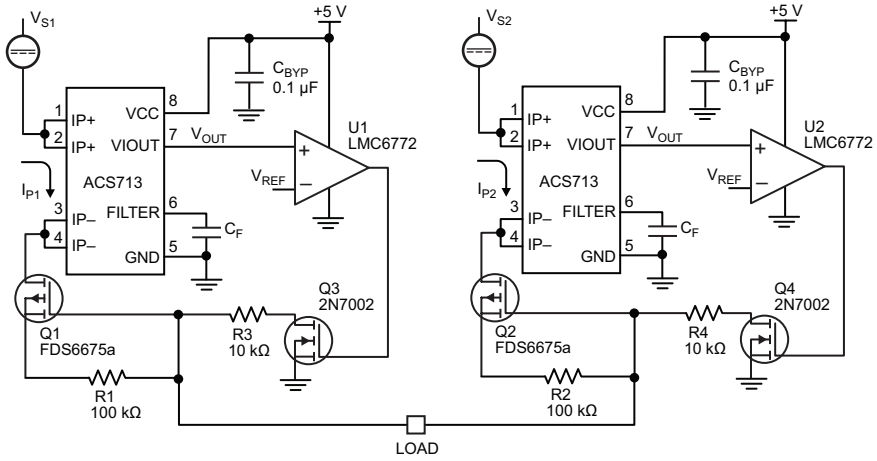
## Typical Applications




Application 2. 10 A Overcurrent Fault Latch. Fault threshold set by R1 and R2. This circuit latches an overcurrent fault and holds it until the 5 V rail is powered down.




Application 3. This configuration increases gain to 610 mV/A (tested using the ACS712ELC-05A).




Application 4. Control circuit for MOSFET ORing.

### Improving Sensing System Accuracy Using the FILTER Pin

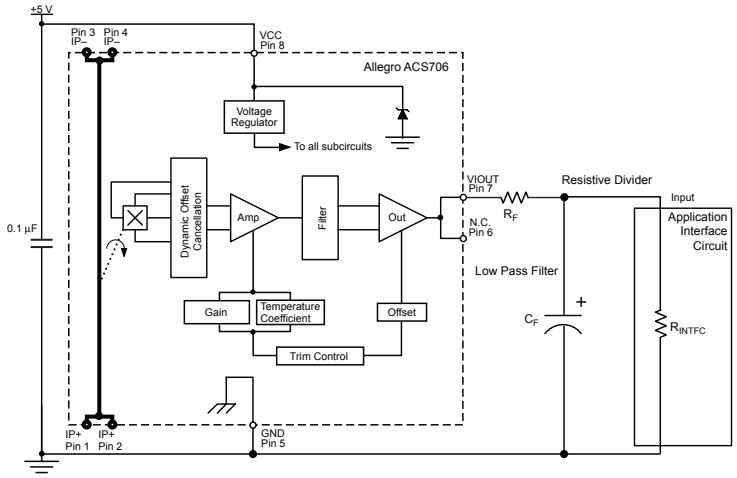
In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the device. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation, $\Delta V_{ATT}$, is a result of the resistive divider effect between the resistance of the external filter, $R_F$ (see Application 5), and the input impedance and resistance of the customer interface circuit, $R_{INTFC}$. The transfer function of this resistive divider is given by:

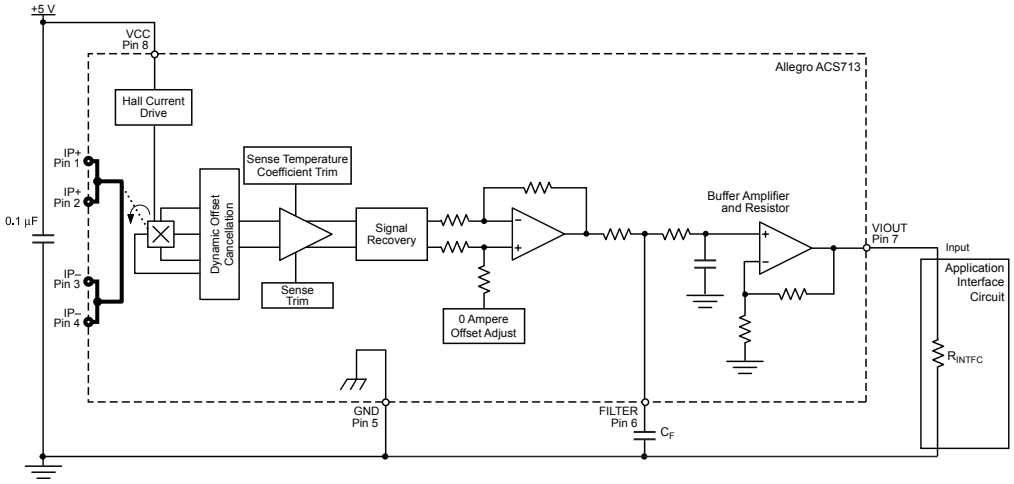
$$\Delta V_{ATT} = V_{IOUT}\left(\frac{R_{INTFC}}{R_F + R_{INTFC}}\right) .$$

Even if $R_F$ and $R_{INTFC}$ are designed to match, the two individual resistance values will most likely drift by different amounts over temperature. Therefore, signal attenuation will vary as a function of temperature. Note that, in many cases, the input impedance, $R_{INTFC}$, of a typical analog-to-digital converter (ADC) can be as low as 10 kΩ.

The ACS713 contains an internal resistor, a FILTER pin connection to the printed circuit board, and an internal buffer amplifier. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor, $C_F$ (see Application 6) from the FILTER pin to ground. The buffer amplifier inside of the ACS713 (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in the equation for $\Delta V_{ATT}$. Therefore, the ACS713 device is ideal for use in high-accuracy applications that cannot afford the signal attenuation associated with the use of an external RC low-pass filter.

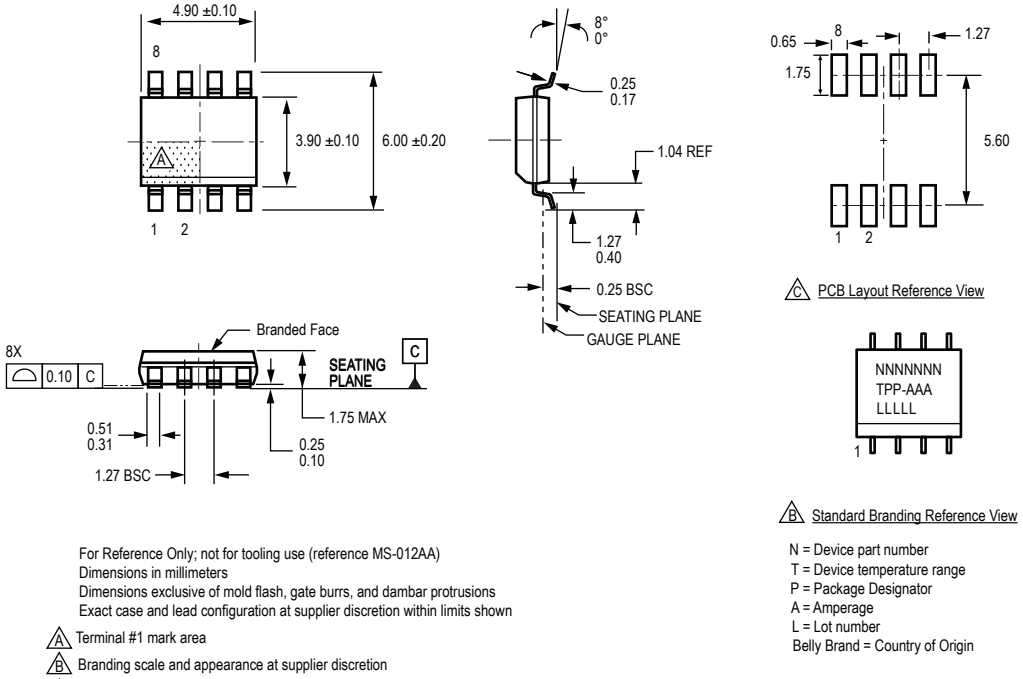



Application 5. When a low pass filter is constructed externally to a standard Hall effect device, a resistive divider may exist between the filter resistor, $R_F$, and the resistance of the customer interface circuit, $R_{INTFC}$. This resistive divider will cause excessive attenuation, as given by the transfer function for $\Delta V_{ATT}$.




Application 6. Using the FILTER pin provided on the ACS713 eliminates the attenuation effects of the resistor divider between $R_F$ and $R_{INTFC}$, shown in Application 5.

## Package LC, 8-pin SOIC




For Reference Only; not for tooling use (reference MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

N = Device part number
T = Device temperature range
P = Package Designator
A = Amperage
L = Lot number
Belly Brand = Country of Origin

## Revision History

| Revision | Revision Date | Description of Revision |
|---|---|---|
| 12 | November 16, 2012 | Update rise time and isolation, $I_{OUT}$ reference data, patents |
| 13 | June 5, 2017 | Updated product status |



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