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Devices Connected/Referenced	
AD8606	Precision, Low Noise, Dual CMOS, Rail-to-Rail Input/Output Op Amp
AD7091R	1 MSPS, Ultralow Power, 12-Bit ADC
ADuM5401	Quad-Channel, 2.5 kV Isolators with Integrated DC-to-DC Converter

12-Bit, 300 kSPS, Single-Supply, Fully Isolated, Data Acquisition System for ±10 V Inputs

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN0335 Circuit Evaluation Board (EVAL-CN0335-PMDZ)
SDP/PMD Interposer Board (SDP-PMD-IB1Z)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a completely isolated 12-bit, 300 kSPS data acquisition system utilizing only three active devices.

The system processes ±10 V input signals using a single 3.3 V supply. The total error after room temperature calibration is less than ±0.1% FSR over a ±10°C temperature change, making it ideal for a wide variety of industrial measurements.

The small footprint of the circuit makes this combination an industry-leading solution for data acquisition systems where the accuracy, speed, cost, and size play a critical role. Both data and power are isolated, thereby making the circuit robust to high voltages and also ground-loop interference often encountered in harsh industrial environments.

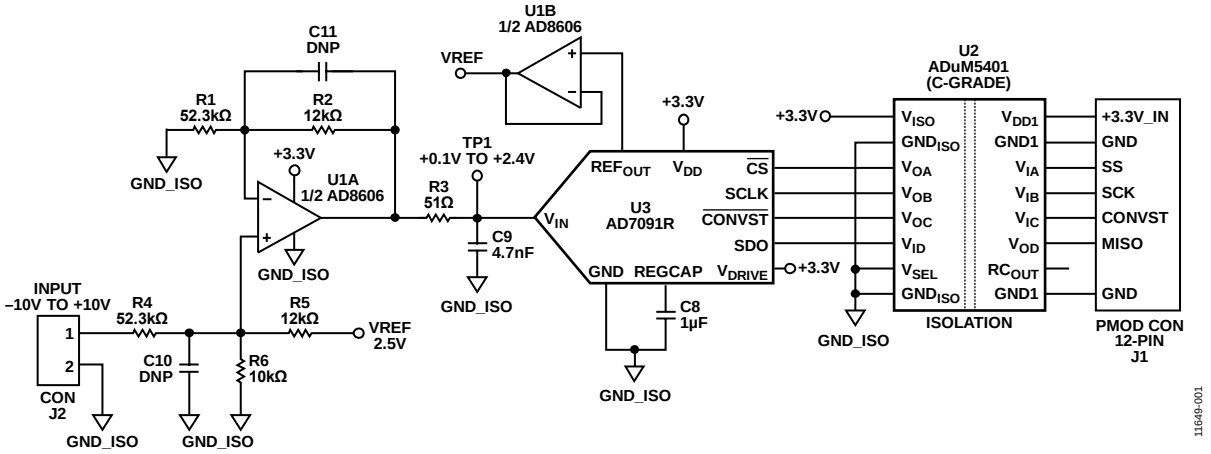

Figure 1. ±10 V Single Supply Data Acquisition System with Isolation (All Connections and Decoupling Not Shown)

Rev. A

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CIRCUIT DESCRIPTION

The circuit consists of an input signal conditioning stage, an ADC stage, and an output isolation stage. The ±10 V input signal is level shifted and attenuated by the U1A op amp that is one-half of the dual AD8606. The output of the op amp is 0.1 V to 2.4 V, which matches the input range of the ADC (0 V to 2.5 V) with 100 mV headroom to maintain linearity. The buffered voltage reference (V_{REF} =2.5 V) from the ADC is used to generate the required offset. Resistor values can be modified to accommodate other popular input ranges as described later in this circuit note.

The circuit design allows single supply operation. The minimum output voltage specification of the AD8606 is 50 mV for a 2.7 V power supply and 290 mV for 5 V power supply with 10 mA load current, over the temperature range of −40°C to +125°C. A minimum output voltage of 45 mV to 60 mV is a conservative estimate for a 3.3 V power supply, a load current less than 1 mA, and a narrower temperature range.

Considering the tolerances of the parts, the minimum output voltage (low limit of the range) is set to 100 mV to allow a safety margin. The upper limit of the output range is set to 2.4 V in order to give 100 mV headroom for the positive swing at the ADC input. Therefore, the nominal output voltage range of the input op amp is 0.1 V to 2.4 V.

The second half of the AD8606 (U1B) is used to buffer the internal 2.5 V voltage reference of the AD7091R (U3) ADC.

The AD8606 is chosen for this application because of its low offset voltage (65 µV maximum), low bias current (1 pA maximum) and low noise (12 nV/√Hz maximum). Power dissipation is only 9.2 mW on a 3.3 V supply.

A single-pole RC filter (R3/C9) follows the op amp output stage to reduce the out-of-band noise. The cutoff frequency of the RC filter is set to 664 kHz. An optional second order filter (R4, C10, and R1, R2, C11) can be added to reduce the filter cutoff frequency even further in case of low frequency industrial noise. In such case, the sampling rate of the AD7091R can be reduced because of the lower signal bandwidth.

The AD7091R 12-bit 1 MSPS SAR ADC is chosen because of its ultralow power 349 µA at 3.3 V (1.2 mW) which is significantly lower than any competitive ADC currently available in the market. The AD7091R also contains an internal 2.5 V reference with ±4.5 ppm/°C typical drift. The input bandwidth is 7.5 MHz, and the high speed serial interface is SPI compatible. The AD7091R is available in a small footprint 10-lead MSOP.

The total power dissipation of the circuit (excluding the ADuM5401 isolator) is approximately 10.4 mW when operating on a 3.3 V supply.

Galvanic isolation is provided by the ADuM5401 (C-Grade) quad channel digital isolator. In addition to the isolated output data, the ADuM5401 also provides isolated 3.3 V for the circuit. The ADuM5401 is not required for normal circuit operation unless isolation is needed. The ADuM5401 quad-channel, 2.5 kV isolators with integrated dc-to-dc converter, is available in a small 16-lead SOIC. Power dissipation of the ADuM5401 with a 7 MHz clock is approximately 140 mW.

The AD7091R requires a 50 MHz serial clock (SCLK) to achieve a 1 MSPS sampling rate. However, the ADuM5401 (C-grade) isolator has a maximum data rate of 25 Mbps that corresponds to a maximum serial clock frequency of 12.5 MHz. In addition, the SPI port requires that the trailing edge of the SCLK clock the output data into the processor, therefore the total round-trip propagation delay through the ADuM5401 (120 ns maximum) limits the upper clock frequency to 1/120 ns = 8.3 MHz.

Even though the AD7091R is a 12-bit ADC, the serial data is formatted into a 16-bit word to be compatible with the processor serial port requirements. The sampling period, T_S, therefore consists of the AD7091R 650 ns conversion time plus 58 ns (extra time required from data sheet, t_1 delay + t_{QUIET} delay) plus 16 clock cycles for the SPI interface data transfer.

$$T_S = 650 \text{ ns} + 58 \text{ ns} + 16 \times 120 \text{ ns} = 2628 \text{ ns}$$

$$f_S = 1/T_S = 1/2628 \text{ ns} = 380 \text{ kSPS}$$

In order to provide a safety margin, a maximum SCLK of 7 MHz and a maximum sampling rate of 300 kSPS is recommended. The digital SPI interface can be connected to the microprocessor evaluation board using the 12-pin Pmod-compatible connector (Digilent Pmod Specifications).

Circuit Design

The circuit shown in Figure 2 attenuates and level shifts the −10 V to +10 V input signal to the ADC input range of 0.1 V to 2.4 V.

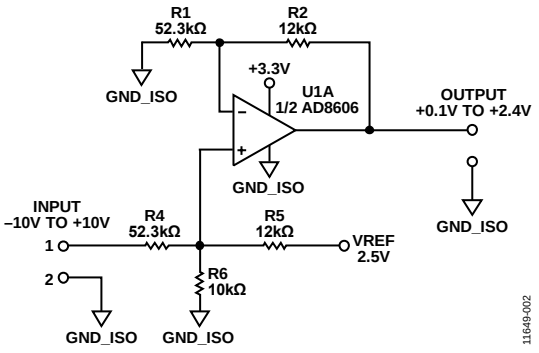

Figure 2. Input Voltage Signal Conditioning Circuit

The transfer function is obtained from the superposition principle:

$$V_{OUT} = V_{IN} \frac{R5 \| R6}{R4 + R5 \| R6}\left(1 + \frac{R2}{R1}\right) + V_{REF} \frac{R4 \| R6}{R5 + R4 \| R6}\left(1 + \frac{R2}{R1}\right) =$$

$$= V_{IN} \frac{R}{R4 + R} k + V_{REF} \frac{R0}{R5 + R0} k = V_{IN} GAIN + OFFSET \quad (1)$$

where:

$$R = R5 \| R6 = \frac{R5R6}{R5 + R6}, \quad R0 = R4 \| R6 = \frac{R4R6}{R4 + R6} \quad (2)$$

$$\text{and } k = \left(1 + \frac{R2}{R1}\right) \quad (3)$$

Calculation of the Gain, Output Offset, and the Resistor Values

For input voltage range ±10 V, the calculations are as follows.

The gain of the circuit is:

$$GAIN = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{2.4\text{ V} - 0.1\text{ V}}{+10\text{ V} - (-10\text{ V})} = \frac{2.3\text{ V}}{20\text{ V}} = 0.115 \quad (4)$$

and according to the transfer function:

$$GAIN = \frac{R5 \| R6}{R4 + R5 \| R6}\left(1 + \frac{R2}{R1}\right) = \frac{R}{R4 + R} k \quad (5)$$

The output offset of the circuit is:

$$OFFSET = V_{OUT}\ (V_{IN} = 0\text{ V}) = 0.1\text{ V} + \frac{2.4\text{ V} - 0.1\text{ V}}{2} = 1.25\text{ V} \quad (6)$$

and according to the transfer function:

$$OFFSET = V_{REF} \frac{R4 \| R6}{R5 + R4 \| R6}\left(1 + \frac{R2}{R1}\right) = V_{REF} \frac{R0}{R5 + R0} k \quad (7)$$

From Equation 4, for k =1.23 (this value can vary, depending on the value of the standard value resistors R1 and R2), the ratio R4/R can be calculated:

$$R4 = 9.696\, R \quad (8)$$

From Equation 7, for V_{REF} = 2.5V and k =1.23 the ratio R5/R0 can be calculated:

$$R5 = 1.46\, R0 \quad (9)$$

Using Equation 2 for the resistors R and R0, and the ratios in Equation 8 and Equation 9, the ratio R4/R6 can be calculated:

$$R4 = 5.346\, R6 \quad (10)$$

From Equation 8, Equation 9, and Equation 10, the resistors R4, R5, and R6 can be calculated. For example choosing R6 = 10 kΩ leads to R4 = 53.46 kΩ, and R5 =12.3 kΩ.

In the actual circuit the nearest available standard resistor values were chosen for R4 and R5. The values selected were R4 = 52.3 kΩ and R5 = 12 kΩ. Note that R1 = R4 and R2 = R5.

If these values are chosen carefully, the overall error due to substituting standard value resistors can be made less than a few percent. However, use Equation 1 to recalculate the U1A op amp output for ±10 V inputs to ensure that the required headroom is preserved.

The absolute accuracy in this type of circuit is primarily determined by the resistors, and therefore gain and offset calibration is required to remove the error due to standard value substitution and resistor tolerances.

Calculation of Resistor Values for Different Input Ranges

For input ranges other than ±10 V complete the following calculation steps.

Define the input span, the output span, and the offset:

$$\Delta V_{IN} = V_{IN\_MAX} - V_{IN\_MIN} \quad (11)$$

$$\Delta V_{OUT} = V_{IOUT\_MAX} - V_{OUT\_MIN} \quad (12)$$

$$Offset = \frac{\Delta V_{OUT}}{2} + V_{OUT\_MIN} \quad (13)$$

Calculate the gain:

$$GAIN = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \quad (14)$$

Calculate the offset:

$$Offset = \frac{\Delta V_{OUT}}{2} + V_{OUT\_MIN} \quad (15)$$

Choose the value for the parameter k:

$$k = \left(1 + \frac{R2}{R1}\right) \quad (16)$$

Calculate the ratio R4/R, using:

$$GAIN = \frac{R}{R4 + R} k \quad (17)$$

Calculate the ratio R5/R0, using:

$$Offset = V_{REF} \frac{R0}{R5 + R0} k \quad (18)$$

Replace R and R0 in Equation 17 and Equation 18 with the values defined in Equation 2, and solve both equations find the ratio R4/R6.

Choose a value for the resistor R6. Calculate R4 using the ratio of R4/R6. Knowing the values for R4 and R6, calculate R5 using Equation 2 and the R4/R6 ratio. Calculate R2 and R1 using Equation 16. It is reasonable to choose R1 = R4 and calculate R2.

Effect of Resistor Temperature Coefficients on Overall Error

Equation 1 shows that the output voltage is a function of five resistors: R1, R2, R4, R5, and R6. The sensitivity of the full-scale output voltage at TP1 to small changes in each of the five resistors was calculated using a simulation program. The input voltage to the circuit was +10 V. The individual sensitivities calculated were S_{R1} = 0.19, S_{R2} = 0.19, S_{R4} = 0.39, S_{R5} = 0.11, S_{R6} = 0.50. Assuming the individual temperature coefficients combine in a root-sum-square (rss) manner, then the overall full-scale drift using 100 ppm/°C resistors is approximately:

Full scale drift =

$=100\ ppm/°C\ \sqrt{(S_{R1}^2 + S_{R2}^2 + S_{R4}^2 + S_{R5}^2 + S_{R6}^2)}$

$=100\ ppm/°C\ \sqrt{(0.19^2 + 0.19^2 + 0.39^2 + 0.11^2 + 0.50^2)}$

$= 69\ ppm/°C$

The full scale drift of 69 ppm/°C corresponds to 0.0069% FSR/°C. Using 25 ppm/°C resistors reduces the drift error to 0.25 × 69 ppm/°C = 17 ppm/°C, or 0.0017% FSR/°C.

Effect of Active Component Temperature Coefficients on Overall Error

The dc offsets of the AD8606 op amps and the AD7091R ADC are eliminated by the calibration procedure.

The offset drift of the ADC AD7091R internal reference is 4.5 ppm/°C typical and 25 ppm/°C maximum.

The offset drift of the AD8606 op amp is 1µV/°C typical and 4.5µV/°C maximum.

The error due to the U1A input AD8606 is referenced to the 2.3 V output range and is therefore 2 ppm/°C. The error due to the U1B reference buffer is referenced to 2.5 V and is also approximately 2 ppm/°C.

The total drift error is summarized in Table 1. These errors do not include the ±1 LSB integral nonlinearity error of the AD7091R.

Note that resistor drift is the largest contributor to total drift if 50 ppm/°C or 100 ppm/°C resistors are used, and the drift due to active components can be neglected.

Table 1. Error Due to Temperature Drift

Error Source	Total Error
Resistors (1%, 100 ppm/°C)	±0.0069% FSR/°C
AD7091R ($\Delta V_{VREF}/\Delta T$ = 25 ppm/°C)	±0.0025% FSR/°C
AD8606, U1A ($\Delta V_{OS}/\Delta T$= 4.5 µV/°C), 2 ppm/°C, Referenced to 2.3 V	±0.0002% FSR/°C
AD8606, U1B ($\Delta V_{OS}/\Delta T$= 4.5 µV/°C), 2 ppm/°C, Referenced to 2.5 V	±0.0002% FSR/°C
Total FSR Error Temperature Coefficient (100 ppm/°C Resistors)	±0.0098% FSR/°C
Total % FSR Error for ΔT=±10°C (100 ppm/°C Resistors)	±0.098% FSR
Total % FSR Error for ΔT=±10°C (25 ppm/°C Resistors)	±0.046% FSR

Test Data Before and After Two-Point Calibration

To perform the two-point calibration, −10 V is first applied to the input, and the ADC output code is recorded as Code_1. Then +10 V is applied to the input, and the ADC output code is recorded as Code_2. The gain factor is calculated by

$$GF = \frac{20\ V}{Code\_2 - Code\_1}$$

The input voltage can now be calculated corresponding to any output code, Code_x, using the equation:

$$V_{IN} = -10\ V + GF\,(Code\_x - Code\_1).$$

The error before calibration is obtained by comparing the ideal transfer function calculated using the nominal values of the components, and real circuit transfer function without calibration. The tested circuits have been built with resistors having ±1% tolerance. The test results do not include temperature changes.

The graph in Figure 3 shows test results for percent error (FSR) before and after calibration at ambient temperature. As it is shown, the maximum error before calibration is about 0.23% FSR. After calibration, the error decreases to ±0.03% FSR, which approximately corresponds to 1 LSB error of the ADC.

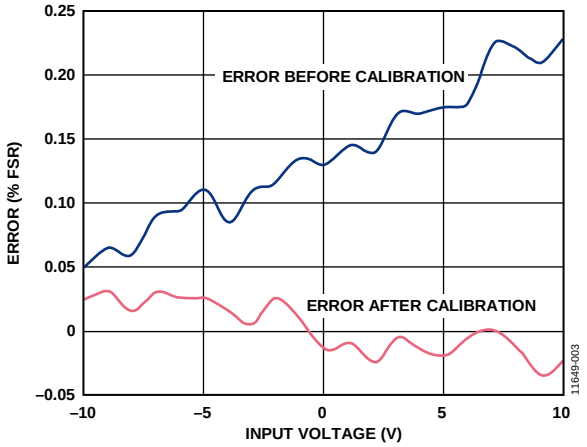

Figure 3. Circuit Test Error Before and After Room Temperature Calibration

PCB Layout Considerations

In any circuit where accuracy is crucial, it is important to consider the power supply and ground return layout on the board. The PCB should isolate the digital and analog sections as much as possible. The PCB for this system was constructed in a simple 2-layer stack up, but a 4-layer stack up gives better EMS. See the MT-031 Tutorial for more information on layout and grounding and the MT-101 Tutorial for information on decoupling techniques. Decouple the power supply to AD8606 with 10 µF and 0.1 µF capacitors to properly suppress noise and reduce ripple. Place the capacitors as close to the device as possible with the 0.1 µF capacitor having a low ESR value. Ceramic capacitors are advised for all high frequency decoupling. Power supply lines should have as large trace width as possible to provide a low impedance path and to reduce glitch effects on the supply line.

The ADuM5401 *iso*Power integrated dc-to-dc converter requires power supply bypassing at the input and output supply pins. Note that low ESR bypass capacitors are required between Pin 1 and Pin 2 and between Pin 15 and Pin 16, as close to the chip pads as possible. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for V_{DD1} and V_{ISO}. The smaller capacitor must have a low ESR, for example, use of a ceramic capacitor is advised. The total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. Consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16, unless both common ground pins are connected together close to the package. For more information, see the ADuM5401 datasheet.

A complete documentation package including schematics, board layout, and bill of materials (BOM) can be found at www.analog.com/CN0335-DesignSupport.

High Voltage Capability

This PCB is designed in adherence with 2500 V basic insulation practices. High voltage testing beyond 2500 V is not recommended. Take appropriate care when using this evaluation board at high voltages, and do not rely on the PCB for safety functions because it has not been high potential tested (also known as hipot tested or dielectric withstanding voltage tested) or certified for safety.

COMMON VARIATIONS

The circuit is proven to work with good stability and accuracy with component values shown. Other precision op-amps and other ADCs can be used in this configuration to convert ±10V input voltage range to digital output and for other various applications for this circuit.

The circuit in Figure 1 can be designed for other than ±10 V input voltage ranges, following the equations given in the Circuit Design section. Table 2 shows the resistor calculations for some standard voltage ranges.

Table 2. Component Values for Standard Voltage Ranges

Range (V)	k	R4 (kΩ)	R5 (kΩ)	R6 (kΩ)
±5	1.2	40.87	18.8	20
±2	2	32.174	37	20
±1	4	40.87	94	20
0 to 1	4	14.435	830	20
0 to 2	2	14.087	405	20
0 to 2.5	2	22.609	520	20
0 to 5	2	65.217	750	20
0 to 10	1	63.478	365	20
0 to 24	1	90.174	216	10

In the cases, when the lower range is zero and the upper range is greater than the reference voltage the conversion does not need gain (k = 1), and the circuit can be simplified. An example is shown in Figure 4 for the input range 0 V to 10 V.

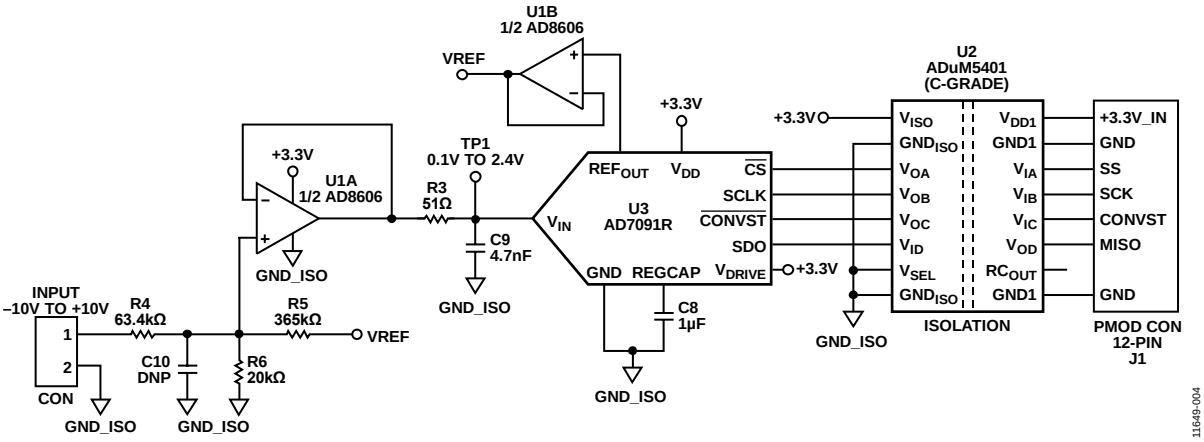

Figure 4. 0 V to 10 V Single Supply Analog to Digital Conversion with Isolation (All connections and Decoupling Not Shown)

The AD7091 is similar to the AD7091R, but without the voltage reference output, and the input range is equal to the power supply voltage. The AD7091 can be used with a 2.5 V ADR391 reference. The ADR391 does not require buffering, therefore a single AD8605 can be used in the circuit.

The ADR391 is a precision 2.5 V band gap voltage reference, featuring low power and high precision (9 ppm/°C of temperature drift) in a tiny TSOT package.

The AD8608 is a quad version of the AD8605 and can be used as a substitute for the AD8606, if additional precision op-amps are needed.

The AD8601, AD8602 and AD8604 are single, dual, and quad rail-to-rail, input and output, single-supply amplifiers featuring very low offset voltage and wide signal bandwidth, that can be used in place of AD8605, AD8606, and AD8608.

The AD7457 is a 12-bit, 100 kSPS, low power, SAR ADC, and can be used in combination with the ADR391 voltage reference in place of AD7091R, when a 300 kSPS throughput rate is not needed.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0335-PMDZ circuit board, the SDP-PMD-IB1Z and the EVAL-SDP-CB1Z system demonstration platform (SDP) evaluation board. The interposer board SDP-PMD-IB1Z and the SDP board EVAL-SDP-CB1Z have 120-pin mating connectors. The interposer board and the EVAL-CN0335-PMDZ board have 12-pin Pmod matching connectors, allowing quick setup and evaluation of the circuit's performance. The EVAL-CN0335-PMDZ board contains the circuit to be evaluated, as described in this note and the SDP evaluation board is used with the CN0335 evaluation software to capture the data from the EVAL-CN0335-PMDZ circuit board.

Equipment Needed

- PC with a USB port Windows® XP or Windows Vista® (32-bit), or Windows® 7/8 (64 or 32-bit)
- EVAL-CN0335-PMDZ circuit evaluation board
- EVAL-SDP-CB1Z SDP evaluation board
- SDP-PMD-IB1Z interposer board
- CN0335 evaluation software
- Precision voltage source

Getting Started

Load the evaluation software by placing the CN0335 evaluation software disc in the CD drive of the PC. You also can download the most up to date copy of the evaluation software from CN0335 evaluation software. Using "My Computer," locate the drive that contains the evaluation software disc and open the setup.exe. Follow the on-screen prompts to finish the installation. It is recommended to install all software components to the default locations.

Functional Block Diagram

Figure 5 shows the functional diagram of the test setup.

Setup

1. Connect the EVAL-CFTL-6V-PWRZ (+6 V dc power supply) to SDP-PMD-IB1Z interposer board via the dc barrel jack.
2. Connect the SDP-PMD-IB1Z (interposer board) to EVAL-SDP-CB1Z SDP board via the 120-pin ConA connector.
3. Connect the EVAL-SDP-CB1Z (SDP board) to the PC via the USB cable.
4. Connect the EVAL-CN0335-PMDZ evaluation board to the SDP-PMD-IB1Z interposer board via the 12-pin header Pmod connector.
5. Connect the voltage source (voltage generator) to the EVAL-CN0335-PMDZ evaluation board via the terminal block J2.

Test

Launch the evaluation software. The software communicates to the SDP board if the Analog Devices System Development Platform drivers are listed in the Device Manager. After USB communications are established, the SDP board can be used to send, receive, and capture serial data from the EVAL-CN0335-PMDZ board. Data can be saved in the computer for various values of input voltages. Information and details regarding how to use the evaluation software for data capturing can be found at CN0335 Software User Guide.

A photo of the EVAL-CN0335-PMDZ board is shown in Figure 6.

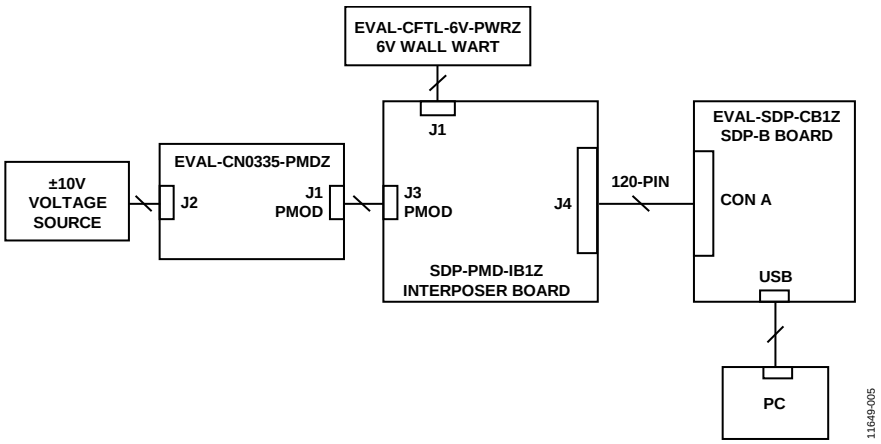

Figure 5. Test Setup Functional Block Diagram

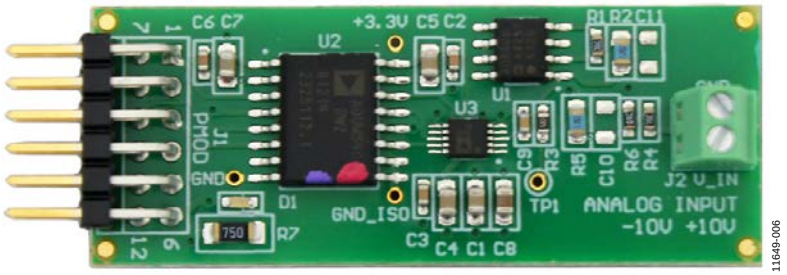

Figure 6. Photo of EVAL-CN0335-PMDZ Board

LEARN MORE

CN0335 Design Support Package: http://www.analog.com/CN0335-DesignSupport

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Krakauer, David. "Digital Isolation Offers Compact, Low-Cost Solutions to Challenging Design Problems."Analog Dialogue. Volume 40, December 2006.

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MT-101 Tutorial, *Decoupling Techniques*, Analog Devices

Wayne, Scott. "*i*Coupler® Digital Isolators Protect RS-232, RS-485, and CAN Buses in Industrial, Instrumentation, and Computer Apps, Analog Dialogue, Volume 39, Number 4, 2005.

Data Sheets and Evaluation Boards

AD8606 Data Sheet

AD7091R Data Sheet

ADuM5401 Data Sheet

REVISION HISTORY

3/14—Rev. 0 to Rev. A

Change to Circuit Function and Benefits Section 1

2/14—Revision 0: Initial Version