

## FEATURES

Low power, smallest pin-compatible, dual *nano*DAC: 12 bits

User-selectable external or internal reference

External reference default

On-chip 2.5 V,  $\pm 10$  ppm/ $^{\circ}$ C reference

10-lead MSOP

4.5 V to 5.5 V power supply

Guaranteed monotonic by design

Power-on reset to zero scale

Per channel power-down

Serial interface up to 50 MHz

Hardware LDAC and CLR functions

## ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC)

Extended temperature range:  $-55^{\circ}$ C to  $+105^{\circ}$ C

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available on request

## APPLICATIONS

Process control

Data acquisition systems

## GENERAL DESCRIPTION

The [AD5623R-EP](#), a member of the *nano*DAC<sup>®</sup> family, is a low power, dual 12-bit buffered voltage output digital-to-analog converter (DAC) that operates from a single 4.5 V to 5.5 V supply and is guaranteed monotonic by design.

The [AD5623R-EP](#) has an on-chip 2.5 V reference giving a maximum full-scale output of 5 V. The on-chip reference is off at power-up, allowing the use of an external reference.

The [AD5623R-EP](#) incorporates a power-on reset circuit that ensures that the output of the DACs powers up to 0 V and remains there until a valid write takes place. The [AD5623R-EP](#) contains a power-down feature that reduces the current consumption of the device to 0.48  $\mu$ A at 5 V and provides software-selectable output loads while in power-down mode.

The low power consumption of this device in normal operation makes it ideally suited to portable, battery-operated equipment.

The [AD5623R-EP](#) uses a versatile, 3-wire serial interface that operates at clock rates of up to 50 MHz, and is compatible with standard SPI, QSPI<sup>™</sup>, MICROWIRE<sup>™</sup>, and DSP interface standards. The on-chip precision output amplifier enables rail-to-rail output swing to be achieved. Additional application and technical information can be found in the [AD5623R](#) data sheet.

## PRODUCT HIGHLIGHTS

1. Dual 12-Bit DAC.
2. On-Chip 2.5 V,  $\pm 10$  ppm/ $^{\circ}$ C Reference.
3. Available in 10-Lead MSOP.
4. Low Power. Typically consumes 1.25 mW at 5 V. 4.5  $\mu$ s maximum settling time.

Table 1. Related Device

Part No.	Description
<a href="#">AD5623R</a>	2.7 V to 5.5 V, dual 12-bit <i>nano</i> DAC, with external reference

## FUNCTIONAL BLOCK DIAGRAM

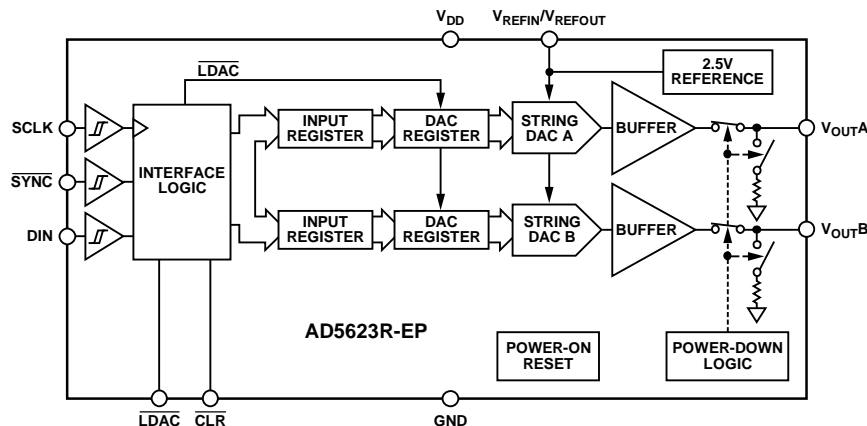


Figure 1.

Rev. A

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## TABLE OF CONTENTS

Features .....	1	Absolute Maximum Ratings .....	6
Enhanced Product Features .....	1	ESD Caution.....	6
Applications.....	1	Pin Configuration and Function Descriptions.....	7
General Description .....	1	Typical Performance Characteristics .....	8
Product Highlights .....	1	Applications Information .....	13
Functional Block Diagram .....	1	Using a Reference as a Power Supply.....	13
Revision History .....	2	Outline Dimensions .....	14
Specifications.....	3	Ordering Guide .....	14
AC Characteristics.....	4		
Timing Characteristics .....	4		

## REVISION HISTORY

### 9/15—Rev. 0 to Rev. A

Changes to Features Section.....	1
Added Enhanced Product Features Section.....	1
Change to Table 5 .....	6
Changes to Using a Reference as a Power Supply Section and Figure 33 .....	13
Deleted Terminology Section .....	13
Deleted Theory of Operation Section, Digital-to-Analog Architecture Section, Figure 33; Renumbered Sequentially, Resistor String Section, Output Amplifier Section, Figure 34, Internal Reference Section, External Reference Section, and Serial Interface Section .....	15
Deleted Input Shift Register Section, Table 7; Renumbered Sequentially, Table 8, SYNC Interrupt Section, Power-On Reset Section, Software Reset Section, Table 9, Figure 35, and Figure 36 .....	16
Deleted Power-Down Modes Section, Table 10 to Table 13, and Figure 37 .....	17
Deleted $\overline{\text{LDAC}}$ Function Section, Synchronous $\overline{\text{LDAC}}$ Section, Asynchronous $\overline{\text{LDAC}}$ Section, Table 14 to Table 16, and Internal Reference Setup Section.....	18
Deleted Microprocessor Interfacing Section, AD5623R-EP to Blackfin® ADSP-BF53x Interface Section, Figure 38, AD5623R-EP to M68HC11/MC68L11 Interface Section, Figure 39, AD5623R-EP to 80C51 Interface Section, Figure 40, AD5623R-EP to MICOWIRE Interface Section, and Figure 41.....	19
Deleted Power Supply Bypassing and Grounding Section .....	20

### 4/14—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ;  $R_L = 2\text{ k}\Omega$  to GND;  $C_L = 200\text{ pF}$  to GND;  $V_{REFIN}/V_{REFOUT} = V_{DD}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter <sup>1</sup>	Min	Typ	Max	Unit	Test Conditions/Comments
<b>STATIC PERFORMANCE<sup>2</sup></b>					
Resolution	12			Bits	
Relative Accuracy, INL		±1	±1.5	LSB	
Differential Nonlinearity, DNL			±1	LSB	Guaranteed monotonic by design
Zero-Scale Error		+2	+12	mV	All 0s loaded to DAC register
Offset Error		±1	±12	mV	
Full-Scale Error		-0.1	±1	% of FSR	All 1s loaded to DAC register
Gain Error			±1.5	% of FSR	
Zero-Scale Error Drift		±2		$\mu\text{V}/^\circ\text{C}$	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/ $^\circ\text{C}$
DC Power Supply Rejection Ratio		-100		dB	DAC code = midscale; $V_{DD} = 5\text{ V} \pm 10\%$
DC Crosstalk					
External Reference		10		$\mu\text{V}$	Due to full-scale output change; $R_L = 2\text{ k}\Omega$ to GND or $V_{DD}$
		10		$\mu\text{V}/\text{mA}$	Due to load current change
		5		$\mu\text{V}$	Due to powering down (per channel)
Internal Reference		25		$\mu\text{V}$	Due to full-scale output change; $R_L = 2\text{ k}\Omega$ to GND or $V_{DD}$
		20		$\mu\text{V}/\text{mA}$	Due to load current change
		10		$\mu\text{V}$	Due to powering down (per channel)
<b>OUTPUT CHARACTERISTICS<sup>3</sup></b>					
Output Voltage Range	0		$V_{DD}$	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	$R_L = 2\text{ k}\Omega$
DC Output Impedance		0.5		$\Omega$	
Short-Circuit Current		30		mA	$V_{DD} = 5\text{ V}$
Power-Up Time		4		$\mu\text{s}$	Coming out of power-down mode; $V_{DD} = 5\text{ V}$
<b>REFERENCE INPUTS</b>					
Reference Current		170	200	$\mu\text{A}$	$V_{REFIN}/V_{REFOUT} = V_{DD} = 5.5\text{ V}$
Reference Input Range	0.75		$V_{DD}$	V	
Reference Input Impedance		26		$\text{k}\Omega$	
<b>REFERENCE OUTPUT</b>					
Output Voltage	2.495		2.505	V	At ambient
Reference Temperature Coefficient <sup>3</sup>		±10		ppm/ $^\circ\text{C}$	
Output Impedance		7.5		$\text{k}\Omega$	
<b>LOGIC INPUTS<sup>3</sup></b>					
Input Current			±2	$\mu\text{A}$	All digital inputs
Input Low Voltage ( $V_{INL}$ )			0.8	V	$V_{DD} = 5\text{ V}$
Input High Voltage ( $V_{INH}$ )	2			V	$V_{DD} = 5\text{ V}$
Pin Capacitance		3		pF	$\overline{\text{DIN}}$ , $\overline{\text{SCLK}}$ , and $\overline{\text{SYNC}}$
		19		pF	$\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$
<b>POWER REQUIREMENTS</b>					
$V_{DD}$	4.5		5.5	V	
$I_{DD}$ (Normal Mode) <sup>4</sup>					$V_{INH} = V_{DD}$ and $V_{INL} = \text{GND}$
Internal Reference Off		0.25	0.45	mA	$V_{DD} = 4.5\text{ V to }5.5\text{ V}$
Internal Reference On		0.8	1	mA	$V_{DD} = 4.5\text{ V to }5.5\text{ V}$
$I_{DD}$ (All Power-Down Modes) <sup>5</sup>		0.48	1	$\mu\text{A}$	$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ , $V_{INH} = V_{DD}$ and $V_{INL} = \text{GND}$

<sup>1</sup> Temperature range =  $-55^\circ\text{C}$  to  $+105^\circ\text{C}$ , typical at  $+25^\circ\text{C}$ .

<sup>2</sup> Linearity calculated using a reduced code range: Code 32 to Code 4064. Output unloaded.

<sup>3</sup> Guaranteed by design and characterization, but not production tested.

<sup>4</sup> Interface inactive. All DACs active. DAC outputs unloaded.

<sup>5</sup> Both DACs powered down.

**AC CHARACTERISTICS**

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ;  $R_L = 2\text{ k}\Omega$  to GND;  $C_L = 200\text{ pF}$  to GND;  $V_{REFIN}/V_{REFOUT} = V_{DD}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 3.

Parameter <sup>1,2</sup>	Min	Typ	Max	Unit	Test Conditions/Comments
SLEW RATE		1.8		V/ $\mu$ s	
FEEDTHROUGH					
Digital Feedthrough		0.1		nV-sec	$V_{REFIN}/V_{REFOUT} = 2\text{ V} \pm 0.1\text{ V p-p}$ , frequency 10 Hz to 20 MHz
Reference Feedthrough		-90		dB	
CROSSTALK					
Digital Crosstalk		0.1		nV-sec	External reference
Analog Crosstalk		1		nV-sec	
		4		nV-sec	Internal reference
DAC-to-DAC Crosstalk		1		nV-sec	External reference
		4		nV-sec	Internal reference
MULTIPLYING BANDWIDTH		340		kHz	$V_{REFIN}/V_{REFOUT} = 2\text{ V} \pm 0.1\text{ V p-p}$
TOTAL HARMONIC DISTORTION		-80		dB	$V_{REFIN}/V_{REFOUT} = 2\text{ V} \pm 0.1\text{ V p-p}$ , frequency = 10 kHz
OUTPUT CHARACTERISTICS					
Digital-to-Analog Glitch Impulse		10		nV-sec	1 LSB change around major carry
Output Voltage Settling Time		3	4.5	$\mu$ s	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to $\pm 0.5$ LSB
Output Noise Spectral Density		120		nV/ $\sqrt{\text{Hz}}$	DAC code = midscale, 1 kHz
		100		nV/ $\sqrt{\text{Hz}}$	DAC code = midscale, 10 kHz
Output Noise		15		$\mu$ V p-p	0.1 Hz to 10 Hz

<sup>1</sup> Guaranteed by design and characterization, but not production tested.

<sup>2</sup> Temperature range =  $-55^\circ\text{C}$  to  $+105^\circ\text{C}$ , typical at  $+25^\circ\text{C}$ .

**TIMING CHARACTERISTICS**

All input signals are specified with  $t_R = t_F = 1\text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{INL} + V_{INH})/2$ .

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 4.

Parameter <sup>1</sup>	Limit at $T_{MIN}, T_{MAX}$	Unit	Description
$t_1^2$	20	ns min	SCLK cycle time
$t_2$	9	ns min	SCLK high time
$t_3$	9	ns min	SCLK low time
$t_4$	13	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
$t_5$	5	ns min	Data setup time
$t_6$	5	ns min	Data hold time
$t_7$	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
$t_8$	15	ns min	Minimum $\overline{\text{SYNC}}$ high time
$t_9$	13	ns min	$\overline{\text{SYNC}}$ rising edge to SCLK fall ignore
$t_{10}$	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ fall ignore
$t_{11}$	10	ns min	$\overline{\text{LDAC}}$ pulse width low
$t_{12}$	15	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ rising edge
$t_{13}$	5	ns min	$\overline{\text{CLR}}$ pulse width low
$t_{14}$	0	ns min	SCLK falling edge to $\overline{\text{LDAC}}$ falling edge
$t_{15}$	300	ns max	$\overline{\text{CLR}}$ pulse activation time

<sup>1</sup> Guaranteed by design and characterization, but not production tested.

<sup>2</sup> Maximum SCLK frequency is 50 MHz at  $V_{DD} = 2.7\text{ V to }5.5\text{ V}$ .

Timing Diagram

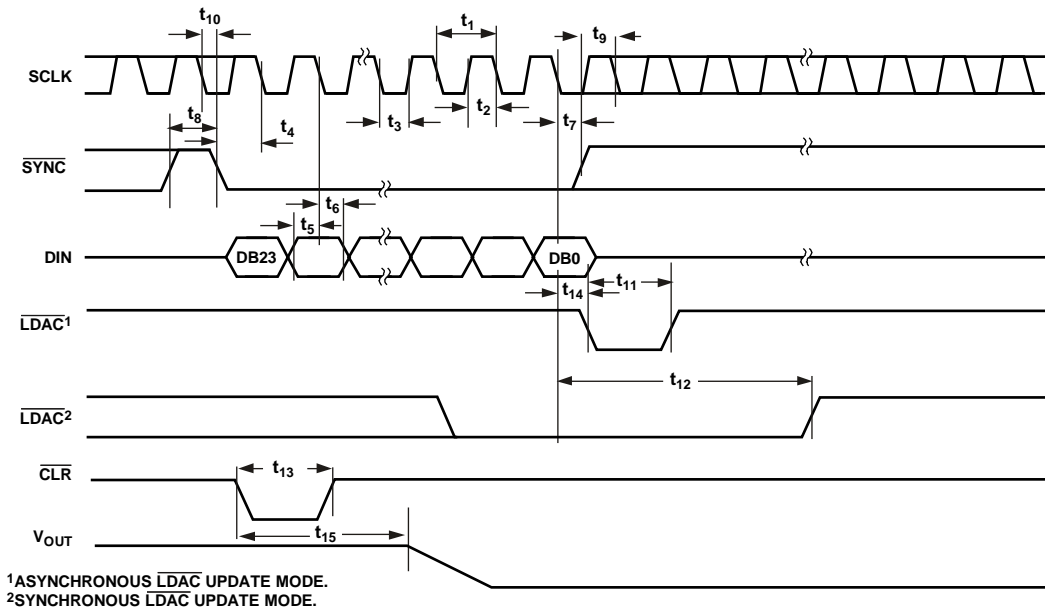


Figure 2. Serial Write Operation

12105-002

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +7 V
$V_{OUTx}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
$V_{REFIN}/V_{REFOUT}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Digital Input Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Industrial	$-55^\circ\text{C}$ to $+105^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Junction Temperature ( $T_{J\text{max}}$ )	$150^\circ\text{C}$
Power Dissipation	$(T_{J\text{max}} - T_A)/\theta_{JA}$
MSOP Package (4-Layer Board)	
$\theta_{JA}$ Thermal Impedance	$142^\circ\text{C}/\text{W}$
$\theta_{JC}$ Thermal Impedance	$43.7^\circ\text{C}/\text{W}$
Reflow Soldering Peak Temperature	
Pb-Free	$260 (+0/-5)^\circ\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

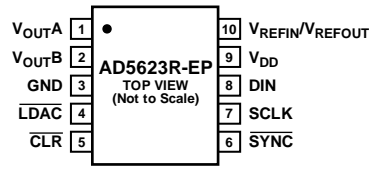


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{OUTA}$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	$V_{OUTB}$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
3	GND	Ground. Reference point for all circuitry on the device.
4	$\overline{LDAC}$	Load DAC. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
5	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. While $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The device exits clear code mode on the 24th falling edge of the next write to the device. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.
6	$\overline{SYNC}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
7	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
8	DIN	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
9	$V_{DD}$	Power Supply Input. This device can be operated from 4.5 V to 5.5 V. Decouple the supply with a 10 $\mu$ F capacitor in parallel with a 0.1 $\mu$ F capacitor to GND.
10	$V_{REFIN}/V_{REFOUT}$	Common Reference Input/Reference Output. When the internal reference is selected, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is a reference input.

TYPICAL PERFORMANCE CHARACTERISTICS

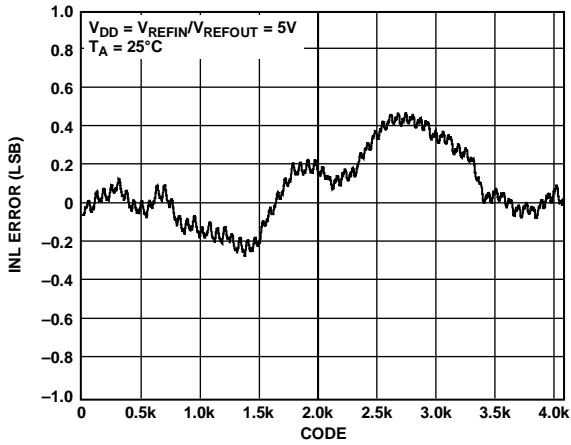


Figure 4. INL, External Reference

12105-007

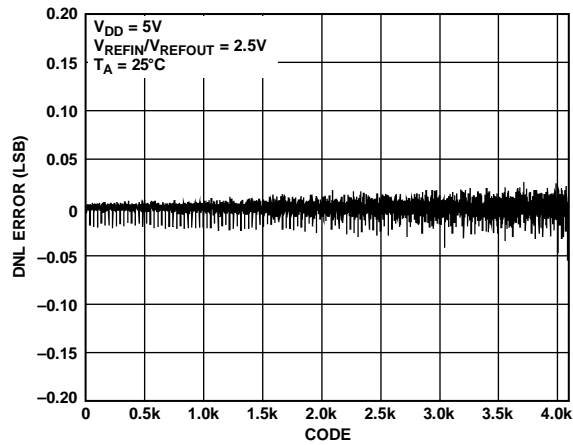


Figure 7. DNL, at 5 V<sub>DD</sub>

12105-016

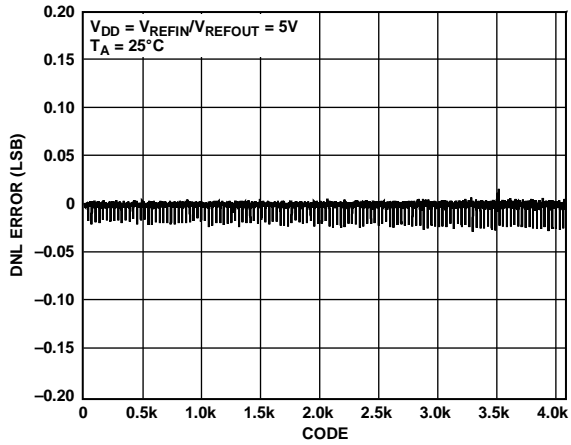


Figure 5. DNL, External Reference

12105-010

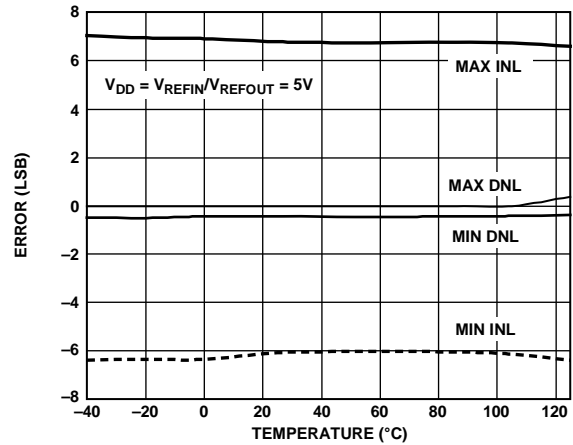


Figure 8. INL Error and DNL Error vs. Temperature

12105-080

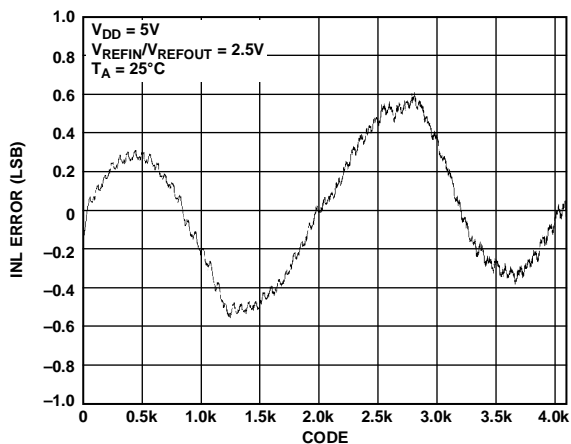


Figure 6. INL, at 5 V<sub>DD</sub>

12105-013

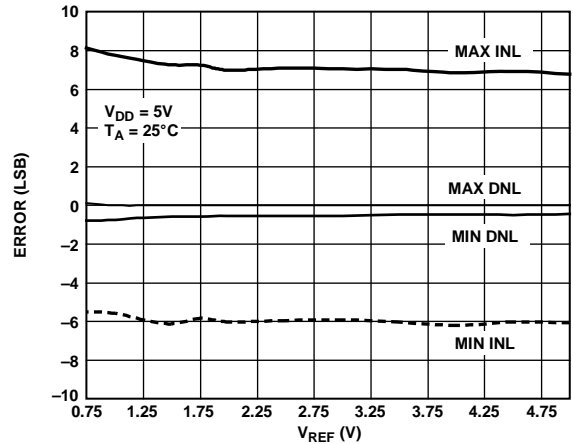


Figure 9. INL Error and DNL Error vs. V<sub>REF</sub>

12105-081



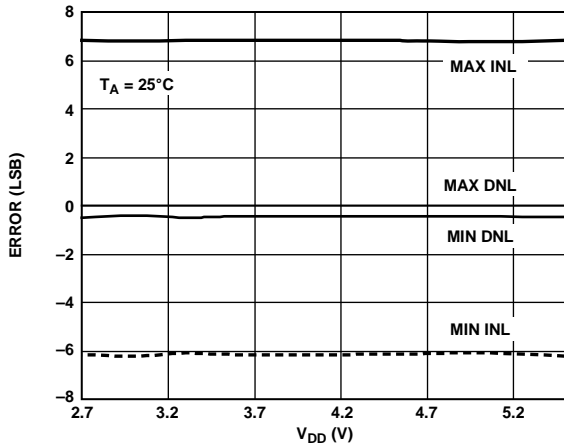


Figure 10. INL Error and DNL Error vs.  $V_{DD}$

12105-082

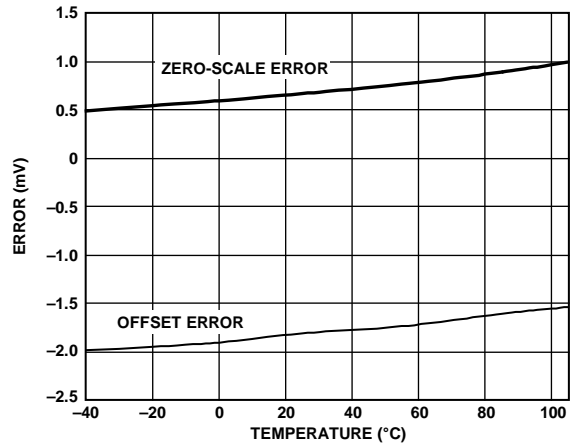


Figure 13. Zero-Scale Error and Offset Error vs. Temperature

12105-024

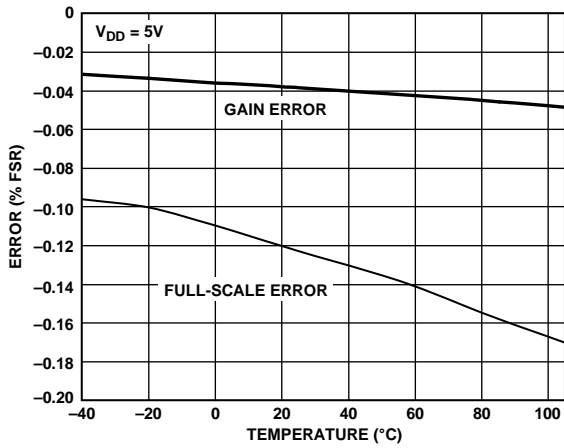


Figure 11. Gain Error and Full-Scale Error vs. Temperature

12105-023

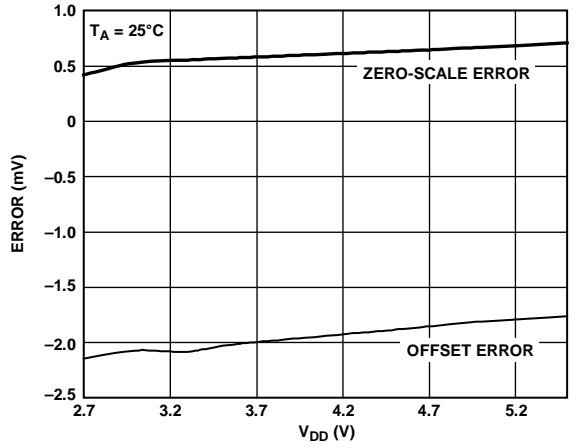


Figure 14. Zero-Scale Error and Offset Error vs.  $V_{DD}$

12105-026

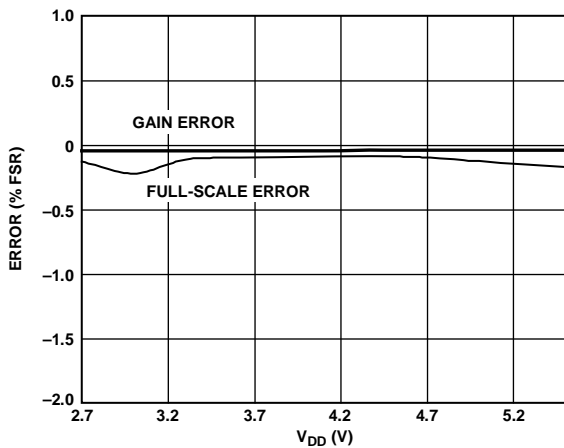


Figure 12. Gain Error and Full-Scale Error vs.  $V_{DD}$

12105-025

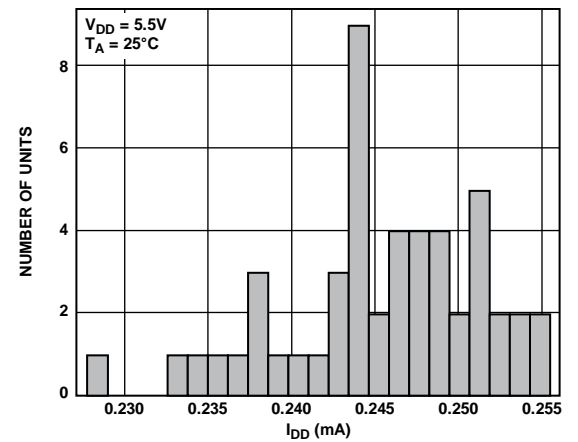


Figure 15.  $I_{DD}$  Histogram with External Reference

12105-080

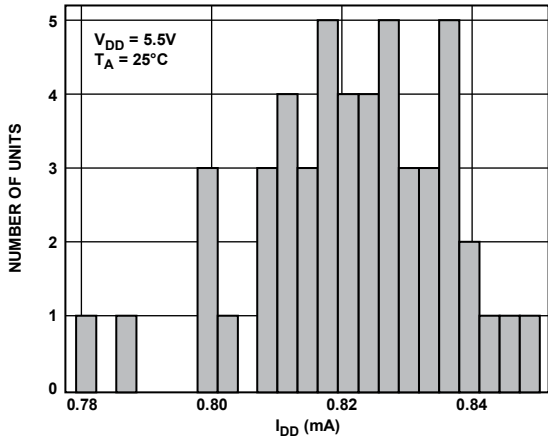


Figure 16.  $I_{DD}$  Histogram with Internal Reference

12105-091

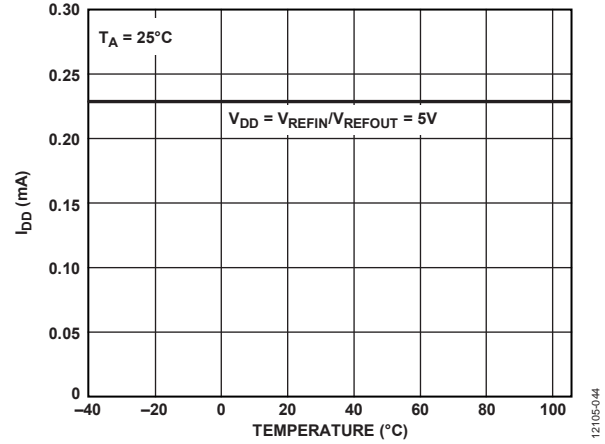


Figure 19. Supply Current vs. Temperature

12105-044

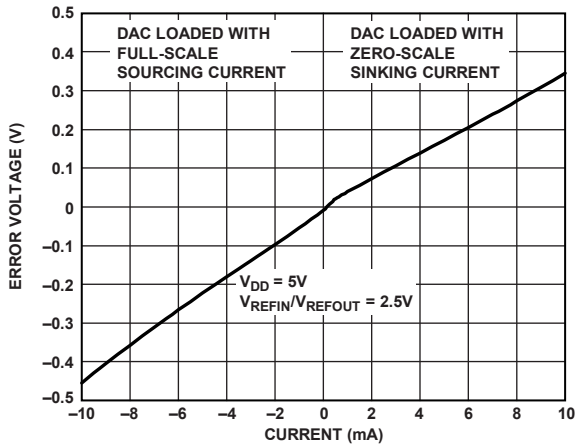


Figure 17. Headroom at Rails vs. Source and Sink Current

12105-029

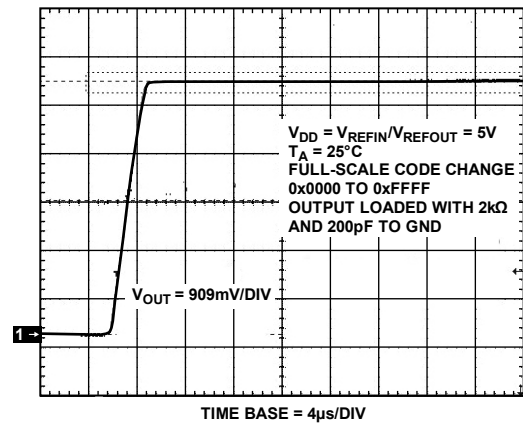


Figure 20. Full-Scale Settling Time, 5 V

12105-060

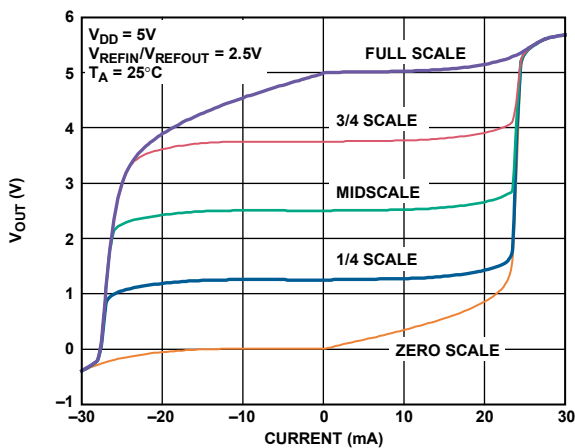


Figure 18. 5 V  $V_{DD}$  Source and Sink Capability

12105-030

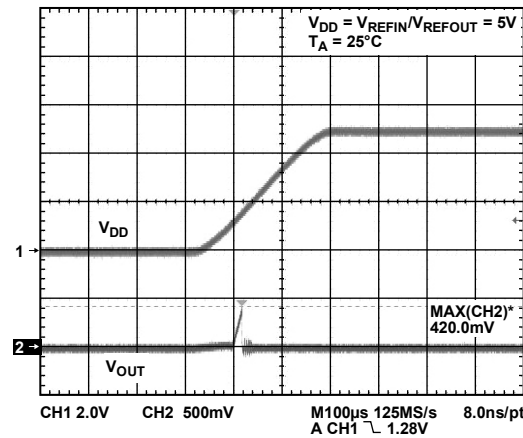


Figure 21. Power-On Reset to 0 V

12105-061

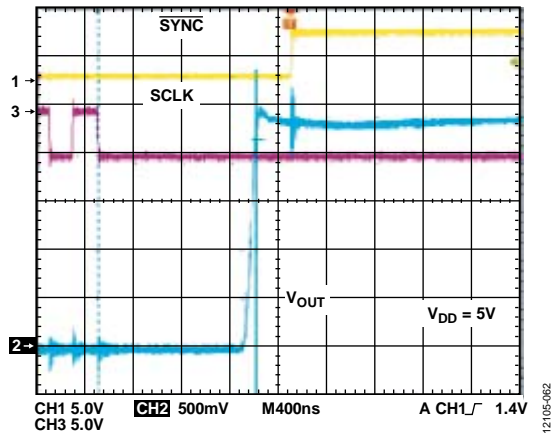


Figure 22. Exiting Power-Down to Midscale

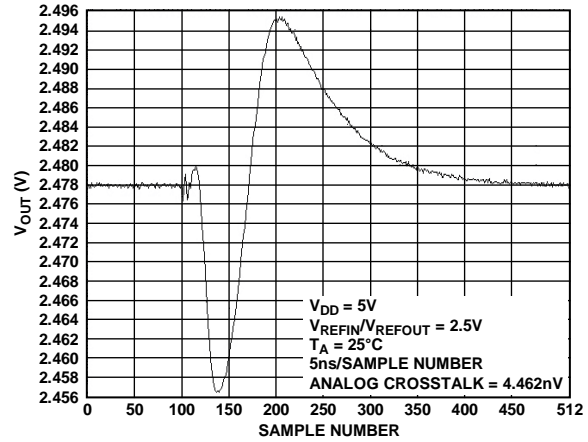


Figure 25. Analog Crosstalk, Internal Reference

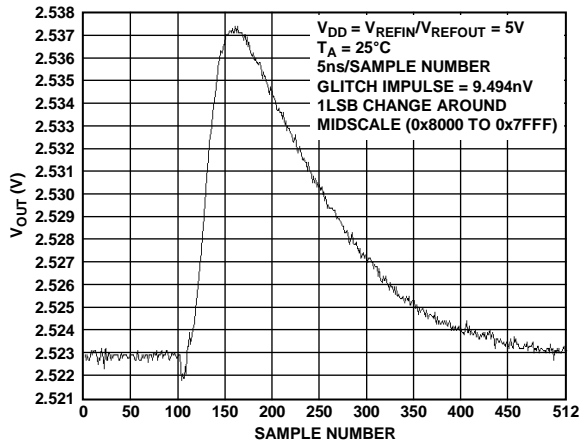


Figure 23. Digital-to-Analog Glitch Impulse (Negative)

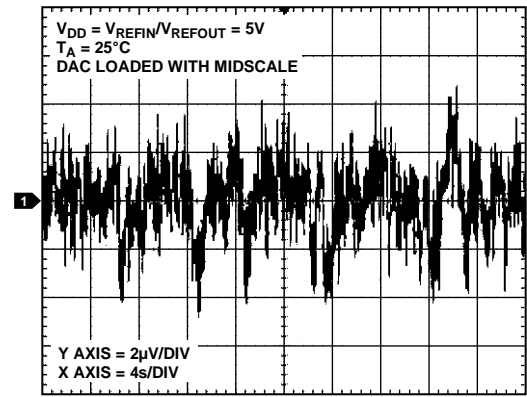


Figure 26. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

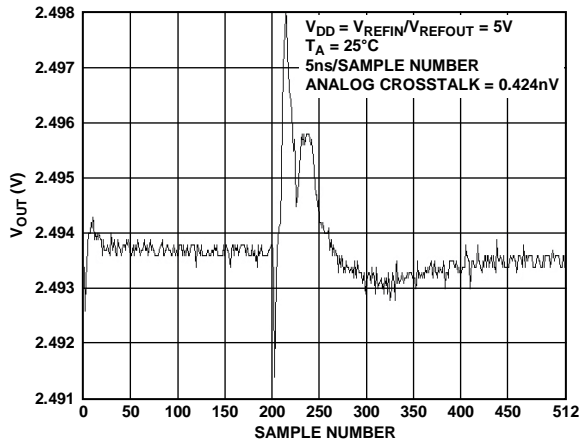


Figure 24. Analog Crosstalk, External Reference

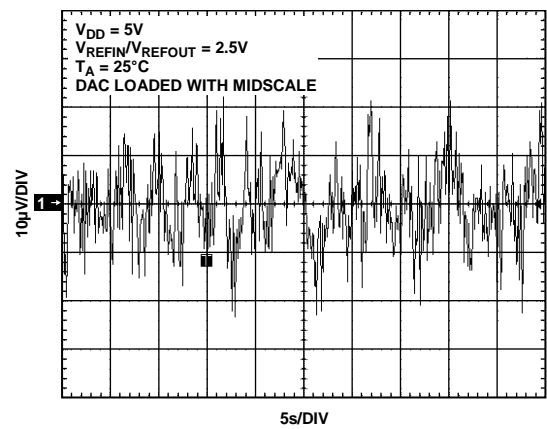


Figure 27. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

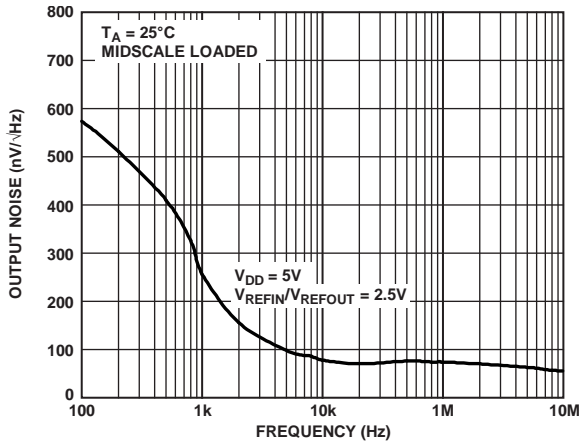


Figure 28. Noise Spectral Density, Internal Reference

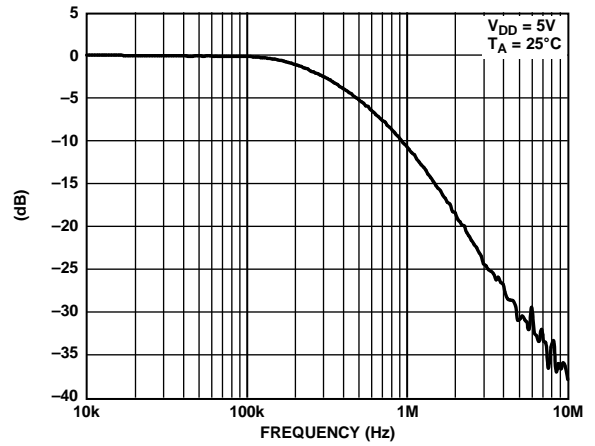


Figure 31. Multiplying Bandwidth

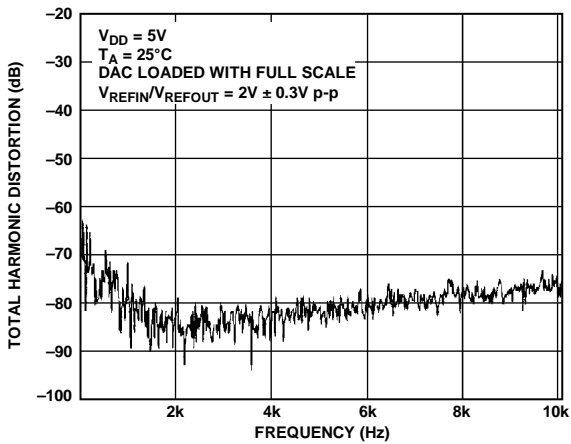


Figure 29. Total Harmonic Distortion

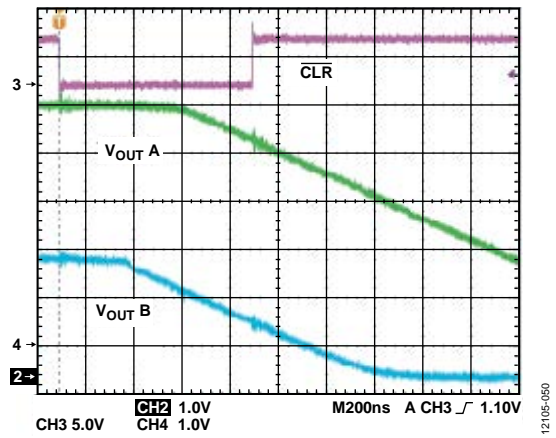


Figure 32. CLR Pulse Activation Time

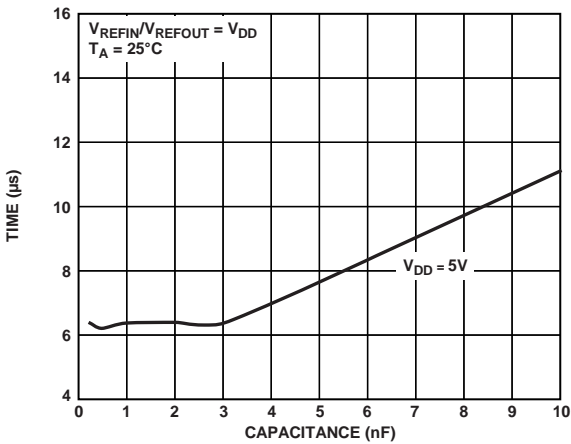


Figure 30. Settling Time vs. Capacitive Load

12105-066

12105-069

12105-067

12105-050

12105-068

## APPLICATIONS INFORMATION

### USING A REFERENCE AS A POWER SUPPLY

Because the supply current required by the [AD5623R-EP](#) is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the device (see Figure 33). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the [AD5623R-EP](#). If the [ADR293-EP](#) is used, it must supply  $\sim 500 \mu\text{A}$  of current to the [AD5623R-EP](#), with no load on the output of the DAC. When the DAC output is loaded, the [ADR293-EP](#) also needs to supply the current to the load. The total current required (with a  $5 \text{ k}\Omega$  load on the DAC output) is

$$500 \mu\text{A} + (5 \text{ V} / 5 \text{ k}\Omega) = 1.5 \text{ mA}$$

The load regulation of the [ADR293-EP](#) is typically 30 ppm/mA, which results in a 45 ppm ( $225 \mu\text{V}$ ) error for the 1.5 mA current drawn from it. This corresponds to a 0.184 LSB error.

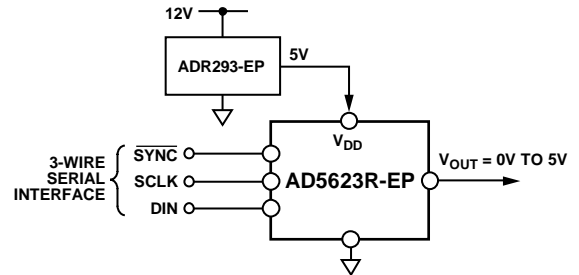
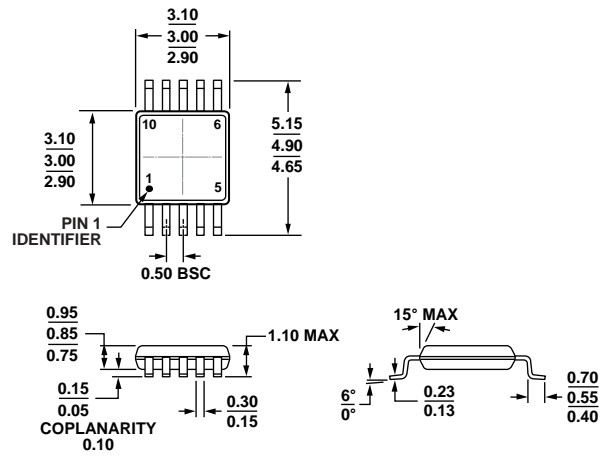


Figure 33. [ADR293-EP](#) as Power Supply to the [AD5623R-EP](#)

12105-041

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 34. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

Dimensions shown in millimeters

091709-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Accuracy	Internal Reference	Package Description	Package Option	Branding
AD5623RSRMZ-EP-5R7	-55°C to +105°C	±1.5 LSB INL	2.5 V	10-Lead MSOP	RM-10	DN9

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**