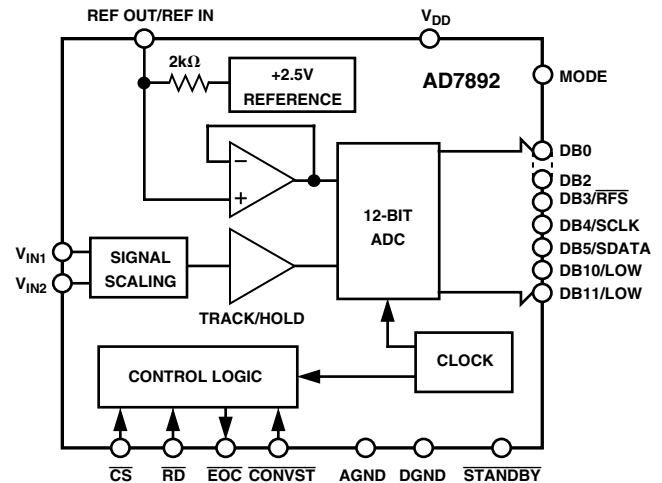


**FEATURES**

**Fast 12-Bit ADC with 1.47  $\mu$ s Conversion Time**  
**600 kSPS Throughput Rate (AD7892-3)**  
**500 kSPS Throughput Rate (AD7892-1, AD7892-2)**  
**Single Supply Operation**  
**On-Chip Track/Hold Amplifier**  
**Selection of Input Ranges:**  
 $\pm 10$  V or  $\pm 5$  V for AD7892-1  
 0 V to +2.5 V for AD7892-2  
 $\pm 2.5$  V for AD7892-3  
**High Speed Serial and Parallel Interface**  
**Low Power, 60 mW typ**  
**Overvoltage Protection on Analog Inputs (AD7892-1  
 and AD7892-3)**

**FUNCTIONAL BLOCK DIAGRAM**

**GENERAL DESCRIPTION**

The AD7892 is a high speed, low power, 12-bit A/D converter that operates from a single +5 V supply. The part contains a 1.47  $\mu$ s successive approximation ADC, an on-chip track/hold amplifier, an internal +2.5 V reference and on-chip versatile interface structures that allow both serial and parallel connection to a microprocessor. The part accepts an analog input range of  $\pm 10$  V or  $\pm 5$  V (AD7892-1), 0 V to +2.5 V (AD7892-2) and  $\pm 2.5$  V (AD7892-3). Overvoltage protection on the analog inputs for the AD7892-1 and AD7892-3 allows the input voltage to go to  $\pm 17$  V or  $\pm 7$  V respectively without damaging the ports.

The AD7892 offers a choice of two data output formats: a single, parallel, 12-bit word or serial data. Fast bus access times and standard control inputs ensure easy parallel interface to microprocessors and digital signal processors. A high speed serial interface allows direct connection to the serial ports of microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7892 is fabricated in Analog Devices' Linear Compatible CMOS (LC<sup>2</sup>MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. It is available in a 24-lead, 0.3" wide, plastic or hermetic DIP or in a 24-lead SOIC.

**PRODUCT HIGHLIGHTS**

1. The AD7892-3 features a conversion time of 1.47  $\mu$ s and a track/hold acquisition time of 200 ns. This allows a throughput rate for the part up to 600 kSPS. The AD7892-1 and AD7892-2 operate with throughput rates of 500 kSPS.
2. The AD7892 operates from a single +5 V supply and consumes 60 mW typ making it ideal for low power and portable applications.
3. The part offers a high speed, flexible interface arrangement with parallel and serial interfaces for easy connection to microprocessors, microcontrollers and digital signal processors.

**REV. C**

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# AD7892\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD7892 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-414: Low Cost, Low Power Devices for HDSL Applications

### Data Sheet

- AD7892: LC<sup>2</sup>MOS Single Supply, 12-Bit 600 kSPS ADC Data Sheet
- AD7892: Military Data Sheet

### Product Highlight

- 8- to 18-Bit SAR ADCs ... From the Leader in High Performance Analog

## REFERENCE MATERIALS

### Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

## DESIGN RESOURCES

- AD7892 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD7892 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

# AD7892—SPECIFICATIONS ( $V_{DD} = +5\text{ V} \pm 5\%$ , $AGND = DGND = 0\text{ V}$ , $REF\ IN = +2.5\text{ V}$ . All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

Parameter	A Versions <sup>1</sup>	B Versions	S Version <sup>2</sup>	Unit	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>					
AD7892-1, AD7892-2					
Signal to (Noise + Distortion) Ratio <sup>3</sup>	70	70	70	dB min	$f_{IN} = 100\text{ kHz}$ . $f_{SAMPLE} = 500\text{ kSPS}$
Total Harmonic Distortion <sup>3</sup>	-78	-78	-78	dB max	typ -84 dB
Peak Harmonic or Spurious Noise <sup>3</sup>	-79	-79	-79	dB max	
Intermodulation Distortion <sup>3</sup>					
2nd Order Terms	-78	-78	-78	dB max	$f_a = 49\text{ kHz}$ , $f_b = 50\text{ kHz}$
3rd Order Terms	-78	-78	-78	dB max	typ -84 dB
AD7892-3					
Signal to (Noise + Distortion) Ratio <sup>3</sup>	70	70		dB min	$f_{IN} = 100\text{ kHz}$ . $f_{SAMPLE} = 600\text{ kSPS}$
Total Harmonic Distortion <sup>3</sup>	-78	-78		dB max	
Peak Harmonic or Spurious Noise <sup>3</sup>	-79	-79		dB max	
Intermodulation Distortion <sup>3</sup>					
2nd Order Terms	-78	-78		dB max	$f_a = 49\text{ kHz}$ , $f_b = 50\text{ kHz}$
3rd Order Terms	-78	-78		dB max	
<b>DC ACCURACY</b>					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed					
Relative Accuracy <sup>3</sup>	$\pm 1.5$	$\pm 1$	$\pm 1$	Bits	
Differential Nonlinearity <sup>3</sup>	$\pm 1$	$\pm 1$	$\pm 1$	LSB max	
AD7892-1					
Positive Full-Scale Error <sup>3</sup>	$\pm 4$	$\pm 4$	$\pm 5$	LSB max	
Negative Full-Scale Error <sup>3</sup>	$\pm 4$	$\pm 4$	$\pm 5$	LSB max	
Bipolar Zero Error <sup>3</sup>	$\pm 3$	$\pm 2$	$\pm 3$	LSB max	
AD7892-3					
Positive Full-Scale Error <sup>3</sup>	$\pm 4$	$\pm 4$		LSB max	
Negative Full-Scale Error <sup>3</sup>	$\pm 4$	$\pm 4$		LSB max	
Bipolar Zero Error <sup>3</sup>	$\pm 4$	$\pm 3$		LSB max	
AD7892-2					
Positive Full-Scale Error <sup>3</sup>	$\pm 5$	$\pm 5$	$\pm 5$	LSB max	
Unipolar Offset Error <sup>3</sup>	$\pm 4$	$\pm 3$	$\pm 4$	LSB max	
<b>ANALOG INPUT</b>					
AD7892-1					
Input Voltage Range	$\pm 10$	$\pm 10$	$\pm 10$	Volts	Input Applied to $V_{IN1}$ with $V_{IN2}$ Grounded
Input Voltage Range	$\pm 5$	$\pm 5$	$\pm 5$	Volts	Input Applied to $V_{IN1}$ and $V_{IN2}$
Input Resistance	8	8	8	k $\Omega$ min	Input Applied to $V_{IN1}$ with $V_{IN2}$ Grounded
AD7892-2					
Input Voltage Range on $V_{IN1}$	0 to +2.5	0 to +2.5	0 to +2.5	Volts	Input Applied to $V_{IN1}$
Input Current	10	10	50	nA max	
Input Voltage Range on $V_{IN2}$	$\pm 50$	$\pm 50$	$\pm 50$	mV max	
AD7892-3					
Input Voltage Range on $V_{IN1}$	$\pm 2.5$	$\pm 2.5$		Volts	Input Applied to $V_{IN1}$
Input Resistance	2	2		k $\Omega$ min	
<b>REFERENCE OUTPUT/INPUT</b>					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	$2.5\text{ V} \pm 5\%$
Input Impedance	1.6	1.6	1.6	k $\Omega$ min	Resistor Connected to Internal Reference Node
Input Capacitance <sup>4</sup>	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	$\pm 10$	$\pm 10$	$\pm 10$	mV max	
$T_{MIN}$ to $T_{MAX}$	$\pm 20$	$\pm 20$	$\pm 25$	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	5.5	5.5	5.5	k $\Omega$ nom	
<b>LOGIC INPUTS</b>					
Input High Voltage, $V_{INH}$	2.4	2.4	2.4	V min	$V_{DD} = 5\text{ V} \pm 5\%$
Input Low Voltage, $V_{INL}$	0.8	0.8	0.8	V max	$V_{DD} = 5\text{ V} \pm 5\%$
Input Current, $I_{IN}$	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	$V_{IN} = 0\text{ V}$ to $V_{DD}$
Input Capacitance, $C_{IN}^4$	10	10	10	pF max	

Parameter	A Versions <sup>1</sup>	B Versions	S Version <sup>2</sup>	Unit	Test Conditions/Comments
<b>LOGIC OUTPUTS</b>					
Output High Voltage, $V_{OH}$	4.0	4.0	4.0	V min	$I_{SOURCE} = 200 \mu A$ $I_{SINK} = 1.6 mA$
Output Low Voltage, $V_{OL}$	0.4	0.4	0.4	V max	
DB11–DB0					
Floating-State Leakage Current	$\pm 10$	$\pm 10$	$\pm 10$	$\mu A$ max	
Floating-State Capacitance <sup>4</sup>	15	15	15	pF max	
Output Coding	Two's Complement				
AD7892-1 and AD7892-3	Straight (Natural) Binary				
AD7892-2	Straight (Natural) Binary				
<b>CONVERSION RATE</b>					
Conversion Time	1.47	1.47		$\mu s$ max	AD7892-3
Track/Hold Acquisition Time <sup>3</sup>	0.2	0.2		$\mu s$ max	AD7892-3
Conversion Time	1.6	1.6	1.68	$\mu s$ max	AD7892-1 and AD7892-2
Track/Hold Acquisition Time <sup>3</sup>	0.4	0.4	0.32	$\mu s$ max	AD7892-1 and AD7892-2
<b>POWER REQUIREMENTS</b>					
$V_{DD}$	+5	+5	+5	V nom	$\pm 5\%$ for Specified Performance
$I_{DD}$ <sup>5</sup>					
Normal Operation	18	18	19	mA max	
Standby Mode <sup>6</sup>					
AD7892-2	250	250		$\mu A$ typ	
AD7892-3, AD7892-1	80	80	100	$\mu A$ max	typ 15 $\mu A$
Power Dissipation <sup>7</sup>					
Normal Operation	90	90	95	mW max	$V_{DD} = +5 V$ . Typically 60 mW
Standby Mode <sup>6</sup>					
AD7892-2	1.25	1.25		mW typ	
AD7892-3, AD7892-1	400	400	500	$\mu W$ max	$V_{DD} = +5 V$ . Typically 75 $\mu W$

**NOTES**

<sup>1</sup>Temperature ranges are as follows: A, B Versions:  $-40^{\circ}C$  to  $+85^{\circ}C$ ; S Version:  $-55^{\circ}C$  to  $+125^{\circ}C$ .

<sup>2</sup>S Version available on AD7892-1 and AD7892-2 only.

<sup>3</sup>See Terminology.

<sup>4</sup>Sample tested @  $+25^{\circ}C$  to ensure compliance.

<sup>5</sup>These normal mode and standby mode currents are achieved with resistors (in the range 10 k $\Omega$  to 100 k $\Omega$ ) to either DGND or  $V_{DD}$  on Pins 8, 9, 16 and 17.

<sup>6</sup>A conversion should not be initiated on the part within 30  $\mu s$  of exiting standby mode.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS\***

( $T_A = +25^{\circ}C$  unless otherwise noted)

$V_{DD}$  to AGND . . . . .  $-0.3 V$  to  $+7 V$

$V_{DD}$  to DGND . . . . .  $-0.3 V$  to  $+7 V$

Analog Input Voltage to AGND

AD7892-1 . . . . .  $\pm 17 V$

AD7892-2 . . . . .  $-0.3 V, V_{DD}$

AD7892-3 . . . . .  $\pm 7 V$

Reference Input Voltage to AGND . . . . .  $-0.3 V$  to  $V_{DD} + 0.3 V$

Digital Input Voltage to DGND . . . . .  $-0.3 V$  to  $V_{DD} + 0.3 V$

Digital Output Voltage to DGND . . . . .  $-0.3 V$  to  $V_{DD} + 0.3 V$

Operating Temperature Range

Commercial (A, B Versions) . . . . .  $-40^{\circ}C$  to  $+85^{\circ}C$

Extended (S Version) . . . . .  $-55^{\circ}C$  to  $+125^{\circ}C$

Storage Temperature Range . . . . .  $-65^{\circ}C$  to  $+150^{\circ}C$

Junction Temperature . . . . .  $+150^{\circ}C$

Plastic DIP Package, Power Dissipation . . . . . 450 mW

$\theta_{JA}$  Thermal Impedance . . . . .  $105^{\circ}C/W$

Lead Temperature (Soldering, 10 sec) . . . . .  $+260^{\circ}C$

Cerdip Package, Power Dissipation . . . . . 450 mW

$\theta_{JA}$  Thermal Impedance . . . . .  $70^{\circ}C/W$

Lead Temperature (Soldering, 10 sec) . . . . .  $+300^{\circ}C$

SOIC Package, Power Dissipation . . . . . 450 mW

$\theta_{JA}$  Thermal Impedance . . . . .  $75^{\circ}C/W$

Lead Temperature, Soldering

Vapor Phase (60 sec) . . . . .  $+215^{\circ}C$

Infrared (15 sec) . . . . .  $+220^{\circ}C$

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# AD7892

## TIMING CHARACTERISTICS<sup>1, 2</sup> ( $V_{DD} = +5\text{ V} \pm 5\%$ , $AGND = DGND = 0\text{ V}$ , $REF\ IN = +2.5\text{ V}$ )

Parameter	A, B Versions	S Version	Unit	Test Conditions/Comments
$t_{CONV}$	1.47 1.6	1.68	$\mu\text{s max}$ $\mu\text{s max}$	Conversion Time for AD7892-3 Conversion Time for AD7892-1, AD7892-2
$t_{ACQ}$	200 400	320	$\text{ns min}$ $\text{ns min}$	Acquisition Time for AD7892-3 Acquisition Time for AD7892-1, AD7892-2
<b>Parallel Interface</b>				
$t_1$	35	45	$\text{ns min}$	$\overline{CONVST}$ Pulsewidth
$t_2$	60	60	$\text{ns min}$	$\overline{EOC}$ Pulsewidth
$t_3$	0	0	$\text{ns min}$	$\overline{EOC}$ Falling Edge to $\overline{CS}$ Falling Edge Setup Time
$t_4$	0	0	$\text{ns min}$	$\overline{CS}$ to $\overline{RD}$ Setup Time
$t_5$	35	45	$\text{ns min}$	Read Pulsewidth
$t_6^3$	35	40	$\text{ns max}$	Data Access Time After Falling Edge of $\overline{RD}$
$t_7^4$	5	5	$\text{ns min}$	Bus Relinquish Time After Rising Edge of $\overline{RD}$
	30	40	$\text{ns max}$	
$t_8$	0	0	$\text{ns min}$	$\overline{CS}$ to $\overline{RD}$ Hold Time
$t_9$	200	200	$\text{ns min}$	$\overline{RD}$ to $\overline{CONVST}$ Setup Time
<b>Serial Interface</b>				
$t_{10}$	30	35	$\text{ns min}$	$\overline{RFS}$ Low to SCLK Falling Edge Setup Time
$t_{11}^3$	25	30	$\text{ns max}$	$\overline{RFS}$ Low to Data Valid Delay
$t_{12}$	25	25	$\text{ns min}$	SCLK High Pulsewidth
$t_{13}$	25	25	$\text{ns min}$	SCLK Low Pulsewidth
$t_{14}^3$	5	5	$\text{ns min}$	SCLK Rising Edge to Data Valid Hold Time
$t_{15}^3$	25	30	$\text{ns max}$	SCLK Rising Edge to Data Valid Delay
$t_{16}$	20	30	$\text{ns min}$	$\overline{RFS}$ to SCLK Falling Edge Hold Time
$t_{17}^4$	0	0	$\text{ns min}$	Bus Relinquish Time after Rising Edge of $\overline{RFS}$
	30	30	$\text{ns max}$	
$t_{17A}^4$	0	0	$\text{ns min}$	Bus Relinquish Time after Rising Edge of SCLK
	30	30	$\text{ns max}$	

### NOTES

<sup>1</sup>Sample tested at +25°C to ensure compliance. All input signals are measured with  $t_r = t_f = 1\text{ ns}$  (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.

<sup>2</sup>See Figures 2 and 3.

<sup>3</sup>Measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

<sup>4</sup>These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

<sup>5</sup>Assumes CMOS loads on the data bits. With TTL loads, more current is drawn from the data lines and the  $\overline{RD}$  to  $\overline{CONVST}$  time needs to be extended to 400 ns min. Specifications subject to change without notice.

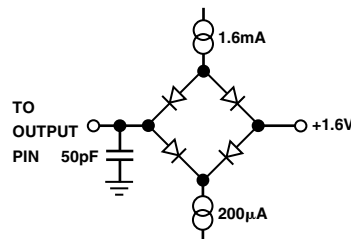


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

### CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7892 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## ORDERING GUIDE

Model	Input Range	Sample Rate	Relative Accuracy	Temperature Range	Package Option <sup>1</sup>
AD7892AN-1	±5 V or ±10 V	500 kSPS		−40°C to +85°C	N-24
AD7892BN-1	±5 V or ±10 V	500 kSPS	±1 LSB	−40°C to +85°C	N-24
AD7892AR-1	±5 V or ±10 V	500 kSPS		−40°C to +85°C	R-24
AD7892BR-1	±5 V or ±10 V	500 kSPS	±1 LSB	−40°C to +85°C	R-24
AD7892SQ-1	±5 V or ±10 V	500 kSPS	±1 LSB	−55°C to +125°C	Q-24
AD7892AN-2	0 V to +2.5 V	500 kSPS		−40°C to +85°C	N-24
AD7892BN-2	0 V to +2.5 V	500 kSPS	±1 LSB	−40°C to +85°C	N-24
AD7892AR-2	0 V to +2.5 V	500 kSPS		−40°C to +85°C	R-24
AD7892BR-2	0 V to +2.5 V	500 kSPS	±1 LSB	−40°C to +85°C	R-24
AD7892AN-3	±2.5 V	600 kSPS		−40°C to +85°C	N-24
AD7892BN-3	±2.5 V	600 kSPS	±1 LSB	−40°C to +85°C	N-24
AD7892AR-3	±2.5 V	600 kSPS		−40°C to +85°C	R-24
AD7892BR-3	±2.5 V	600 kSPS	±1 LSB	−40°C to +85°C	R-24
EVAL-AD7892-2CB <sup>2</sup>	Evaluation Board				
EVAL-AD7892-3CB <sup>2</sup>	Evaluation Board				
EVAL-CONTROL BOARD <sup>3</sup>	Controller Board				

## NOTES

<sup>1</sup>N = Plastic DIP; Q = Cerdip; R = SOIC.

<sup>2</sup>These boards can be used as stand-alone evaluation boards or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

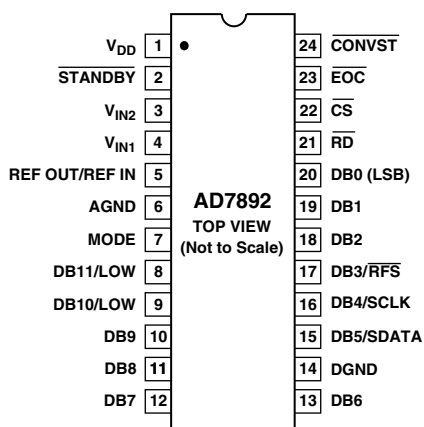
<sup>3</sup>This board is a complete unit allowing a PC to control and communicate with all Analog Devices' evaluation boards ending in the CB designators.

## PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Positive Supply Voltage, +5 V ± 5%.
2	<u>STANDBY</u>	Standby Input. Logic Input. With this input at a logic high, the part is in its normal operating mode; with this input at a logic low, the part is placed in its standby or power-down mode, which reduces power consumption to 5 mW typical.
3	V <sub>IN2</sub>	Analog Input 2. For the AD7892-1, this input either connects to AGND or to V <sub>IN1</sub> to determine the analog input voltage range. With V <sub>IN2</sub> connected to AGND on the AD7892-1, the analog input range at the V <sub>IN1</sub> input is ±10 V. With V <sub>IN2</sub> connected to V <sub>IN1</sub> on the AD7892-1, the analog input range to the part is ±5 V. For the AD7892-2 and AD7892-3, this input can be left unconnected but must not be connected to a potential other than AGND.
4	V <sub>IN1</sub>	Analog Input 1. The analog input voltage to be converted by the AD7892 is applied to this input. For the AD7892-1, the input voltage range is either ±5 V or ±10 V depending on where the V <sub>IN2</sub> input is connected. For the AD7892-2, the voltage range on the V <sub>IN1</sub> input is 0 V to +2.5 V with respect to the voltage appearing at the V <sub>IN2</sub> input. For the AD7892-3, the voltage range on the V <sub>IN1</sub> input is ±2.5 V.
5	REF OUT/REF IN	Voltage Reference Output/Input. The part can be used with either its own internal reference or with an external reference source. The on-chip +2.5 V reference is provided at this pin. When using this internal reference as the reference source for the part, REF OUT should be decoupled to AGND with a 0.1 μF disc ceramic capacitor. The output impedance of this reference source is typically 5.5 kΩ. When using an external reference source as the reference voltage for the part, the reference source should be connected to this pin. This overdrives the internal reference and provides the reference source for the part. The REF IN input is buffered on-chip but must be able to sink or source current through the resistor to the output of the on-chip reference. The nominal reference voltage for correct operation of the AD7892 is +2.5 V.
6	AGND	Analog Ground. Ground reference for track/hold, comparator and DAC.
7	MODE	Mode. Control input which determines the interface mode for the AD7892. With this pin at a logic low, the device is in its serial interface mode; with this pin at a logic high, the device is in its parallel interface mode.
8	DB11/LOW	Data Bit 11/Test Pin. When the device is in its parallel mode, this pin is Data Bit 11 (MSB), a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation of the AD7892.
9	DB10/LOW	Data Bit 10/Test Pin. When the device is in its parallel mode, this pin is Data Bit 10, a three-state TTL-compatible output. When the device is in its serial mode, this is used as a test pin which must be tied to a logic low for correct operation of the AD7892.
10	DB9	Data Bit 9. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
11	DB8	Data Bit 8. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
12	DB7	Data Bit 7. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
13	DB6	Data Bit 6. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
14	DGND	Digital Ground. Ground reference for digital circuitry.
15	DB5/SDATA	Data Bit 5/Serial Data. When the device is in its parallel mode, this pin is Data Bit 5, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial data output line. Sixteen bits of serial data are provided with four leading zeros preceding the 12 bits of valid data. Serial data is valid on the falling edge of SCLK for sixteen edges after $\overline{\text{RFS}}$ goes low. Output coding is two's complement for AD7892-1 and AD7892-3 and straight (natural) binary for AD7892-2.

Pin No.	Mnemonic	Description
16	DB4/SCLK	Data Bit 4/Serial Clock. When the device is in its parallel mode, this pin is Data Bit 4, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the serial clock pin, SCLK. SCLK is an input and an external serial clock must be provided at this pin to obtain serial data from the AD7892. Serial data is clocked out from the output shift register on the rising edges of SCLK after $\overline{RFS}$ goes low.
17	DB3/ $\overline{RFS}$	Data Bit 3/Receive Frame Synchronization. When the device is in its parallel mode, this pin is Data Bit 3, a three-state TTL-compatible output. When the device is in its serial mode, this becomes the receive frame synchronization input with $\overline{RFS}$ provided externally to obtain serial data from the AD7892.
18	DB2	Data Bit 2. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
19	DB1	Data Bit 1. Three-state TTL-compatible output. This output should be left unconnected when the device is in its serial mode.
20	DB0	Data Bit 0 (LSB). Three-state TTL-compatible output. Output coding is two's complement for AD7892-1 and AD7892-3 and straight (natural) binary for AD7892-2. This output should be left unconnected when the device is in its serial mode.
21	$\overline{RD}$	Read. Active low logic input which is used in conjunction with $\overline{CS}$ low to enable the data outputs.
22	$\overline{CS}$	Chip Select. Active low logic input which is used in conjunction with $\overline{RD}$ to enable the data outputs.
23	$\overline{EOC}$	End-of-Conversion. Active low logic output indicating converter status. The end of conversion is signified by a low going pulse on this line. The duration of this $\overline{EOC}$ pulse is nominally 100 ns.
24	$\overline{CONVST}$	Convert Start. Logic Input. A low-to-high transition on this input puts the track/hold into its hold mode and starts conversion.

### PIN CONFIGURATION DIP and SOIC





# AD7892

## TERMINOLOGY

### Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ( $f_s/2$ ), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB.

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7892, it is defined as:

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where  $V_1$  is the rms amplitude of the fundamental and  $V_2$ ,  $V_3$ ,  $V_4$ ,  $V_5$  and  $V_6$  are the rms amplitudes of the second through the sixth harmonics.

### Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to  $f_s/2$  and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

### Intermodulation Distortion

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any active device with nonlinearities will create distortion products at sum and difference frequencies of  $m f_a \pm n f_b$  where  $m, n = 0, 1, 2, 3$ , etc. Intermodulation terms are those for which neither  $m$  nor  $n$  are equal to zero. For example, the second order terms include  $(f_a + f_b)$  and  $(f_a - f_b)$ , while the third order terms include  $(2f_a + f_b)$ ,  $(2f_a - f_b)$ ,  $(f_a + 2f_b)$  and  $(f_a - 2f_b)$ .

The AD7892 is tested using two input frequencies away from the bottom end of the input bandwidth. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

### Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

### Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

### Positive Full-Scale Error (AD7892-1)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal  $4 \times \text{REF IN} - 3/2 \text{ LSB}$  ( $\pm 10 \text{ V}$  range) or  $2 \times \text{REF IN} - 3/2 \text{ LSB}$  ( $\pm 5 \text{ V}$  range) after the bipolar zero error has been adjusted out.

### Positive Full-Scale Error (AD7892-2)

This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal ( $\text{REF IN} - 3/2 \text{ LSB}$ ) after the unipolar offset error has been adjusted out.

### Positive Full-Scale Error (AD7892-3)

This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal ( $\text{REF IN} - 3/2 \text{ LSB}$ ) after the bipolar zero error has been adjusted out.

### Bipolar Zero Error (AD7892-1, AD7892-3)

This is the deviation of the midscale transition (all 1s to all 0s) from the ideal ( $\text{AGND} - 1/2 \text{ LSB}$ ).

### Unipolar Offset Error (AD7892-2)

This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal ( $\text{AGND} + 1/2 \text{ LSB}$ ).

### Negative Full-Scale Error (AD7892-1)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal  $-4 \times \text{REF IN} + 1/2 \text{ LSB}$  ( $\pm 10 \text{ V}$  range) or  $-2 \times \text{REF IN} + 1/2 \text{ LSB}$  ( $\pm 5 \text{ V}$  range) after bipolar zero error has been adjusted out.

### Negative Full-Scale Error (AD7892-3)

This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal  $-\text{REF IN} + 1/2 \text{ LSB}$  after bipolar zero error has been adjusted out.

### Track/Hold Acquisition Time

Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within  $\pm 1/2 \text{ LSB}$ , after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the  $V_{\text{IN}}$  input of the AD7892. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to  $V_{\text{IN}}$  before starting another conversion, to ensure that the part operates to specification.

## CIRCUIT DESCRIPTION

The AD7892 is a fast, 12-bit single supply A/D converter. It provides the user with signal scaling, track/hold, reference, A/D converter and versatile interface logic functions on a single chip. The signal scaling on the AD7892-1 allows the part to handle either  $\pm 5$  V or  $\pm 10$  V input signals while operating from a single +5 V supply. The AD7892-2 handles a 0 V to +2.5 V analog input range, while signal scaling on the AD7892-3 allows it to handle  $\pm 2.5$  V input signals when operating from a single supply. The part requires a +2.5 V reference which can be provided from the part's own internal reference or from an external reference source.

Conversion is initiated on the AD7892 by pulsing the  $\overline{\text{CONVST}}$  input. On the rising edge of  $\overline{\text{CONVST}}$ , the track/hold goes from track mode to hold mode and the conversion sequence is started. At the end of conversion (falling edge of  $\overline{\text{EOC}}$ ), the track/hold returns to tracking mode and the acquisition time begins. Conversion time for the part is 1.47  $\mu\text{s}$  (AD7892-3) and the track/hold acquisition time is 200 ns (AD7892-3). This allows the AD7892-3 to operate at throughput rates up to 600 kSPS. The AD7892-1 and AD7892-2 are specified with a 1.6  $\mu\text{s}$  conversion and 400 ns acquisition time allowing a throughput rate of 500 kSPS.

### Track/Hold Section

The track/hold amplifier on the AD7892 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track/hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 600 kHz (i.e., the track/hold can handle input frequencies in excess of 300 kHz).

The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 200 ns. The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode on the rising edge of  $\overline{\text{CONVST}}$ . The aperture time for the track/hold (i.e., the delay time between the external  $\overline{\text{CONVST}}$  signal and the track/hold actually going into hold) is typically 15 ns. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track/hold amplifier begins at this point.

### Reference Section

The AD7892 contains a single reference pin, labelled REF OUT/REF IN, which either provides access to the part's own +2.5 V reference or to which an external +2.5 V reference can be connected to provide the reference source for the part. The part is

specified with a +2.5 V reference voltage. Errors in the reference source will result in gain errors in the AD7892's transfer function and will add to the specified full-scale errors on the part. On the AD7892-1 and AD7892-3, it will also result in an offset error injected in the attenuator stage.

The AD7892 contains an on-chip +2.5 V reference. To use this reference as the reference source for the AD7892, simply connect a 0.1  $\mu\text{F}$  disc ceramic capacitor from the REF OUT/REF IN pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7892, it should be buffered as the part has a FET switch in series with the reference output resulting in a source impedance for this output of 5.5 k $\Omega$  nominal. The tolerance on the internal reference is  $\pm 10$  mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of  $\pm 25$  mV.

If the application requires a reference with a tighter tolerance or the AD7892 needs to be used with a system reference, then the user has the option of connecting an external reference to this REF OUT/REF IN pin. The external reference will effectively overdrive the internal reference and thus provide the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current is  $\pm 100$   $\mu\text{A}$ . Suitable reference sources for the AD7892 include the AD680, AD780 and REF43 precision +2.5 V references.

## INTERFACING

The part provides two interface options, a 12-bit parallel interface and a three-wire serial interface. The required interface mode is selected via the MODE pin. The two interface modes are discussed in the following sections.

### Parallel Interface Mode

The parallel interface mode is selected by tying the MODE input to a logic high. Figure 2 shows a timing diagram illustrating the operational sequence of the AD7892. The on-chip track/hold goes into hold mode, and conversion is initiated on the rising edge of the  $\overline{\text{CONVST}}$  signal. When conversion is complete, the end of conversion line ( $\overline{\text{EOC}}$ ) pulses low to indicate that new data is available in the AD7892's output register. This  $\overline{\text{EOC}}$  line can be used to drive an edge-triggered interrupt of a microprocessor. The falling edge of the  $\overline{\text{RD}}$  signal should occur 200 ns prior to the next rising edge of  $\overline{\text{CONVST}}$ .  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  going low accesses the 12-bit conversion result. In systems where the part is interfaced to a gate array or ASIC, this  $\overline{\text{EOC}}$

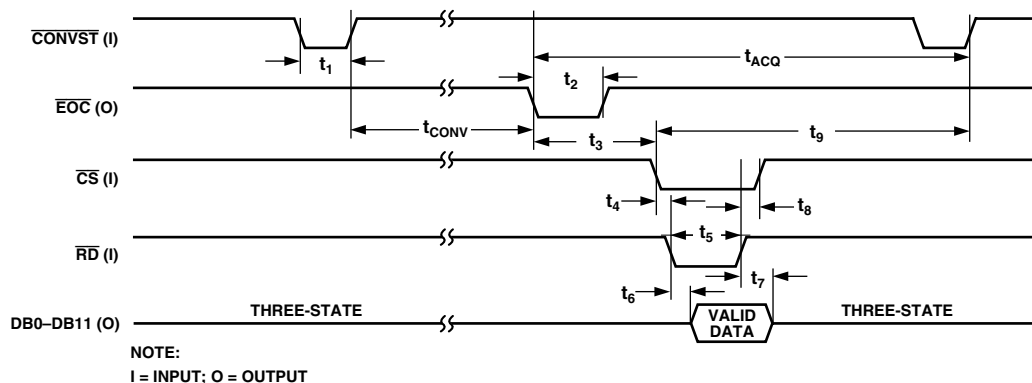


Figure 2. Parallel Mode Timing Diagram

# AD7892

pulse can be applied to the  $\overline{CS}$  and  $\overline{RD}$  inputs to latch data out of the AD7892 and into the gate array or ASIC. This eliminates the logic required in the gate array or ASIC to recognize the end of conversion and generate the read signal for the AD7892. To obtain optimum performance from the AD7892, it is not recommended to tie  $\overline{CS}$  and  $\overline{RD}$  permanently low as this keeps the three-state active during conversion.

## Serial Interface Mode

The AD7892 is configured for serial mode interfacing by tying the MODE input low. It provides for a three-wire, serial link between the AD7892 and industry-standard microprocessors, microcontrollers and digital signal processors. SCLK and  $\overline{RFS}$  of the AD7892 are inputs, and the AD7892's serial interface is designed for direct interface to systems that provide a serial clock input that is synchronized to the serial data output including microcontrollers such as the 80C51, 87C51, 68HC11 and 68HC05 and most digital signal processors.

Figure 3 shows the timing diagram for reading from the AD7892 in the serial interface mode.  $\overline{RFS}$  goes low to access data from the AD7892. The serial clock input does not have to be continuous. The serial data can be accessed in a number of bytes. However,  $\overline{RFS}$  must remain low for the duration of the data transfer operation. Sixteen bits of data are transmitted with four leading zeros followed by the 12-bit conversion result starting with the MSB. Serial data is clocked out of the device on the rising edge of SCLK. Old data is guaranteed to be valid for 5 ns after this edge. This is useful for high speed serial clocks where the access time of the part would not allow sufficient set-up time for the data to be accepted on the falling edge of the clock. In this case, care must be taken that  $\overline{RFS}$  does not go just prior to a rising edge of SCLK. For slower serial clocks data is valid on the falling edge of SCLK. At the end of the read operation, the  $\overline{SDATA}$  line is three-stated by a rising edge on either the SCLK or  $\overline{RFS}$  inputs, whichever occurs first. Serial data cannot be read during conversion to avoid feedthrough problems from the serial clock to the conversion process. For optimum performance of the AD7892-3, a serial read should also be avoided within 200 ns of the rising edge of  $\overline{CONVST}$  to avoid feedthrough into the track/hold during its acquisition time. The serial read should, therefore, occur between the end of conversion ( $\overline{EOC}$  falling edge) and 200 ns prior to the next rising edge of

$\overline{CONVST}$ . For the AD7892-1 and AD7892-2, a serial read should also be avoided within 400 ns of the rising edge of  $\overline{CONVST}$ . This limits the maximum achievable throughput rate in serial mode (assuming 20 MHz serial clock) to 400 kSPS for the AD7892-3 and 357 kSPS for the AD7892-1 and AD7892-2.

## Analog Input Section

The AD7892 is offered as three part types allowing for four different analog input voltage ranges. The AD7892-1 handles either  $\pm 5$  V or  $\pm 10$  V input voltage ranges. The AD7892-2 handles a 0 V to +2.5 V input voltage range while the AD7892-3 handles an input range of  $\pm 2.5$  V.

### AD7892-1

Figure 4 shows the analog input section for the AD7892-1. The analog input range is pin-strappable (using  $V_{IN2}$ ) for either  $\pm 5$  V or  $\pm 10$  V on the  $V_{IN1}$  input. With  $V_{IN2}$  connected to AGND, the input range on  $V_{IN1}$  is  $\pm 10$  V, and the input resistance on  $V_{IN1}$  is 15 k $\Omega$  nominal. With  $V_{IN2}$  connected to  $V_{IN1}$ , the input range on  $V_{IN1}$  is  $\pm 5$  V, and the input resistance on  $V_{IN1}$  is 8 k $\Omega$  nominal. As a result, the  $V_{IN1}$  and  $V_{IN2}$  inputs should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to  $\pm 17$  V without damaging the AD7892-1.

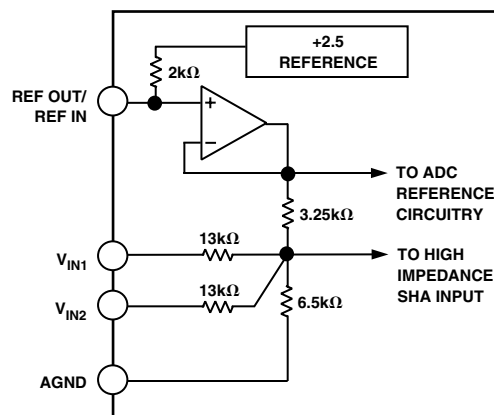


Figure 4. AD7892-1 Analog Input Structure

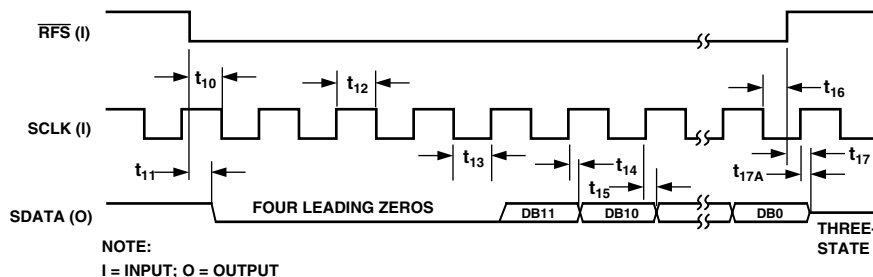


Figure 3. Serial Mode Timing Diagram

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is two's complement binary with 1 LSB = FSR/4096 = 20 V/4096 = 4.88 mV for the ±10 V range and 1 LSB = FSR/4096 = 10 V/4096 = 2.44 mV for the ±5 V range. The ideal input/output transfer function for the AD7892-1 is shown in Table I.

### AD7892-2

The analog input section for the AD7892-2 contains no biasing resistors. The analog input looks directly into the track/hold input stage. The analog input range on the  $V_{IN1}$  input is 0 V to +2.5 V. The  $V_{IN2}$  input can be left unconnected but if it is connected to a potential then that potential must be AGND. The  $V_{IN1}$  input connects directly to the input sampling capacitor of the AD7892-2's track/hold. The value of this input sampling capacitor is nominally 10 pF.

Once again, the designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is straight (natural) binary with 1 LSB = FSR/4096 = 2.5 V/4096 = 0.61 mV. The ideal input/output transfer function for the AD7892-2 is shown in Table II.

**Table I. Ideal Input/Output Code Table for the AD7892-1**

Analog Input	Digital Output Code Transition
+FSR/2 – 3/2 LSB <sup>1,2</sup> (9.99268 or 4.99634) <sup>3</sup>	011 ... 110 to 011 ... 111
+FSR/2 – 5/2 LSBs (9.98779 or 4.99390)	011 ... 101 to 011 ... 110
+FSR/2 – 7/2 LSBs (9.98291 or 4.99146)	011 ... 100 to 011 ... 101
AGND + 3/2 LSB (0.00732 or 0.00366)	000 ... 001 to 000 ... 010
AGND + 1/2 LSB (0.00244 or 0.00122)	000 ... 000 to 000 ... 001
AGND – 1/2 LSB (–0.00244 or –0.00122)	111 ... 111 to 000 ... 000
AGND – 3/2 LSB (–0.00732 or –0.00366)	111 ... 110 to 111 ... 111
–FSR/2 + 5/2 LSB (–9.98779 or –4.99390)	100 ... 010 to 100 ... 011
–FSR/2 + 3/2 LSB (–9.99268 or –4.99634)	100 ... 001 to 100 ... 010
–FSR/2 + 1/2 LSB (–9.99756 or –4.99878)	100 ... 000 to 100 ... 001

**NOTES**

<sup>1</sup>FSR is full-scale range and REF IN = +2.5 V, is 20 V for the ±10 V range and 10 V for the ±5 V range.

<sup>2</sup>1 LSB = FSR/4096 = 4.88 mV (±10 V range) and 2.44 mV (±5 V range) with REF IN = +2.5 V.

<sup>3</sup>±10 V range or ±5 V range.

**Table II. Ideal Input/Output Code Table for the AD7892-2**

Analog Input	Digital Output Code Transition
+FSR – 3/2 LSB <sup>1,2</sup> (2.499084 V)	111 ... 110 to 111 ... 111
+FSR – 5/2 LSBs (2.498474 V)	111 ... 110 to 111 ... 110
+FSR – 7/2 LSBs (2.497864 V)	111 ... 100 to 111 ... 101
AGND + 5/2 LSB (0.001526 V)	000 ... 010 to 010 ... 011
AGND + 3/2 LSB (0.00916 V)	000 ... 001 to 001 ... 010
AGND + 1/2 LSB (0.000305 V)	000 ... 000 to 000 ... 001

**NOTES**

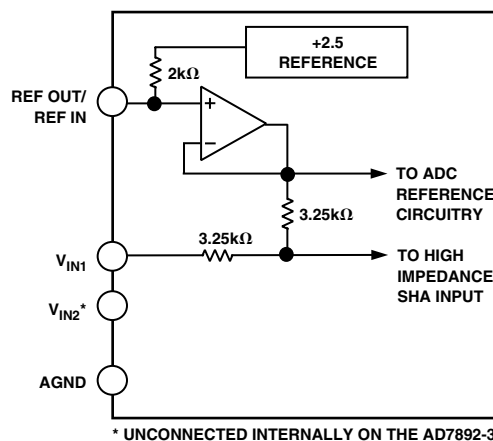
<sup>1</sup>FSR is full-scale range and is 2.5 V with REF IN = +2.5 V.

<sup>2</sup>1 LSB = FSR/4096 = 0.61 mV with REF IN = +2.5 V.

### AD7892-3

Figure 5 shows the analog input section for the AD7892-3. The analog input range is ±2.5 V on the  $V_{IN1}$  input. The  $V_{IN2}$  input can be left unconnected but if it is connected to a potential then that potential must be AGND. The input resistance on the  $V_{IN1}$  is 1.8 kΩ nominal. As a result, the  $V_{IN1}$  input should be driven from a low impedance source. The resistor attenuator stage is followed by the high input impedance stage of the track/hold amplifier. This resistor attenuator stage allows the input voltage to go to ±7 V without damaging the AD7892-3.

The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs). Output coding is two's complement binary with 1 LSB = FSR/4096 = 5 V/4096 = 1.22 mV with REF IN = +2.5 V. The ideal input/output transfer function for the AD7892-3 is shown in Table III.



**Figure 5. AD7892-3 Analog Input Structure**

**Table III. Ideal Input/Output Code Table for the AD7892-3**

Analog Input	Digital Output Code Transition
+FSR/2 – 3/2 LSB <sup>1,2</sup> (2.49817)	011 ... 110 to 011 ... 111
+FSR/2 – 5/2 LSBs (2.49695)	011 ... 110 to 011 ... 110
+FSR/2 – 7/2 LSBs (2.49573)	011 ... 110 to 011 ... 101
AGND + 3/2 LSB (0.00183)	000 ... 001 to 000 ... 010
AGND + 1/2 LSB (0.00061)	000 ... 000 to 000 ... 001
AGND – 1/2 LSB (–0.00061)	111 ... 111 to 000 ... 000
AGND – 3/2 LSB (–0.00183)	111 ... 110 to 111 ... 111
–FSR/2 + 5/2 LSB (–2.49695)	100 ... 010 to 100 ... 011
–FSR/2 + 3/2 LSB (–2.49817)	100 ... 001 to 100 ... 010
–FSR/2 + 1/2 LSB (–2.49939)	100 ... 000 to 100 ... 001

**NOTES**

<sup>1</sup>FSR is full-scale range and is 5 V with REF IN = +2.5 V.

<sup>2</sup>1 LSB = FSR/4096 = 1.22 mV with REF IN = +2.5 V.

# AD7892

## MICROPROCESSOR INTERFACING

The AD7892 features both high speed parallel and serial interfaces, allowing considerable flexibility in interfacing to microprocessor systems. To obtain optimum performance from the part, data should not be read during conversion and this limits the achievable throughput rate in serial mode to 400 kSPS for the AD7892-3.

Figures 6, 7 and 9 show some typical interface circuits between the AD7892 and popular DSP processors. Figure 8 shows an interface between the part and a gate array or ASIC where data is clocked into the ASIC by the AD7892 itself at the end of conversion. In all cases, the CONVST signal is generated from an external timer to ensure equidistant sampling.

### AD7892 to ADSP-2101 Interface

Figure 6 shows a parallel interface between the AD7892 and the ADSP-2101 DSP processor. CONVST starts conversion and at the end of conversion the falling edge of the EOC output provides an interrupt request to the ADSP-2101.

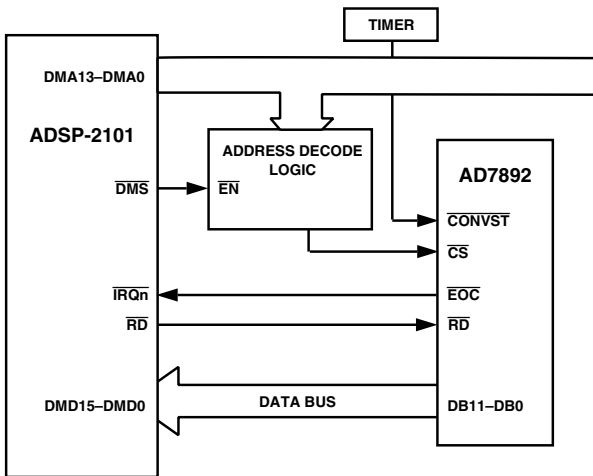


Figure 6. AD7892 to ADSP-2101

### AD7892 to TMS320C25 Interface

Figure 7 shows a parallel interface between the AD7892 and the TMS320C25 DSP processor. CONVST starts conversion and at the end of conversion the falling edge of the EOC output provides an interrupt request to the TMS320C25.

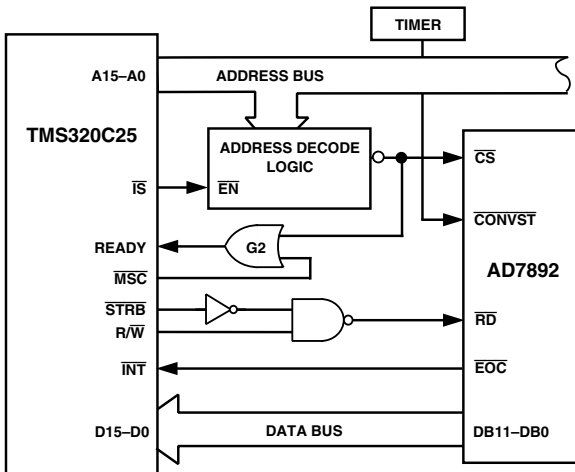


Figure 7. AD7892 to TMS320C25 Interface

### EOC Pulse Provides CS and RD

Figure 8 shows a parallel interface between the AD7892 and a gate array or ASIC. CONVST starts conversion and at the end of conversion the falling edge of the EOC output provides the CS and RD pulse to latch data out of the AD7892 and into the gate array/ASIC. This scheme allows for the fastest possible throughput rate with the part as no time is lost in interrupt service routines and as soon as data is available from the part it is transferred out of it.

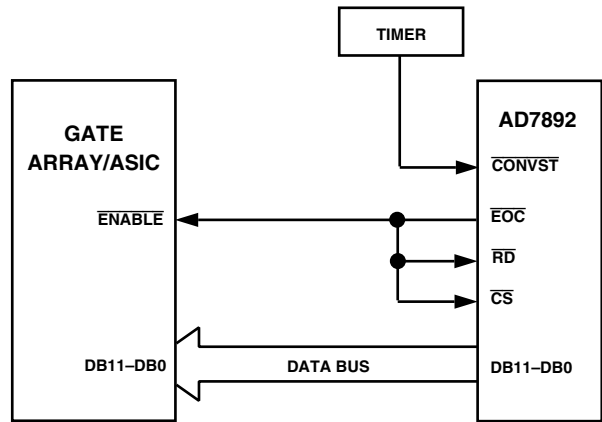


Figure 8. AD7892 to Gate Array/ASIC Interface

### AD7892 to DSP56000 Interface

Figure 9 shows a serial interface between the AD7892 and the DSP56000 DSP processor. CONVST starts conversion and at the end of conversion the falling edge of the EOC output provides an interrupt request to the DSP56000.

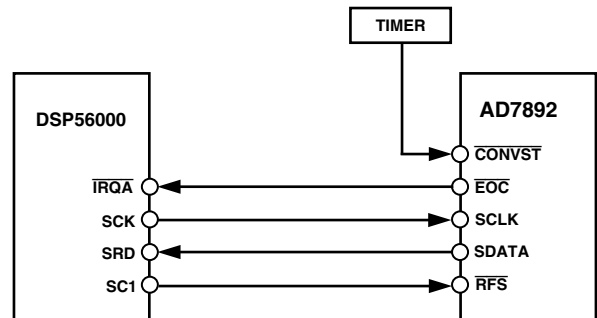


Figure 9. AD7892 to DSP56000 Interface

### Grounding and Layout

The AD7892 has a single supply voltage pin,  $V_{DD}$ , which supplies both the analog and digital circuitry on the part. For optimum performance from the part, it is recommended that this +5 V is taken from the +5 V analog supply in the system. The analog and digital grounds to the AD7892 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The part exhibits good immunity to noise on the supplies but care must still be taken with regard to grounding and layout especially when using switching mode supplies.

The printed circuit board which houses the AD7892 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD7892 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7892. If the AD7892 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7892.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7892 to avoid noise coupling. The power supply lines to the AD7892 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10  $\mu\text{F}$  tantalum in parallel with 0.1  $\mu\text{F}$  capacitors to AGND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1  $\mu\text{F}$  disc ceramic capacitors to DGND. It is recommended that the system's  $AV_{DD}$  supply is used to supply the  $V_{DD}$  for the AD7892. This supply should have the recommended analog supply decoupling capacitors between the  $V_{DD}$  pin of the AD7892 and AGND and the recommended digital supply decoupling capacitor between the  $V_{DD}$  pin of the AD7892 and DGND.

### Evaluating the AD7892 Performance

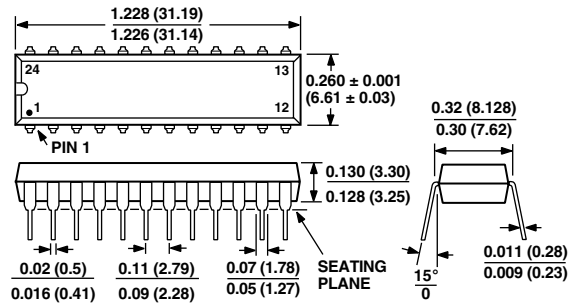
The recommended layout for the AD7892 is outlined in the evaluation board for the AD7892. The evaluation board package includes a fully assembled and tested evaluation board, documentation and software for controlling the board from a PC using the EVAL-CONTROL BOARD. The EVAL-CONTROL BOARD can be used in conjunction with the AD7892 evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator. Using the EVAL-CONTROL BOARD with the AD7892 evaluation board allows the user to evaluate the ac and dc performance of the AD7892 on a PC.

The software provided with the evaluation board allows the user to perform ac (Fast Fourier Transform) and dc (histogram of codes) tests on the AD7892. The evaluation board can also be used in a stand-alone fashion without the EVAL-CONTROL BOARD but in this case, the user has to write their own software to evaluate the part. There are two versions of the evaluation board available, one for the AD7892-2 and one for the AD7892-3. To order the AD7892-2 evaluation board, the order number is EVAL-AD7892-2CB and to order the AD7892-3 evaluation board, the order number is EVAL-AD7892-3CB.

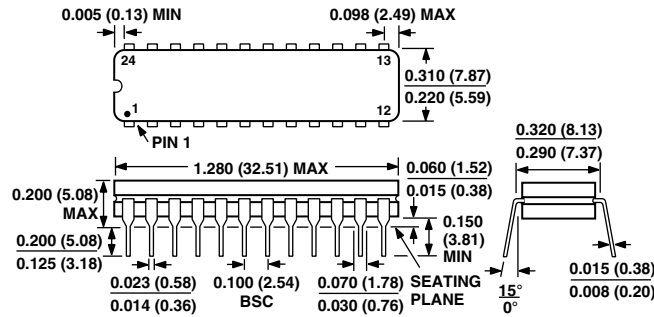
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**Plastic DIP (N-24)**



**Cerdip (Q-24)**



**SOIC (R-24)**

