Network Clock Generator, Two Outputs

AD9575

FEATURES

Fully integrated VCO/PLL core
0.39 ps rms jitter from 12 kHz to 20 MHz at 156.25 MHz
0.15 ps rms jitter from 1.875 MHz to 20 MHz at 156.25 MHz
0.40 ps rms jitter from 12 kHz to 20 MHz at 106.25 MHz
0.15 ps rms jitter from 637 kHz to 10 MHz at 106.25 MHz
Input crystal frequency of 19.44 MHz, 25 MHz, or 25.78125 MHz
Pin selectable divide ratios for 33.33 MHz, 62.5 MHz, 100 MHz, 106.25 MHz, 125 MHz, 155.52 MHz, 156.25 MHz, 159.375 MHz, 161.13 MHz, and 312.5 MHz outputs
LVDS/LVPECL/LVCMOS output format
Integrated loop filter
Space saving 4.4 mm × 5.0 mm TSSOP
100 mA power supply current (LVDS output)
120 mA power supply current (LVPECL output)
3.3 V operation

APPLICATIONS

GbE/FC/SONET line cards, switches, and routers
CPU/PCI-E applications
Low jitter, low phase noise clock generation

GENERAL DESCRIPTION

The AD9575 provides a highly integrated, dual output clock generator function including an on-chip PLL core that is optimized for network clocking. The integer-N PLL design is based on the Analog Devices, Inc., proven portfolio of high performance, low jitter frequency synthesizers to maximize line card performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a low noise phase frequency detector (PFD), a precision charge pump (CP), a low phase noise voltage controlled oscillator (VCO), and pin selectable feedback and output dividers.

By connecting an external crystal, popular network output frequencies can be locked to the input reference. The output divider and feedback divider ratios are pin programmable for the required output rates. No external loop filter components are required, thus conserving valuable design time and board space.

The AD9575 is available in a 16-lead, 4.4 mm × 5.0 mm TSSOP and can be operated from a single 3.3 V supply. The temperature range is −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

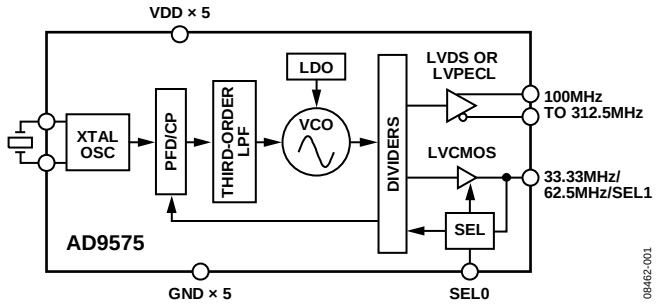

Figure 1.

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COMPARABLE PARTS

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EVALUATION KITS

- AD9575 Evaluation Board

DOCUMENTATION

Data Sheet

- AD9575: Network Clock Generator, Two Outputs Data Sheet

DESIGN RESOURCES

- AD9575 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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DOCUMENT FEEDBACK

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1/10—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) values are given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over the full V_S and T_A (−40°C to +85°C) variation.

PLL CHARACTERISTICS

Table 1.

	LVDS			LVCMOS			LVPECL			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
PHASE NOISE CHARACTERISTICS										
PLL Noise (100 MHz Output)										
At 1 kHz		−123						−122		dBc/Hz
At 10 kHz		−128						−129		dBc/Hz
At 100 kHz		−131						−131		dBc/Hz
At 1 MHz		−150						−151		dBc/Hz
At 10 MHz		−156						−158		dBc/Hz
At 30 MHz		−156						−158		dBc/Hz
PLL Noise (106.25 MHz Output)										
At 1 kHz		−121						−121		dBc/Hz
At 10 kHz		−127						−128		dBc/Hz
At 100 kHz		−130						−130		dBc/Hz
At 1 MHz		−149						−150		dBc/Hz
At 10 MHz		−156						−158		dBc/Hz
At 30 MHz		−156						−159		dBc/Hz
PLL Noise (125 MHz Output)										
At 1 kHz		−120						−120		dBc/Hz
At 10 kHz		−126						−127		dBc/Hz
At 100 kHz		−128						−129		dBc/Hz
At 1 MHz		−148						−150		dBc/Hz
At 10 MHz		−155						−157		dBc/Hz
At 30 MHz		−156						−158		dBc/Hz
PLL Noise (155.52 MHz Output)										
At 1 kHz		−118						−118		dBc/Hz
At 10 kHz		−123						−123		dBc/Hz
At 100 kHz		−125						−125		dBc/Hz
At 1 MHz		−147						−149		dBc/Hz
At 10 MHz		−155						−157		dBc/Hz
At 30 MHz		−156						−157		dBc/Hz
PLL Noise (156.25 MHz Output)										
At 1 kHz		−118						−118		dBc/Hz
At 10 kHz		−124						−125		dBc/Hz
At 100 kHz		−126						−127		dBc/Hz
At 1 MHz		−146						−148		dBc/Hz
At 10 MHz		−155						−157		dBc/Hz
At 30 MHz		−155						−157		dBc/Hz
PLL Noise (159.375 MHz Output)										
At 1 kHz		−118						−118		dBc/Hz
At 10 kHz		−124						−125		dBc/Hz
At 100 kHz		−126						−126		dBc/Hz
At 1 MHz		−146						−147		dBc/Hz
At 10 MHz		−155						−156		dBc/Hz
At 30 MHz		−155						−157		dBc/Hz

Parameter	LVDS Min	LVDS Typ	LVDS Max	LVCMOS Min	LVCMOS Typ	LVCMOS Max	LVPECL Min	LVPECL Typ	LVPECL Max	Unit
PLL Noise (161.132812 MHz Output)										
At 1 kHz		−118						−119		dBc/Hz
At 10 kHz		−122						−123		dBc/Hz
At 100 kHz		−126						−126		dBc/Hz
At 1 MHz		−144						−146		dBc/Hz
At 10 MHz		−154						−156		dBc/Hz
At 30 MHz		−155						−156		dBc/Hz
PLL Noise (312.5 MHz Output)										
At 1 kHz		−112						−112		dBc/Hz
At 10 kHz		−119						−119		dBc/Hz
At 100 kHz		−120						−120		dBc/Hz
At 1 MHz		−140						−142		dBc/Hz
At 10 MHz		−152						−154		dBc/Hz
At 30 MHz		−153						−155		dBc/Hz
PLL Noise (33.33 MHz Output)										
At 1 kHz					−131					dBc/Hz
At 10 kHz					−138					dBc/Hz
At 100 kHz					−140					dBc/Hz
At 1 MHz					−155					dBc/Hz
At 5 MHz					−155					dBc/Hz
PLL Noise (62.5 MHz Output)										
At 1 kHz					−126					dBc/Hz
At 10 kHz					−133					dBc/Hz
At 100 kHz					−134					dBc/Hz
At 1 MHz					−150					dBc/Hz
At 5 MHz					−152					dBc/Hz
Spurious Content		−70						−70		dBc
PLL Figure of Merit		−217						−217		dBc/Hz

LVDS CLOCK OUTPUT JITTER (TYP/MAX)

Typical (typ) values are given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Maximum (max) values are given over the full V_S and T_A (−40°C to +85°C) variation.

Table 2.

Jitter Integration Bandwidth	100 MHz	106.25 MHz	125 MHz	155.52 MHz	156.25 MHz	159.375 MHz	161.13 MHz	312.5 MHz	Unit
12 kHz to 20 MHz	0.38/0.50	0.40/0.54	0.37/0.47	0.41/0.54	0.39/0.51	0.38/0.51	0.44/0.61	0.36/0.48	ps rms
1.875 MHz to 20 MHz					0.15/0.27				ps rms
637 kHz to 10 MHz		0.15/0.21							ps rms

LVPECL CLOCK OUTPUT JITTER (TYP/MAX)

Typical (typ) values are given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Maximum (max) values are given over the full V_S and T_A (−40°C to +85°C) variation.

Table 3.

Jitter Integration Bandwidth	100 MHz	106.25 MHz	125 MHz	155.52 MHz	156.25 MHz	159.375 MHz	161.13 MHz	312.5 MHz	Unit
12 kHz to 20 MHz	0.36/0.46	0.44/0.68	0.36/0.45	0.40/0.52	0.39/0.64	0.41/0.62	0.43/0.69	0.38/0.49	ps rms
1.875 MHz to 20 MHz					0.19/0.54				ps rms
637 kHz to 10 MHz		0.22/0.35							ps rms

OUTPUT FREQUENCY SELECT

Minimum (min) and maximum (max) values are given over the full V_S and T_A (−40°C to +85°C) variation.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Select Pins (SEL0/SEL1)					
Logic 1 Voltage	$0.83 \times V_S + 0.2$			V	
Logic 0 Voltage			$0.33 \times V_S - 0.2$	V	
Logic 1 Current			190	µA	Pull-up to V_S
Logic 0 Current			150	µA	Pull-down to GND

CLOCK OUTPUTS

Typical (typ) values are given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over the full V_S and T_A (−40°C to +85°C) variation.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS CLOCK OUTPUT					Termination = 100 Ω differential; default
Output Frequency			312.5	MHz	
Differential Output Voltage (V_{OD})	250	340	450	mV	See Figure 2 for definition
Delta V_{OD}			25	mV	
Output Offset Voltage (V_{OS})	1.125	1.25	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
Duty Cycle	45	50	55	%	
LVPECL CLOCK OUTPUT					
Output Frequency			312.5	MHz	
Output High Voltage (V_{OH})	$V_S - 1.5$	$V_S - 1.05$	$V_S - 0.8$	V	
Output Low Voltage (V_{OL})	$V_S - 2.5$	$V_S - 1.75$	$V_S - 1.7$	V	
Differential Output Voltage (V_{OD})	430	640	800	mV	See Figure 2 for definition
Duty Cycle	45	50	55	%	
LVCMOS CLOCK OUTPUT					
Output Frequency			62.5	MHz	
Output High Voltage (V_{OH})	$V_S - 0.1$			V	
Output Low Voltage (V_{OL})			0.1	V	
Duty Cycle	45	50	55	%	

TIMING CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS					Termination = 100 Ω differential; C_{LOAD} = 0 pF; C_{AC} = 0.1 µF
Output Rise Time, t_{RL}	150	200	300	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}	150	200	300	ps	80% to 20%, measured differentially
LVPECL					Termination = 200 Ω to GND; C_{LOAD} = 0 pF; C_{AC} = 0.1 µF
Output Rise Time, t_{RL}	180	250	300	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}	180	250	300	ps	80% to 20%, measured differentially
LVCMOS					Termination = 50 Ω to 0 V; C_{LOAD} = 5 pF; C_{AC} = 0.1 µF
Output Rise Time, t_{RC}	0.50	0.70	1.10	ns	20% to 80%
Output Fall Time, t_{FC}	0.50	0.70	1.10	ns	80% to 20%

POWER

Table 7.

Parameter	Min	Typ	Max	Unit
POWER SUPPLY	3.0	3.3	3.6	V
POWER SUPPLY CURRENT				
LVDS		100	130	mA
LVPECL		120	160	mA

CRYSTAL OSCILLATOR

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL SPECIFICATION					Parallel resonant/fundamental mode
Frequency	19.44	25	25.78125	MHz	
ESR			40	Ω	
Load Capacitance		14		pF	Cx/2 (see Figure 24) + parasitic capacitance
Phase Noise		−138		dBc/Hz	At 1 kHz offset
Stability	−30		+30	ppm	

TIMING DIAGRAMS

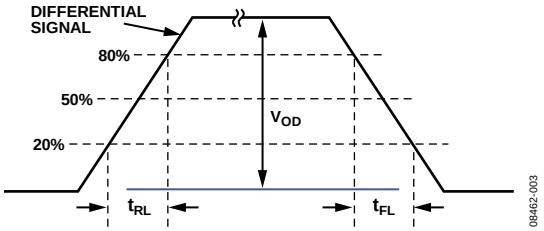


Figure 2. LVDS or LVPECL Timing and Differential Amplitude

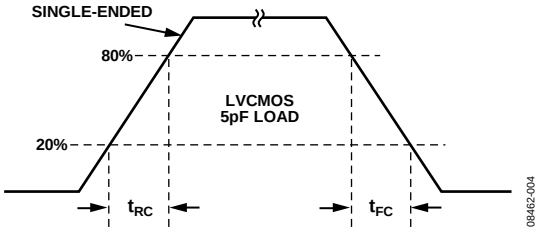


Figure 3. LVCMOS Timing

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
VDD, VDDA, VDDX, VDD_CMOS to GND	−0.3 V to +3.6 V
XO1, XO2 to GND	−0.3 V to V_S + 0.3 V
LVDS/LVPECL OUT, $\overline{\text{LVDS/LVPECL OUT}}$, CMOS OUT/SEL1, SEL0 to GND	−0.3 V to V_S + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 10 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 10. Thermal Resistance[1]

Package Type	θ_{JA}	Unit
16-Lead TSSOP (RU-16)	90.3	°C/W

[1] Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

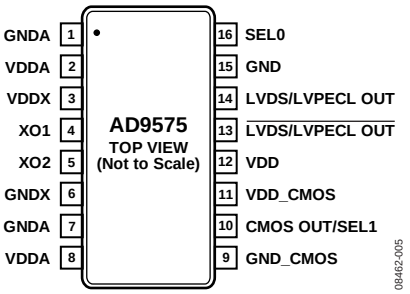


Figure 4. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GNDA	Analog Ground.
2, 8	VDDA	Analog Power Supply (3.3 V).
3	VDDX	Crystal Oscillator Power Supply.
4, 5	XO1, XO2	External Crystal.
6	GNDX	Crystal Oscillator Ground.
9	GND_CMOS	Ground for LVCMOS Output.
10	CMOS OUT/SEL1	LVCMOS Output/Output Frequency Select.
11	VDD_CMOS	Power Supply for LVCMOS Output.
12	VDD	Power Supply for LVDS or LVPECL Output.
13	$\overline{\text{LVDS/LVPECL OUT}}$	Complementary LVDS or LVPECL Output.
14	LVDS/LVPECL OUT	LVDS or LVPECL Output.
15	GND	Ground for LVDS or LVPECL Output.
16	SEL0	Output Frequency Select.

Table 12. Output Frequency Selection[1]

Mode	XTAL	SEL0	SEL1	LVDS/LVPECL Output	LVCMOS Output
1	25 MHz	GND	X[2]	100 MHz	33.33 MHz
2	25 MHz	V_S	GND	156.25 MHz	High-Z
3	25.78125 MHz	V_S	GND	161.13 MHz	High-Z
4	25 MHz	No connect	X[2]	125 MHz	62.5 MHz
5	25 MHz	15 kΩ pull-up	V_S	159.375 MHz	High-Z
6	25 MHz	15 kΩ pull-up	GND	312.5 MHz	High-Z
7	25 MHz	V_S	V_S	106.25 MHz	High-Z
8	19.44 MHz	V_S	No connect	155.52 MHz	High-Z

[1] The AD9575 must be power-cycled if the select pin voltages are altered.
[2] X = in Mode 1, Pin 10 is configured as an LVCMOS output (33.33 MHz) by forcing Pin 16 to GND. In Mode 4, Pin 10 is configured as an LVCMOS output (62.5 MHz) by leaving Pin 16 unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

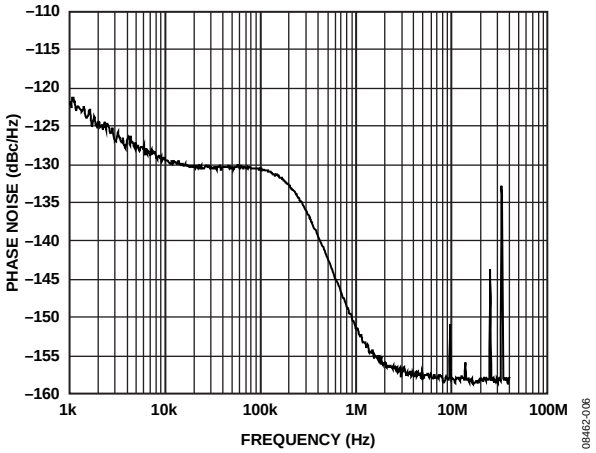


Figure 5. Phase Noise at LVPECL, 100 MHz Clock Output

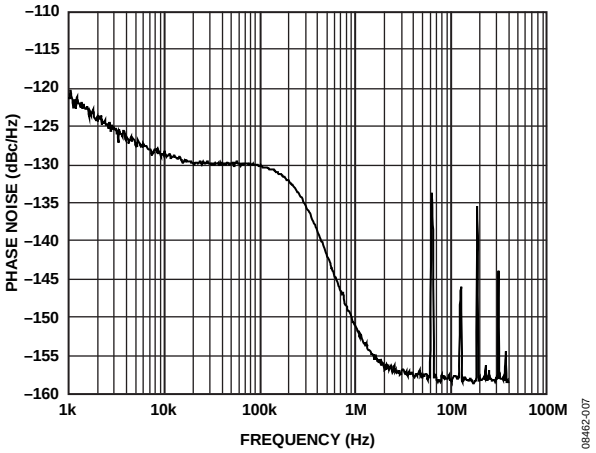


Figure 6. Phase Noise at LVPECL, 106.25 MHz Clock Output

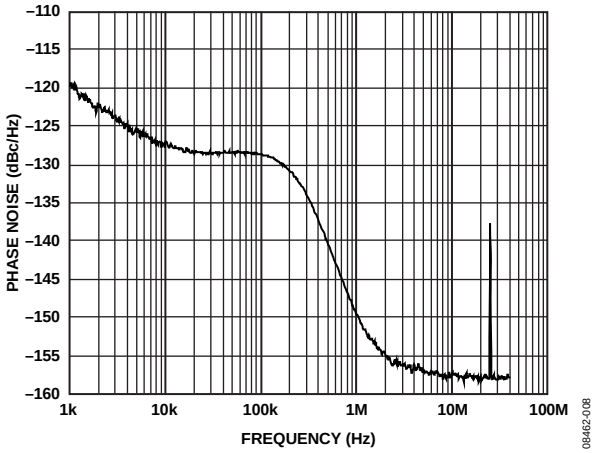


Figure 7. Phase Noise at LVPECL, 125 MHz Clock Output

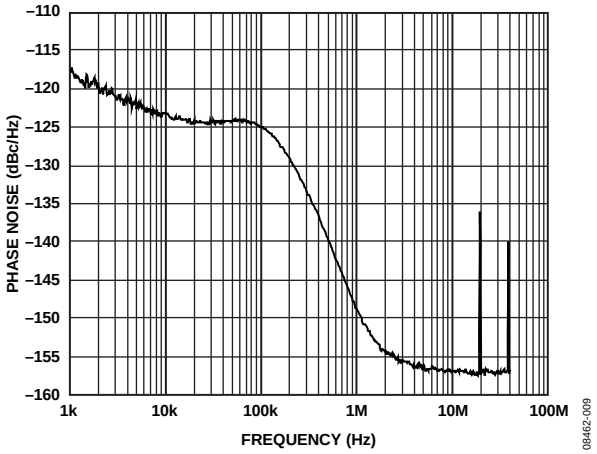


Figure 8. Phase Noise at LVPECL, 155.52 MHz Clock Output

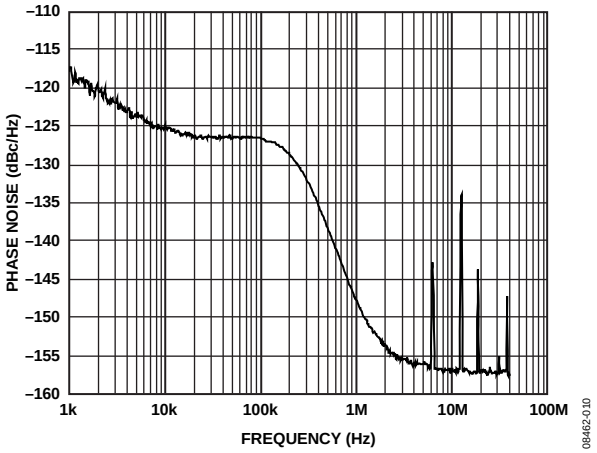


Figure 9. Phase Noise at LVPECL, 156.25 MHz Clock Output

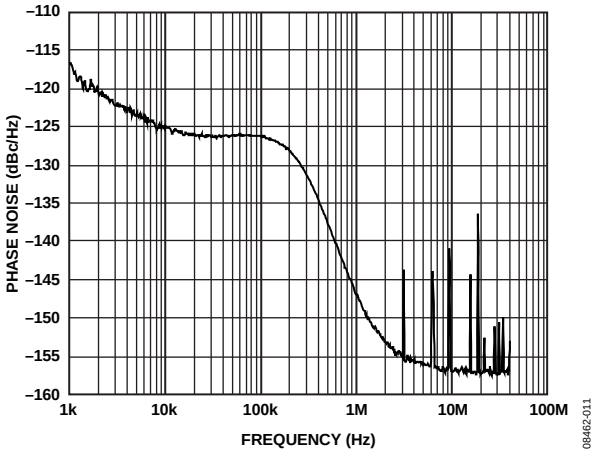


Figure 10. Phase Noise at LVPECL, 159.375 MHz Clock Output

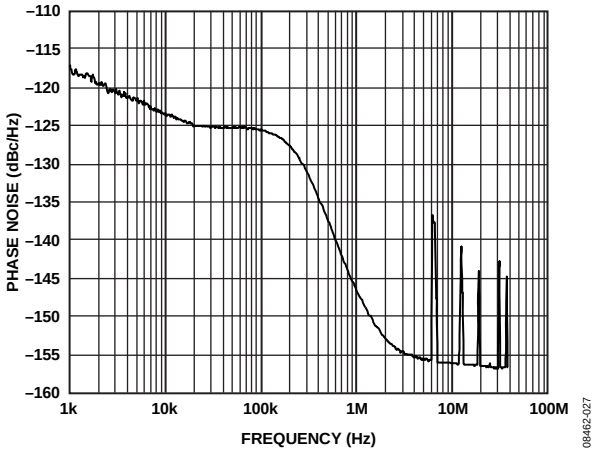


Figure 11. Phase Noise at LVPECL, 161.13 MHz Clock Output

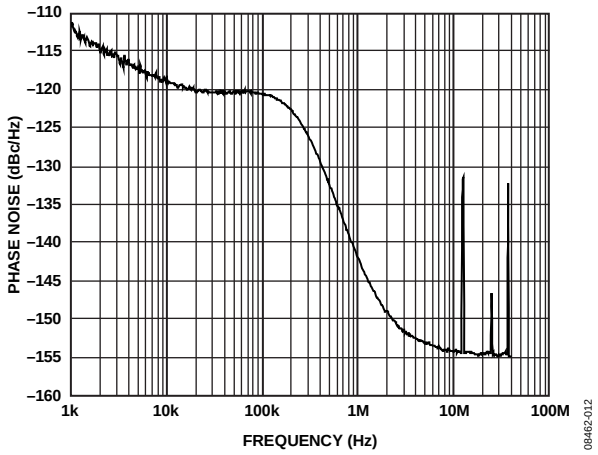


Figure 12. Phase Noise at LVPECL, 312.5 MHz Clock Output

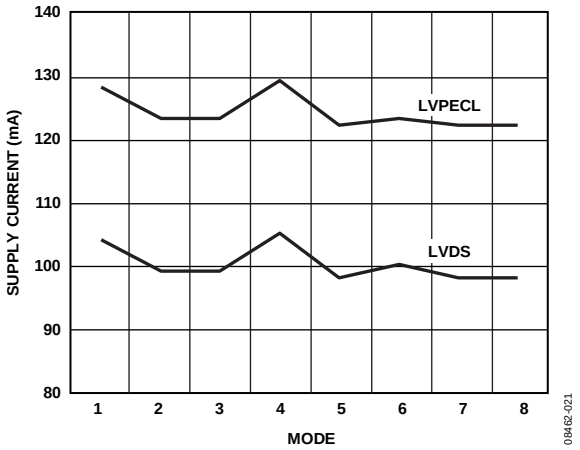


Figure 13. Typical Supply Current vs. Mode (see Table 12)

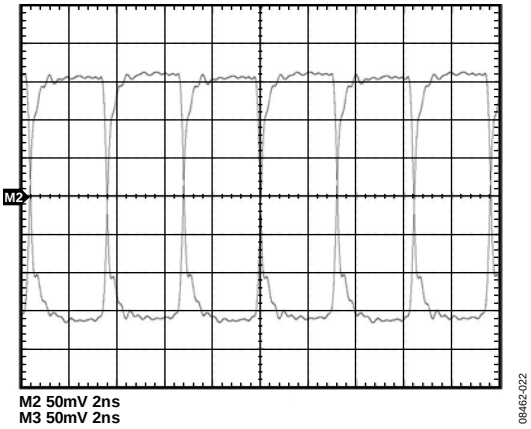


Figure 14. 156.25 MHz LVDS Output

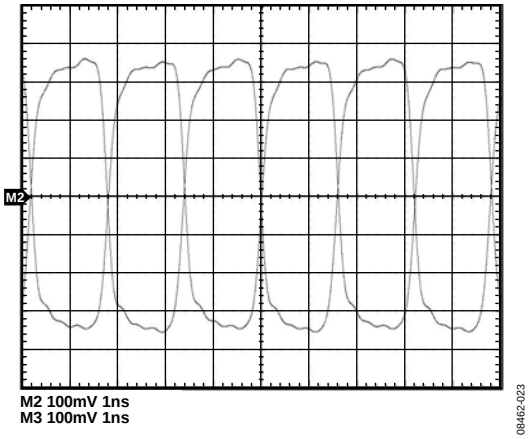


Figure 15. 312.5 MHz LVPECL Output

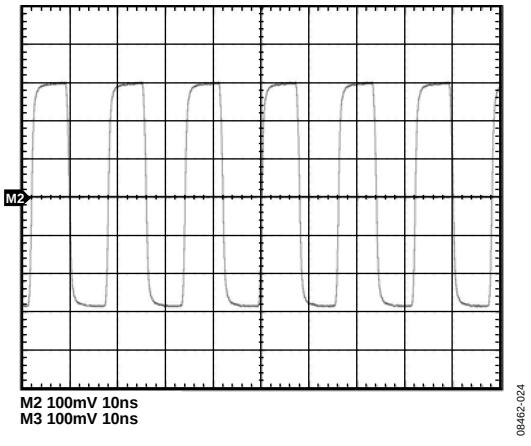


Figure 16. 62.5 MHz LVCMOS Output

TERMINOLOGY

Phase Jitter
An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise
It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on error rate performance by increasing eye closure at the transmitter output and reducing the jitter tolerance/sensitivity of the receiver.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Additive Phase Noise
Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device affects the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter
Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device affects the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

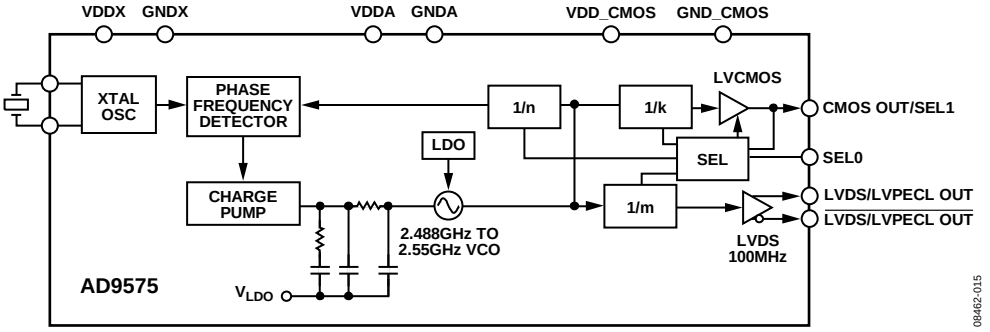


Figure 17. Detailed Block Diagram

Figure 17 shows a block diagram of the AD9575. The chip features a PLL core, which is configured to generate the specific clock frequencies via pin programming. By appropriate connection of the select pins, SEL0 and SEL1, the divide ratios of the feedback divider (n), LVDS output divider (m), and LVCMOS output divider (k) can be programmed (see Table 12). In Mode 1 and Mode 4, Pin 10 is configured as an LVCMOS output by forcing Pin 16 to GND (33.33 MHz output) or by leaving Pin 16 unconnected (62.5 MHz output). In conjunction with a band-select VCO that operates over the range of 2.488 GHz to 2.55 GHz, a wide range of popular network reference frequencies can be generated. This PLL is based on proven Analog Devices synthesizer technology, noted for its exceptional phase noise performance. The AD9575 is highly integrated and includes the loop filter, a regulator for supply noise immunity, all the necessary dividers, output buffers, and a crystal oscillator. A user need only supply an external crystal to implement a clocking solution that requires no processor intervention.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the reference clock and feedback divider to produce an output proportional to the phase and frequency difference between them. Figure 18 shows a simplified schematic.

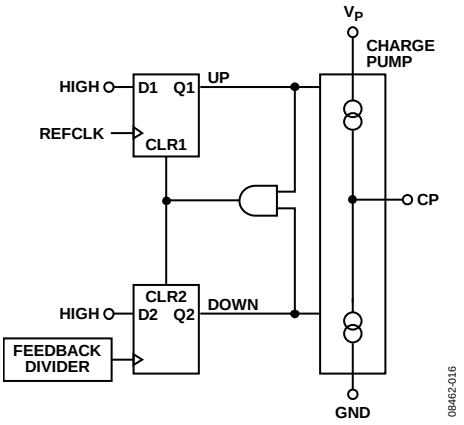


Figure 18. PFD Simplified Schematic

POWER SUPPLY

The AD9575 requires a 3.3 V ± 10% power supply for V_S. The Specifications section gives the performance expected from the AD9575 with the power supply voltage within this range. The absolute maximum range of −0.3 V to +3.6 V, with respect to GND, must never be exceeded on the VDD, VDDA, VDDX, and VDD_CMOS pins.

Good engineering practice should be followed in the layout of power supply traces and the ground plane of the PCB. The power supply should be bypassed on the PCB with adequate capacitance (>10 µF). The AD9575 should be bypassed with adequate capacitors (0.1 µF) at all power pins as close as possible to the part. The layout of the AD9575 evaluation board is a good example.

LVPECL CLOCK DISTRIBUTION

Because they are open emitter, the LVPECL outputs require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 19 shows the LVPECL output stage.

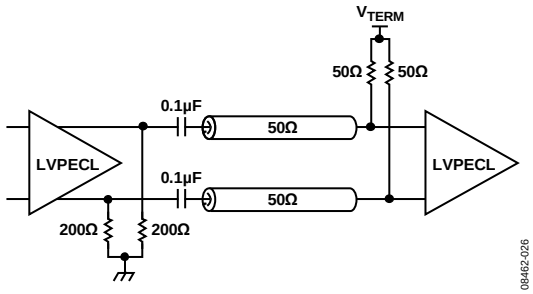


Figure 19. LVPECL AC-Coupled Termination

In most applications, a standard LVPECL far-end termination is recommended, as shown in Figure 20. The resistor network is designed to match the transmission line impedance (50 Ω) and the desired switching threshold (1.3 V).

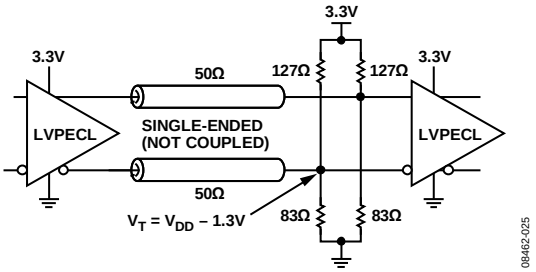


Figure 20. LVPECL Far-End Termination

LVDS CLOCK DISTRIBUTION

The AD9575 is also available with low voltage differential signaling (LVDS) outputs. LVDS uses a current mode output stage with a factory programmed current level. The normal value (default) for this current is 3.5 mA, which yields a 350 mV output swing across a 100 Ω resistor. The LVDS outputs meet or exceed all ANSI/TIA/EIA-644 specifications.

A recommended termination circuit for the LVDS outputs is shown in Figure 21.

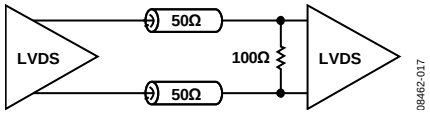


Figure 21. LVDS Output Termination

See the AN-586 Application Note on the Analog Devices website at www.analog.com for more information about LVDS.

LVCMOS CLOCK DISTRIBUTION

The AD9575 provides a 33.33 MHz or 62.5 MHz clock output, which is a dedicated LVCMOS level. Whenever single-ended LVCMOS clocking is used, some of the following general guidelines should be followed.

Point-to-point nets should be designed such that a driver has only one receiver on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver (see Figure 22). The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). LVCMOS outputs are limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 6 inches are recommended to preserve signal rise/fall times and preserve signal integrity.

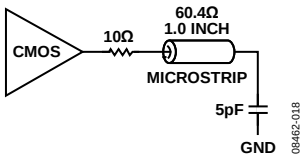


Figure 22. Series Termination of LVCMOS Output

Termination at the far end of the PCB trace is a second option. The LVCMOS output of the AD9575 does not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 23. The far-end termination network should match the PCB trace impedance and provide the desired switching point.

The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

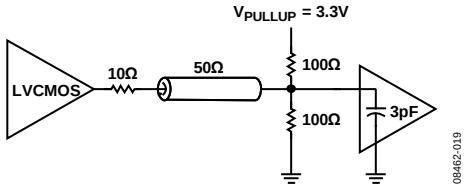


Figure 23. LVCMOS Output with Far-End Termination

TYPICAL APPLICATION CIRCUIT

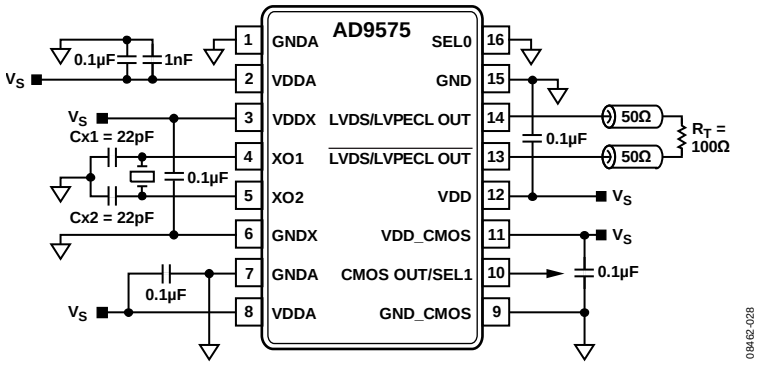
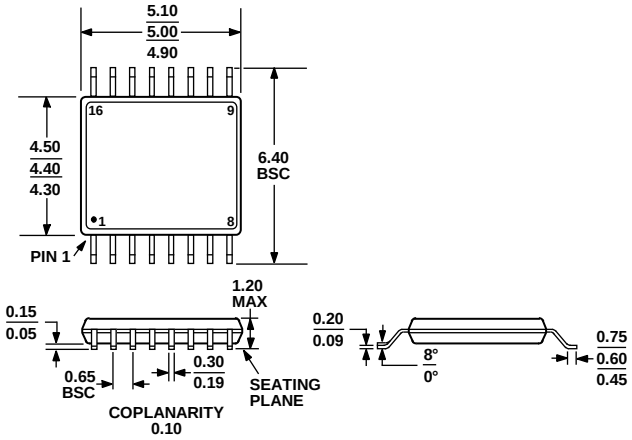


Figure 24. Typical Application Circuit (in LVDS Configuration)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9575ARUZLVD	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP), 96 pcs per Tube, LVDS Output Format	RU-16
AD9575ARUZPEC	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP), 96 pcs per Tube, LVPECL Output Format	RU-16
AD9575-EVALZ-LVD		LVDS Outputs, Evaluation Board	
AD9575-EVALZ-PEC		LVPECL Outputs, Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D08462-0-3/10(A)