

FEATURES

- 44 V supply maximum ratings**
- ±15 V analog signal range**
- Low on resistance (< 35 Ω)**
- Ultralow power dissipation (35 μW)**
- Fast switching times**
 - t_{ON} < 175 ns**
 - t_{OFF} < 145 ns**
- TTL-/CMOS-compatible**
- Plug-in replacement for DG411/DG412/DG413**

APPLICATIONS

- Audio and video switching**
- Automatic test equipment**
- Precision data acquisition**
- Battery-powered systems**
- Sample-and-hold systems**
- Communication systems**

GENERAL DESCRIPTION

The ADG411, ADG412, and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which provides low power dissipation yet gives high switching speed and low on resistance.

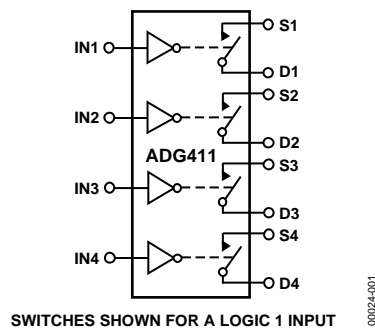
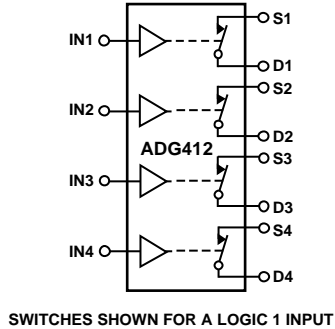
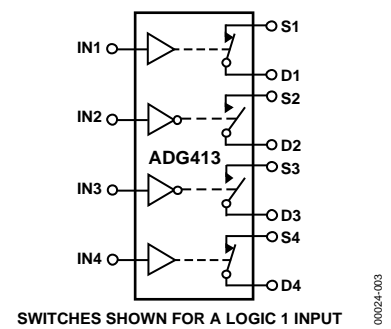
The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG411, ADG412, and ADG413 contain four independent SPST switches. The ADG411 and ADG412 differ only in that the digital control logic is inverted. The ADG411 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG412. The ADG413 has two switches with digital control logic similar to that of the ADG411 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when on, and each has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended signal range
The ADG411, ADG412, and ADG413 are fabricated on an enhanced LC²MOS, giving an increased signal range which extends fully to the supply rails.
2. Ultralow power dissipation
3. Low R_{ON}
4. Break-before-make switching
This prevents channel shorting when the switches are configured as a multiplexer.
5. Single-supply operation
For applications where the analog signal is unipolar, the ADG411, ADG412, and ADG413 can be operated from a single-rail power supply. The parts are fully specified with a single 12 V power supply and remain functional with single supplies as low as 5 V.

FUNCTIONAL BLOCK DIAGRAMS

Figure 1. ADG411
00024-001

Figure 2. ADG412
00024-002

Figure 3. ADG413
00024-003
Rev. D

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	5
Applications.....	1	ESD Caution.....	5
General Description	1	Pin Configuration and Function Descriptions.....	6
Product Highlights	1	Typical Performance Characteristics	7
Functional Block Diagrams.....	1	Terminology	9
Revision History	2	Applications.....	10
Specifications.....	3	Test Circuits.....	11
Dual Supply	3	Outline Dimensions	13
Single Supply	4	Ordering Guide	15

REVISION HISTORY

6/10—Rev. C to Rev. D

Updated Outline Dimensions	13
Changes to Ordering Guide	15

11/04—Rev. B to Rev. C

Format Updated.....	Universal
Change to Package Drawing (Figure 23)	13
Changes to Ordering Guide	14

7/04—Rev. A to Rev. B

Changes to ORDERING GUIDE	5
Updated OUTLINE DIMENSIONS	11

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.¹

Table 1.

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range	V_{DD} to V_{SS}		V_{DD} to V_{SS}		V	
R_{ON}	25		25		Ω typ	$V_D = \pm 8.5\text{ V}$, $I_S = -10\text{ mA}$; $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
	35	45	35	45	Ω max	
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	± 0.1		± 0.1		nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_D = +15.5\text{ V}/-15.5\text{ V}$, $V_S = -15.5\text{ V}/+15.5\text{ V}$; Figure 15 $V_D = +15.5\text{ V}/-15.5\text{ V}$, $V_S = -15.5\text{ V}/+15.5\text{ V}$; Figure 15 $V_D = V_S = +15.5\text{ V}/-15.5\text{ V}$; Figure 16
Drain OFF Leakage I_D (OFF)	± 0.25	± 0.25	± 0.25	± 20	nA max	
	± 0.1		± 0.1		nA typ	
Channel ON Leakage I_D , I_S (ON)	± 0.25	± 5	± 0.25	± 20	nA max	
	± 0.1		± 0.1		nA typ	
	± 0.4	± 10	± 0.4	± 40	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4		2.4		V min	
Input Low Voltage, V_{INL}	0.8		0.8		V max	
Input Current	0.005		0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
I_{INL} or I_{INH}		± 0.5		± 0.5	μA max	
DYNAMIC CHARACTERISTICS²						
t_{ON}	110		110		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Figure 17
		175		175	ns max	
t_{OFF}	100		100		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_S = \pm 10\text{ V}$; Figure 17
		145		145	ns max	
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$; $V_{S1} = V_{S2} = 10\text{ V}$; Figure 18
Charge Injection	5		5		pC typ	
OFF Isolation	68		68		dB typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 10\text{ nF}$; Figure 19
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 20
C_S (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	35		35		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS						
I_{DD}	0.0001		0.0001		μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$; Digital inputs = 0 V or 5 V
	1	5	1	5	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	
I_L	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	

¹ Temperature ranges are as follows: B versions: -40°C to $+85^\circ\text{C}$; T versions: -55°C to $+125^\circ\text{C}$.

² Guaranteed by design; not subject to production test.

ADG411/ADG412/ADG413

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.¹

Table 2.

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
ANALOG SIGNAL RANGE	0 V to V_{DD}		0 V to V_{DD}		V	
R_{ON}	40		40		Ω typ	$0 < V_D = 8.5\text{ V}$, $I_S = -10\text{ mA}$;
	80	100	80	100	Ω max	$V_{DD} = 10.8\text{ V}$
LEAKAGE CURRENTS						$V_{DD} = 13.2\text{ V}$
Source OFF Leakage I_S (OFF)	± 0.1		± 0.1		nA typ	$V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$;
	± 0.25	± 5	± 0.25	± 20	nA max	Figure 15
Drain OFF Leakage I_D (OFF)	± 0.1		± 0.1		nA typ	$V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$;
	± 0.25	± 5	± 0.25	± 20	nA max	Figure 15
Channel ON Leakage I_D, I_S (ON)	± 0.1		± 0.1		nA typ	$V_D = V_S = 12.2\text{ V}/1\text{ V}$;
	± 0.4	± 10	± 0.4	± 40	nA max	Figure 16
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4		2.4		V min	
Input Low Voltage, V_{INL}	0.8		0.8		V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.5		± 0.5	μA max	
DYNAMIC CHARACTERISTICS ²						
t_{ON}	175		175		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		250		250	ns max	$V_S = 8\text{ V}$; Figure 17
t_{OFF}	95		95		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
		125		125	ns max	$V_S = 8\text{ V}$; Figure 17
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$;
Charge Injection	25		25		pC typ	$V_{S1} = V_{S2} = +10\text{ V}$; Figure 18
OFF Isolation	68		68		dB typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 10\text{ nF}$;
						Figure 19
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
						Figure 20
C_S (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
C_D, C_S (ON)	35		35		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS						$V_{DD} = 13.2\text{ V}$;
I_{DD}	0.0001		0.0001		μA typ	Digital inputs = 0 V or 5 V
	1	5	1	5	μA max	
I_L	0.0001		0.0001		μA typ	
	1	5	1	5	μA max	$V_L = 5.25\text{ V}$

¹ Temperature ranges are as follows: B versions: -40°C to +85°C; T versions: -55°C to +125°C.

² Guaranteed by design; not subject to production test.

Table 3. Truth Table (ADG411/ADG412)

ADG411 In	ADG412 In	Switch Condition
0	1	ON
1	0	OFF

Table 4. Truth Table (ADG413)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameters	Ratings
V_{DD} to V_{SS}	44 V
V_{DD} to GND	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
V_L to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog, Digital Inputs ¹	$V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	100 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
PDIP, Power Dissipation	470 mW
θ_{JA} Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 s)	260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA} Thermal Impedance	77°C/W
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	115°C/W
θ_{JC} Thermal Impedance	35°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG411/ADG412/ADG413

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

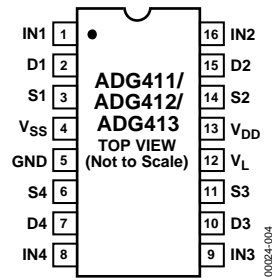


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1–IN4	Logic Control Input.
2, 7, 10, 15	D1–D4	Drain Terminal. Can be an input or output.
3, 6, 11, 14	S1–S4	Source Terminal. Can be an input or output.
4	V _{SS}	Most Negative Power Supply Potential in Dual Supplies. In single supply applications, it may be connected to GND.
5	GND	Ground (0 V) Reference.
12	V _L	Logic Power Supply (5 V).
13	V _{DD}	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS

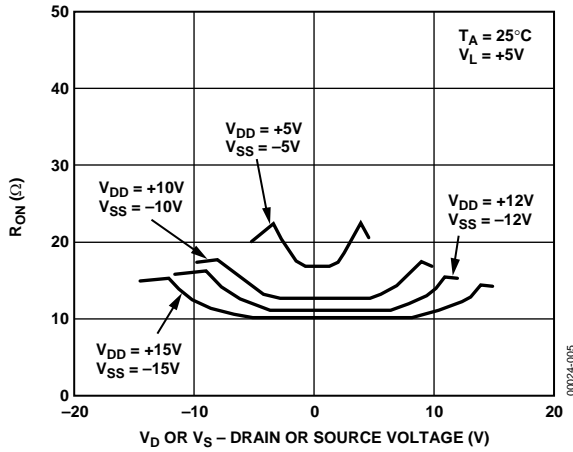


Figure 5. On Resistance as a Function of V_D (V_S) Dual Supplies

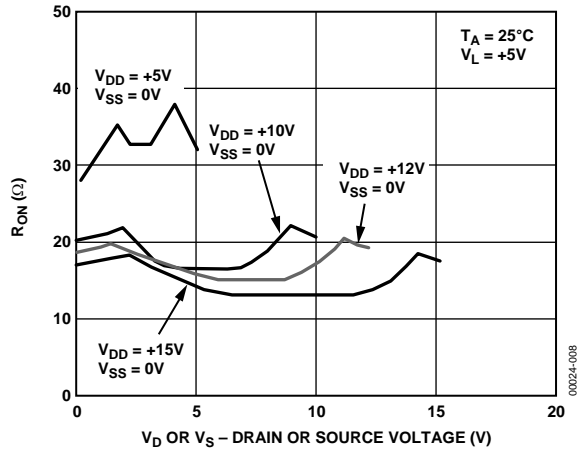


Figure 8. On Resistance as a Function of V_D (V_S) Single Supply

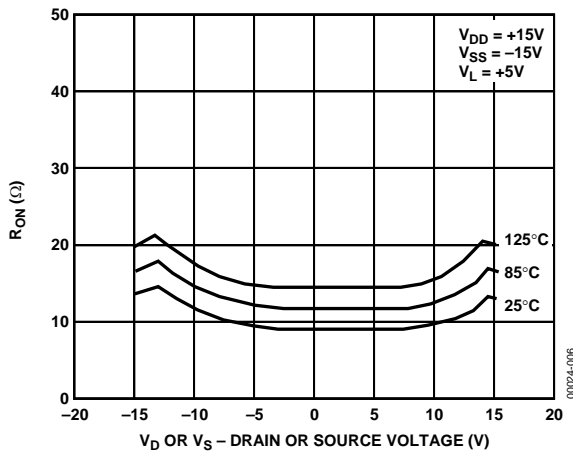


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures

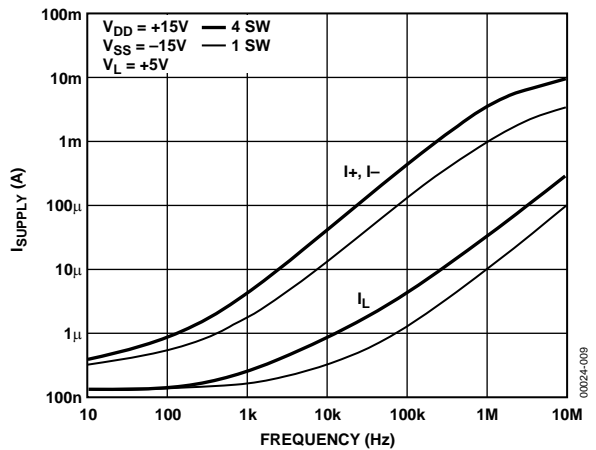


Figure 9. Supply Current vs. Input Switching Frequency

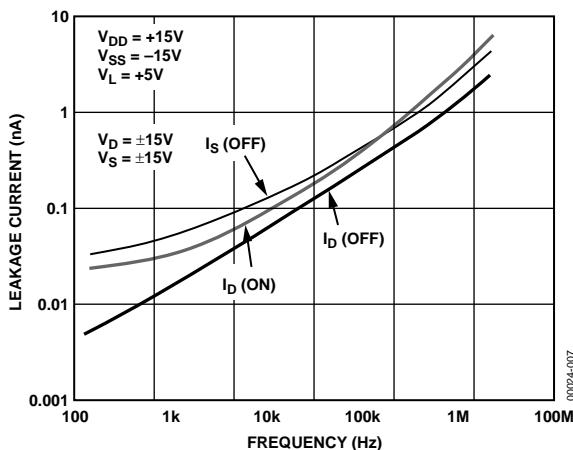


Figure 7. Leakage Currents as a Function of Temperature

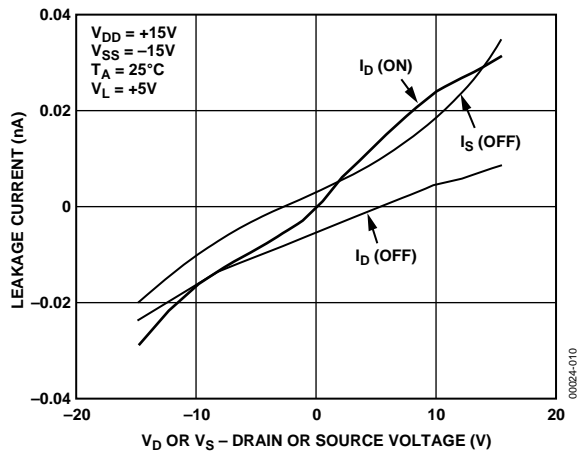


Figure 10. Leakage Currents as a Function of V_D (V_S)

ADG411/ADG412/ADG413



Figure 11. Off Isolation vs. Frequency



Figure 12. Crosstalk vs. Frequency

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

I_S (OFF)

Source leakage current with the switch OFF.

I_D (OFF)

Drain leakage current with the switch OFF.

I_D, I_S (ON)

Channel leakage current with the switch ON.

V_D (V_S)

Analog voltage on terminals D, S.

C_S (OFF)

OFF switch source capacitance.

C_D (OFF)

OFF switch drain capacitance.

C_D, C_S (ON)

ON switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_D

OFF time or ON time measured between the 90% points of both switches, when switching from one address state to another.

Crosstalk

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an OFF switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

ADG411/ADG412/ADG413

APPLICATIONS

Figure 13 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN} . In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H .

Due to switch and capacitor leakage, the voltage on the hold capacitor decreases with time. The ADG411/ADG412/ADG413 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically $30 \mu\text{V}/\mu\text{s}$.

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches are at the same potential, they have a differential effect on the op amp AD711, which minimizes charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C . This compensation network also reduces

the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the $\pm 10 \text{ V}$ input range. Both the acquisition and settling times are 850 ns.

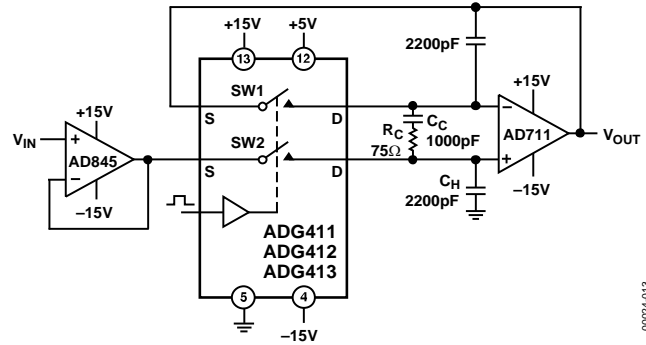


Figure 13. Fast, Accurate Sample-and-Hold

00024-013

TEST CIRCUITS



Figure 14. On Resistance



Figure 15. Off Leakage



Figure 16. On Leakage

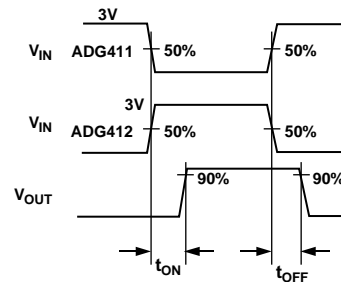
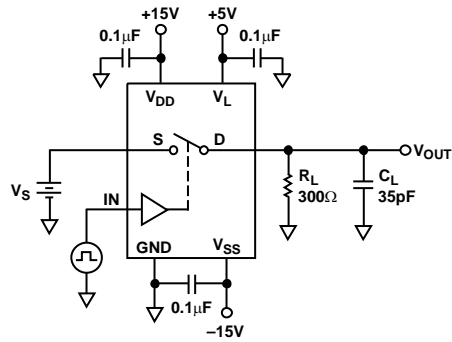


Figure 17. Switching Times

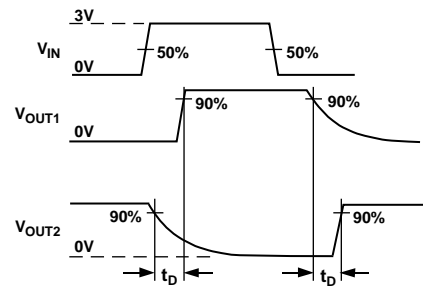


Figure 18. Break-Before-Make Time Delay

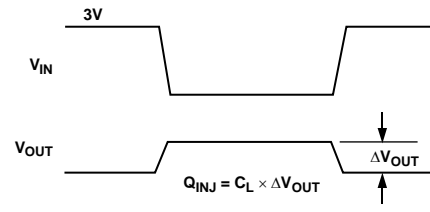
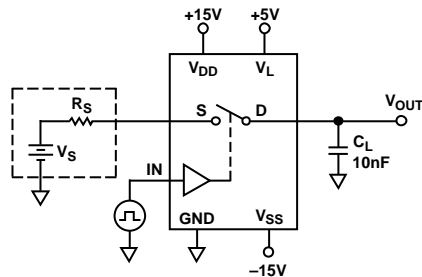


Figure 19. Charge Injection

ADG411/ADG412/ADG413



Figure 20. Off Isolation

00024-020

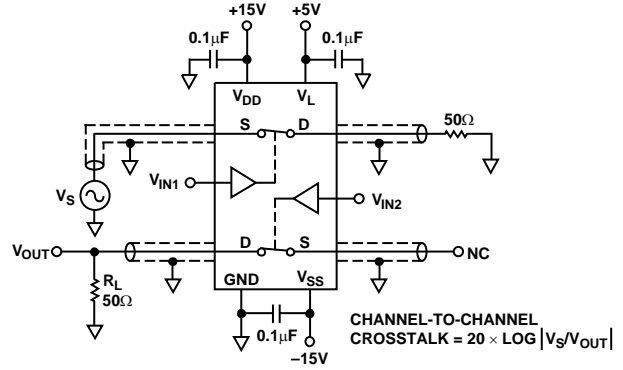


Figure 21. Channel-to-Channel Crosstalk

$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \text{LOG} |V_S/V_{\text{OUT}}|$$

00024-021

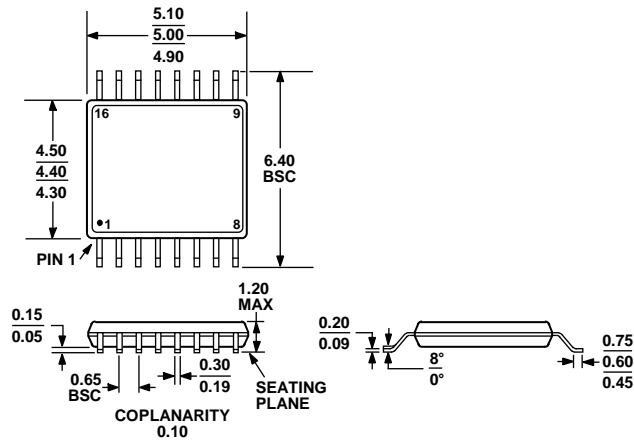
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 16-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-16)
 Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-16)
 Dimensions shown in millimeters

ADG411/ADG412/ADG413



COMPLIANT TO JEDEC STANDARDS MS-001-AB
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 24. 16-Lead Plastic Dual In-Line Package [PDIP]
 (N-16)

Dimensions shown in inches and (millimeters)

072106-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG411BN	-40°C to +85°C	16-Lead P-DIP	N-16
ADG411BNZ	-40°C to +85°C	16-Lead P-DIP	N-16
ADG411BR	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG411BR-REEL	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG411BR-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG411BRZ	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG411BRZ-REEL	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG411BRZ-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG411BRU	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG411BRU-REEL	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG411BRU-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG411BRUZ	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG411BRUZ-REEL	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG411BRUZ-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG411BCHIPS		DIE	
ADG412BN	-40°C to +85°C	16-Lead P-DIP	N-16
ADG412BNZ	-40°C to +85°C	16-Lead P-DIP	N-16
ADG412BR	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG412BR-REEL	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG412BR-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG412BRZ	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG412BRZ-REEL	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG412BRZ-REEL7	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG412BRU	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG412BRU-REEL	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG412BRU-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG412BRUZ	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG412BRUZ-REEL	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG412BRUZ-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG413BN	-40°C to +85°C	16-Lead P-DIP	N-16
ADG413BNZ	-40°C to +85°C	16-Lead P-DIP	N-16
ADG413BR	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG413BR-REEL	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG413BRZ	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG413BRZ-REEL	-40°C to +85°C	16-Lead SOIC_N	R-16
ADG413BRUZ	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG413BRUZ-500RL7	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG413BRUZ-REEL	-40°C to +85°C	16-Lead TSSOP	RU-16
ADG413BRUZ-REEL7	-40°C to +85°C	16-Lead TSSOP	RU-16

¹Z = RoHS Compliant Part.

NOTES