



CMOS 3 V/5 V, Wide Bandwidth Quad 2:1 Mux in Chip Scale Package

ADG784

FEATURES

Low Insertion Loss and On Resistance: 4 Ω Typical

On-Resistance Flatness <2 Ω

Bandwidth >200 MHz

Single 3 V/5 V Supply Operation

Rail-to-Rail Operation

Very Low Distortion: <1%

Low Quiescent Supply Current (100 nA Typical)

Fast Switching Times

t_{ON} 10 ns

t_{OFF} 4 ns

TTL/CMOS Compatible

For Functionally Equivalent Devices in 16-Lead QSOP/
SOIC Packages, See ADG774

APPLICATIONS

100VG-AnyLAN

Token Ring 4 Mbps/16 Mbps

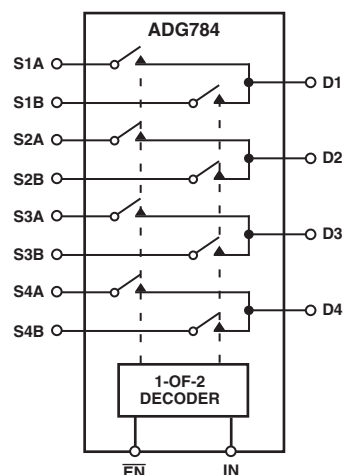
ATM25/155

NIC Adapter and Hubs

Audio and Video Switching

Relay Replacement

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG784 is a monolithic CMOS device comprising four 2:1 multiplexer/demultiplexers with high impedance outputs. The CMOS process provides low power dissipation yet gives high switching speed and low on resistance. The on-resistance variation is typically less than 0.5 Ω with an input signal ranging from 0 V to 5 V.

The bandwidth of the ADG784 is greater than 200 MHz and this, coupled with low distortion (typically 0.5%), makes the part suitable for switching fast ethernet signals.

The on-resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed, coupled with high signal bandwidth, also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG784 operates from a single 3.3 V/5 V supply and is TTL logic compatible. The control logic for each switch is shown in the Truth Table.

These switches conduct equally well in both directions when ON, and have an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG784 switches exhibit break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Also Available as ADG774 in 16-Lead QSOP and SOIC.
2. Wide Bandwidth Data Rates >200 MHz.
3. Ultralow Power Dissipation.

4. Extended Signal Range.

The ADG784 is fabricated on a CMOS process giving an increased signal range that fully extends to the supply rails.

5. Low Leakage over Temperature.
6. Break-Before-Make Switching.
This prevents channel shorting when the switches are configured as a multiplexer.
7. Crosstalk is typically -70 dB @ 30 MHz.
8. Off isolation is typically -60 dB @ 10 MHz.
9. Available in Chip Scale Package (CSP).

REV. A

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ADG784* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1024: How to Calculate the Settling Time and Sampling Rate of a Multiplexer

Data Sheet

- ADG784: CMOS 3 V/5 V, Wide Bandwidth Quad 2:1 Mux in Chip Scale Package Data Sheet

REFERENCE MATERIALS

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

DESIGN RESOURCES

- ADG784 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG784 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

ADG784—SPECIFICATIONS

SINGLE SUPPLY ($V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	T _{MIN} to T _{MAX}		
ANALOG SWITCH				
Analog Signal Range	2.2	0 V to V _{DD}	V	V _D = 0 V to V _{DD} , I _S = −10 mA
On Resistance (R _{ON})		5	Ω typ Ω max	
On Resistance Match Between Channels (ΔR _{ON})	0.15	0.5	Ω typ Ω max	V _D = 0 V to V _{DD} , I _S = −10 mA
On Resistance Flatness (R _{FLAT(ON)})	0.5	1	Ω typ Ω max	V _D = 0 V to V _{DD} ; I _S = −10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01 ±0.5	±1	nA typ nA max	V _D = 4.5 V, V _S = 1 V; V _D = 1 V, V _S = 4.5 V; Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.01 ±0.5	±1	nA typ nA max	V _D = 4.5 V, V _S = 1 V; V _D = 1 V, V _S = 4.5 V; Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01 ±0.5	±1	nA typ nA max	V _D = V _S = 4.5 V; V _D = V _S = 1 V; Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}		0.8	V max	
Input Current I _{INL} or I _{INH}	0.001	±0.5	μA typ μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}		10 20	ns typ ns max	R _L = 100 Ω, C _L = 35 pF, V _S = 3 V; Test Circuit 4
t _{OFF}		4 8	ns typ ns max	R _L = 100 Ω, C _L = 35 pF, V _S = 3 V; Test Circuit 4
Break-Before-Make Time Delay, t _D		5 1	ns typ ns min	R _L = 100 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 5 V; Test Circuit 5
Off Isolation		−65	dB typ	R _L = 100 Ω, f = 10 MHz; Test Circuit 7
Channel-to-Channel Crosstalk		−75	dB typ	R _L = 100 Ω, f = 10 MHz; Test Circuit 8
Bandwidth −3 dB		240	MHz typ	R _L = 100 Ω; Test Circuit 6
Distortion		0.5	% typ	R _L = 100 Ω
Charge Injection		10	pC typ	C _L = 1 nF; Test Circuit 9
C _S (OFF)		10	pF typ	f = 1 kHz
C _D (OFF)		20	pF typ	f = 1 kHz
C _D , C _S (ON)		30	pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	0.001	1	μA max μA typ	V _{DD} = 5.5 V Digital Inputs = 0 V or V _{DD}
I _{IN}		1	μA typ	V _{IN} = 5 V
I _O		100	mA max	V _S /V _D = 0 V

NOTES

¹Temperature ranges are as follows: B Version, -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY ($V_{DD} = 3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	25°C	T _{MIN} to T _{MAX}		
ANALOG SWITCH				
Analog Signal Range	4	0 V to V _{DD}	V	V _D = 0 V to V _{DD} , I _S = -10 mA
On Resistance (R _{ON})		10	Ω typ Ω max	
On Resistance Match Between Channels (ΔR _{ON})	0.15	0.5	Ω typ Ω max	V _D = 0 V to V _{DD} , I _S = -10 mA
On Resistance Flatness (R _{FLAT(ON)})	2	4	Ω typ Ω max	V _D = 0 V to V _{DD} , I _S = -10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01 ±0.5	±1	nA typ nA max	V _D = 3 V, V _S = 1 V; V _D = 1 V, V _S = 3 V; Test Circuit 2
Drain OFF Leakage I _D (OFF)	±0.01 ±0.5	±1	nA typ nA max	V _D = 3 V, V _S = 1 V; V _D = 1 V, V _S = 3 V; Test Circuit 2
Channel ON Leakage I _D , I _S (ON)	±0.01 ±0.5	±1	nA typ nA max	V _D = V _S = 3 V; V _D = V _S = 1 V; Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}		0.4	V max	
Input Current I _{INL} or I _{INH}	0.001	±0.5	μA typ μA max	
DYNAMIC CHARACTERISTICS ²				
t _{ON}		12 25	ns typ ns max	R _L = 100 Ω, C _L = 35 pF, V _S = 1.5 V; Test Circuit 4
t _{OFF}		5 10	ns typ ns max	R _L = 100 Ω, C _L = 35 pF, V _S = 1.5 V; Test Circuit 4
Break-Before-Make Time Delay, t _D		5 1	ns typ ns min	R _L = 100 Ω, C _L = 35 pF, V _{S1} = V _{S2} = 3 V; Test Circuit 5
Off Isolation		-65	dB typ	R _L = 50 Ω, f = 10 MHz; Test Circuit 7
Channel-to-Channel Crosstalk		-75	dB typ	R _L = 50 Ω, f = 10 MHz; Test Circuit 8
Bandwidth -3 dB		240	MHz typ	R _L = 50 Ω; Test Circuit 6
Distortion		2	% typ	R _L = 50 Ω
Charge Injection		3	pC typ	C _L = 1 nF; Test Circuit 9
C _S (OFF)		10	pF typ	f = 1 kHz
C _D (OFF)		20	pF typ	f = 1 kHz
C _D , C _S (ON)		30	pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	0.001	1	μA max μA typ	V _{DD} = 3.3 V Digital Inputs = 0 V or V _{DD}
I _{IN}		1	μA typ	V _{IN} = 3 V
I _O		100	mA max	V _S /V _D = 0 V

NOTES

¹Temperature ranges are as follows: B Version, -40°C to +85°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Table I. Truth Table

\overline{EN}	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	DISABLE
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

ADG784

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted.)

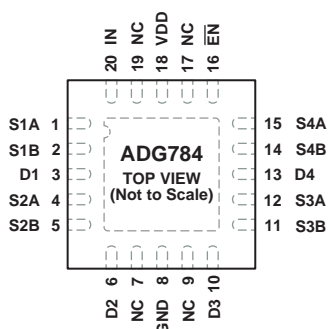
V _{DD} to GND	–0.3 V to +6 V
Analog, Digital Inputs ²	–0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Chip Scale Package	
θ _{JA} Thermal Impedance	32°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	2 kV

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATION



NOTES

1. NC = NO CONNECT.
2. EXPOSED PAD TIED TO SUBSTRATE, GND.

TERMINOLOGY

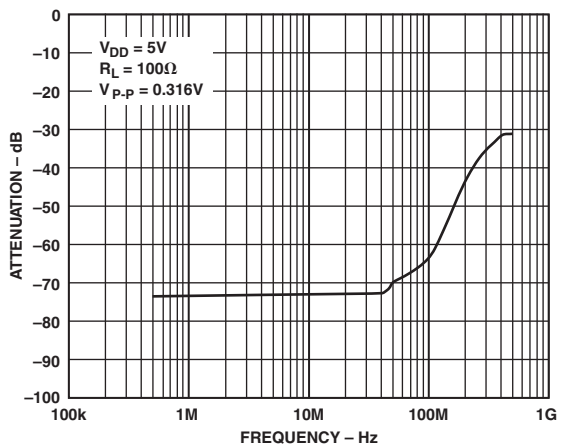
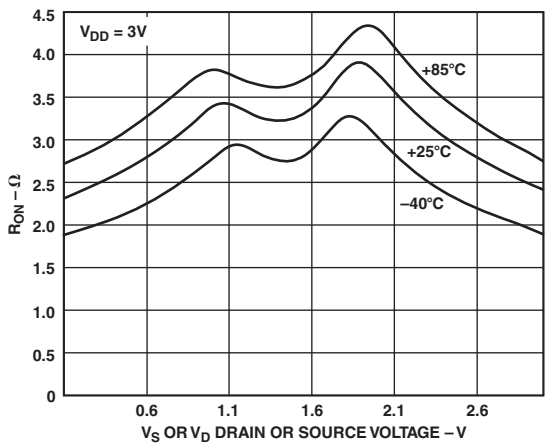
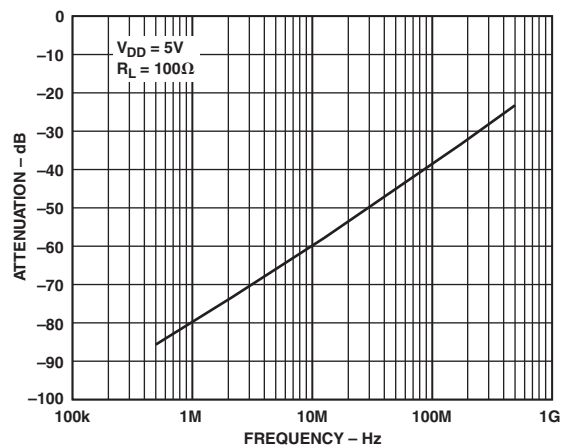
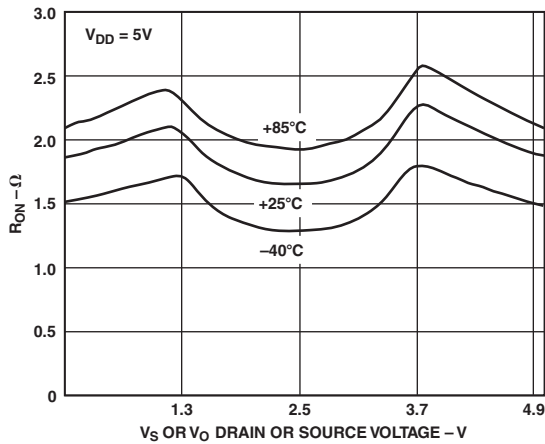
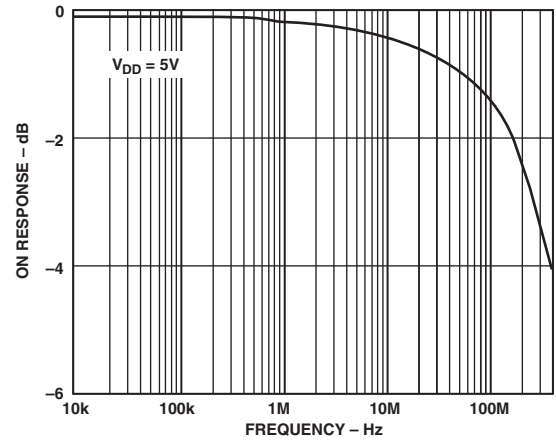
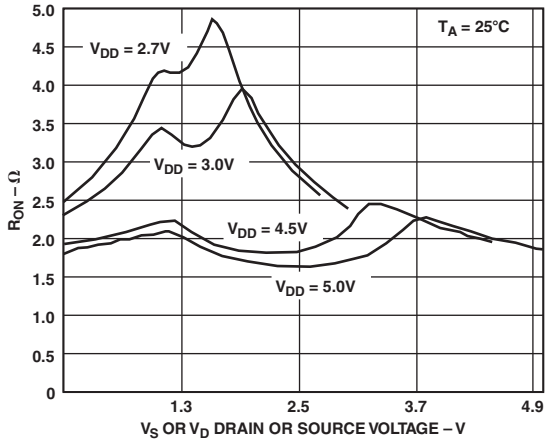
V _{DD}	Most Positive Power Supply Potential.
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
$\overline{\text{EN}}$	Logic Control Input.
R _{ON}	Ohmic resistance between D and S.
ΔR _{ON}	On Resistance match between any two channels i.e., R _{ON} max – R _{ON} min.
R _{FLAT(ON)}	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I _S (OFF)	Source Leakage Current with the switch “OFF.”
I _D (OFF)	Drain Leakage Current with the switch “OFF.”
I _D , I _S (ON)	Channel Leakage Current with the switch “ON.”
V _D (V _S)	Analog Voltage on Terminals D, S.
C _S (OFF)	“OFF” Switch Source Capacitance.
C _D (OFF)	“OFF” Switch Drain Capacitance.
C _D , C _S (ON)	“ON” Switch Capacitance.
t _{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t _{OFF}	Delay between applying the digital control input and the output switching Off.
t _D	“OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
Bandwidth	Frequency response of the switch in the ON state measured at 3 dB down.
Distortion	R _{FLAT(ON)} /R _L

CAUTION

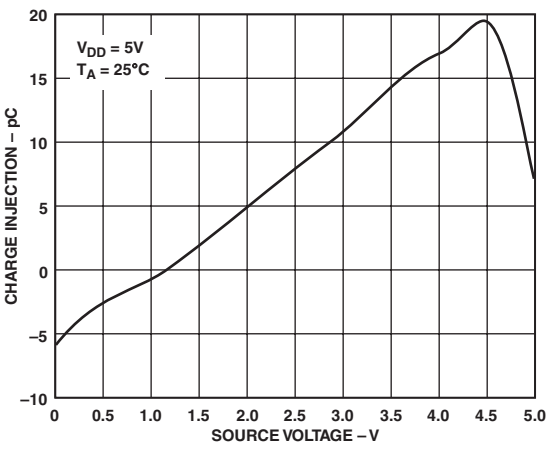
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG784 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance Characteristics—ADG784



ADG784



TPC 7. Charge Injection vs. Source Voltage

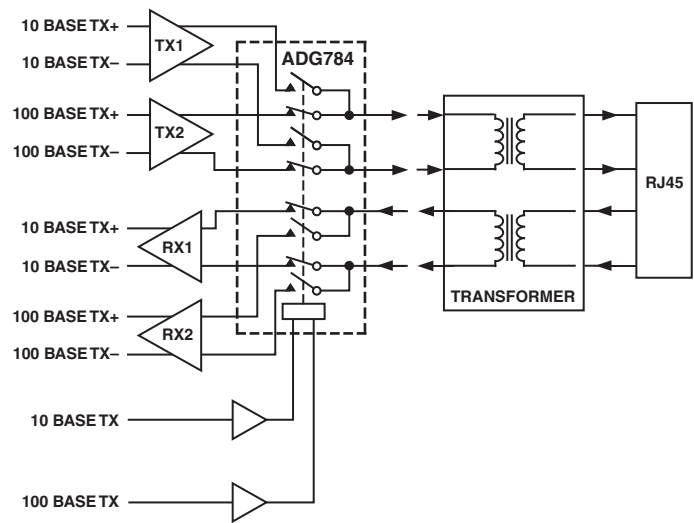


Figure 1. Full Duplex Transceiver

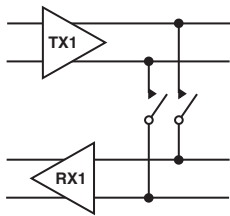


Figure 2. Loop Back

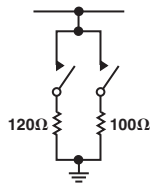


Figure 3. Line Termination

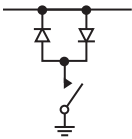
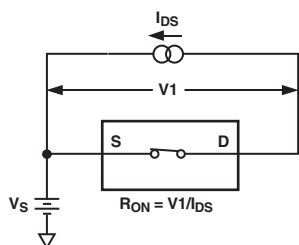
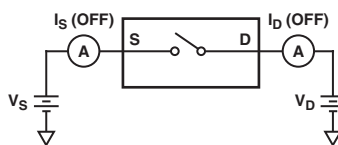


Figure 4. Line Clamp

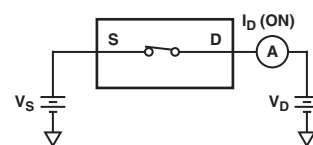
Test Circuits



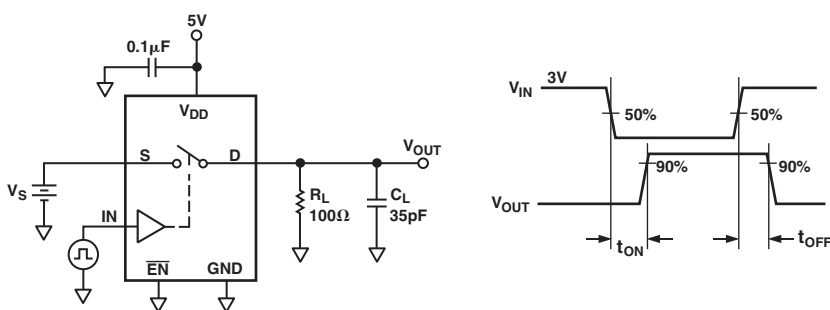
Test Circuit 1. On Resistance



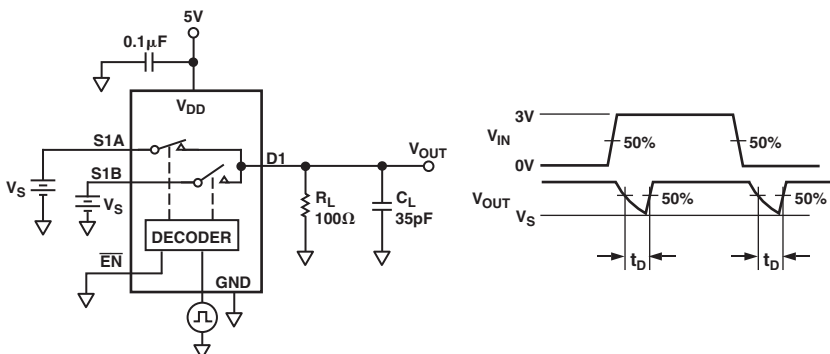
Test Circuit 2. Off Leakage



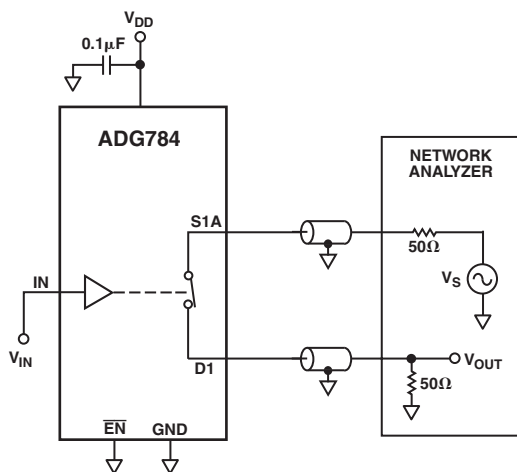
Test Circuit 3. On Leakage



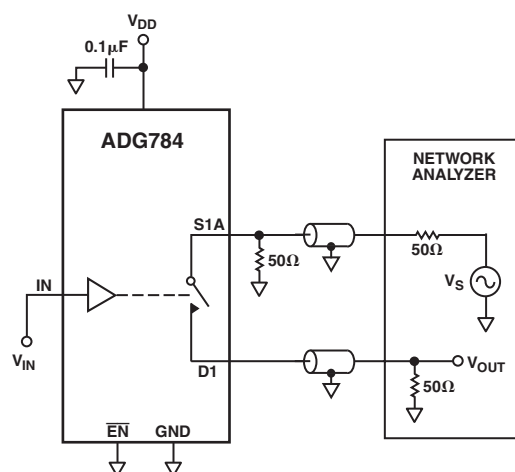
Test Circuit 4. Switching Times



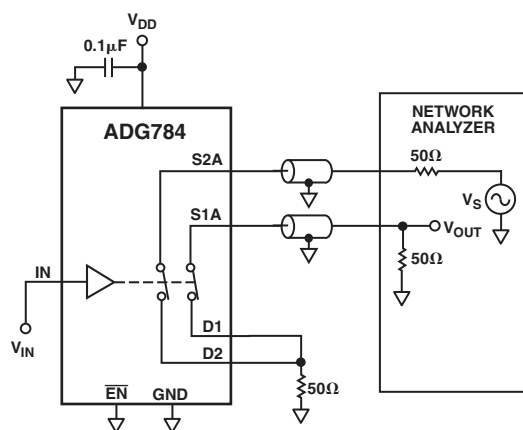
Test Circuit 5. Break-Before-Make Time Delay



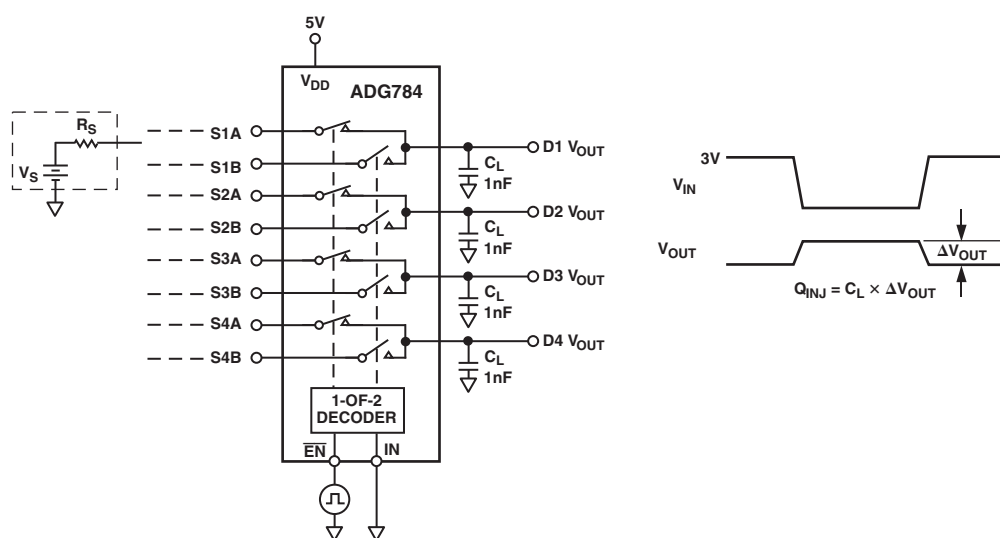
Test Circuit 6. Bandwidth



Test Circuit 7. Off Isolation

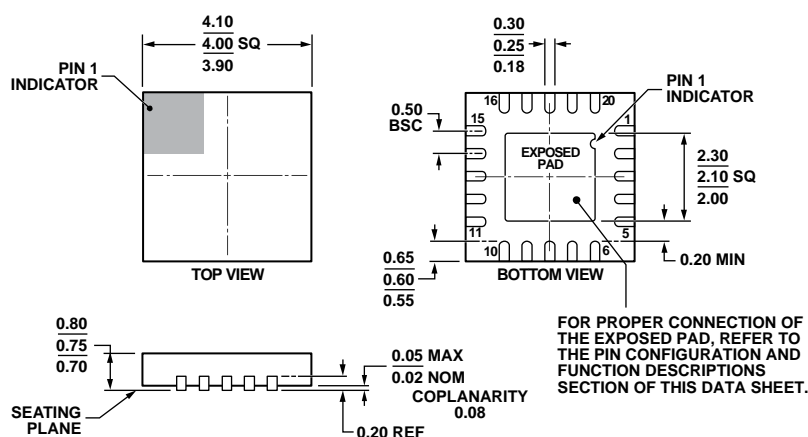
ADG784

Test Circuit 8. Channel-to-Channel Crosstalk



Test Circuit 9. Charge Injection

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 37. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

08-16-2010-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG784BCPZ	−40°C to +85°C	20-Lead LFCSP_WQ	CP-20-6
ADG784BCPZ-REEL	−40°C to +85°C	20-Lead LFCSP_WQ	CP-20-6
ADG784BCPZ-REEL7	−40°C to +85°C	20-Lead LFCSP_WQ	CP-20-6

¹ Z = RoHS Compliant Part.

REVISION HISTORY

2/13—Rev. 0 to Rev. A

Changes to Pin Configuration.....	4
Updated Outline Dimensions.....	9
Changes to Ordering Guide.....	9

4/01—Revision 0: Initial Version