1.3 Ω CMOS, 1.8 V to 5.5 V Single SPDT Switch/2:1 MUX in SOT-66 Package

ADG859

FEATURES

1.8 V to 5.5 V single supply
Tiny 1.65 mm × 1.65 mm package
Low on resistance: 1.3 Ω at 5 V supply
High current-carrying capability:
300 mA continuous current
500 mA peak current at 5 V
Rail-to-rail operation
Typical power consumption: <0.01 µW
TTL-/CMOS-compatible inputs

APPLICATIONS

Cellular phones
PDAs
MP3 players
Battery-powered systems
Audio and video signal routing
Modems
PCMCIA cards
Hard drives
Relay replacement

FUNCTIONAL BLOCK DIAGRAM

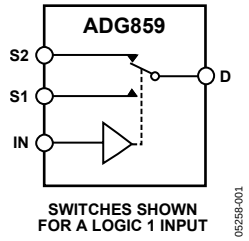

Figure 1.

GENERAL DESCRIPTION

The ADG859 is a monolithic, CMOS SPDT (single pole, double throw) switch that operates with a supply range of 1.8 V to 5.5 V. It is designed to offer low on resistance of 2.3 Ω maximum over the entire temperature range of −40°C to +125°C. The ADG859 also has the capability of carrying large amounts of current, typically 300 mA at 5 V operation. These features make the ADG859 an ideal solution for applications that are space-constrained, such as handsets, PDAs, and MP3 players.

Each switch conducts equally well in both directions when on. The device exhibits break-before-make switching action, thereby preventing momentary shorting when switching channels.

The ADG859 is available in a tiny 6-lead SOT-66 package.

PRODUCT HIGHLIGHTS

1. Low on resistance: 2.3 Ω maximum over the full temperature range of −40°C to +125°C.
2. High current-carrying capability.
3. Tiny 6-lead, 1.65 mm × 1.65 mm SOT-66 package.

Rev. A

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REVISION HISTORY

12/06—Rev. 0 to Rev. A

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6/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	1.3			Ω typ	V_{DD} = 4.5 V, V_S = 0 V to V_{DD}, I_S = −100 mA;
	2.1	2.2	2.3	Ω max	Figure 16
On Resistance Match Between Channels, ΔR_{ON}	0.01			Ω typ	V_{DD} = 4.5 V, V_S = 4.5V, I_S = −100 mA;
	0.093	0.163	0.163	Ω max	Figure 16
On Resistance Flatness, $R_{FLAT (ON)}$	0.32			Ω typ	V_{DD} = 4.5 V, V_S = 0 V to V_{DD}, I_S = −100 mA;
	0.45	0.6	0.65	Ω max	Figure 16
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V; Figure 17
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 4.5 V; Figure 18
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	8			ns typ	R_L = 50 Ω, C_L = 35 pF
	10	11	12	ns max	V_S = 3 V; Figure 19
t_{OFF}	4.5			ns typ	R_L = 50 Ω, C_L = 35 pF
	6	6.5	7	ns max	V_S = 3 V; Figure 19
Break-Before-Make Time Delay, t_{BBM}	4			ns typ	R_L = 50 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 20
Charge Injection	±13			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 21
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 22
Channel-to-Channel Crosstalk	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 23
−3 dB Bandwidth	125			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 24
Insertion Loss	−0.11			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 24
Total Harmonic Distortion (THD + N)	0.062			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 3 V p-p; Figure 14
C_S (Off)	18			pF typ	f = 1 MHz
C_D, C_S (On)	45			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or 5.5 V
			1	μA max	

[1] Temperature range is −40°C to +125°C.

[2] Guaranteed by design; not subject to production test.

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.[1]

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	3			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_S = −100 mA;
	4.3	4.5	4.7	Ω max	Figure 16
On Resistance Match Between Channels, ΔR_{ON}	0.03			Ω typ	V_{DD} = 2.7 V, V_S = 1.2 V, I_S = −100 mA;
	0.11	0.15	0.15	Ω max	Figure 16
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V; Figure 17
Channel On Leakage, I_D, I_S (On)	±0.05			nA typ	V_S = V_D = 1 V or 3 V; Figure 18
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	V_{DD} = 3 V to 3.6 V
			0.7	V max	V_{DD} = 2.7 V
Input Current, I_{INL} or I_{IN}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	11			ns typ	R_L = 50 Ω, C_L = 35 pF
	15	16	17	ns max	V_S = 1.5 V; Figure 19
t_{OFF}	6			ns typ	R_L = 50 Ω, C_L = 35 pF
	9.5	10	11	ns max	V_S = 1.5 V; Figure 19
Break-Before-Make Time Delay, t_{BBM}	5			ns typ	R_L = 50 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 20
Charge Injection	±7			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 21
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 22
Channel-to-Channel Crosstalk	−78			dB typ	S1 to S2; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 23
−3 dB Bandwidth	125			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 24
Insertion Loss	−0.11			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 24
Total Harmonic Distortion (THD + N)	0.1			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p; Figure 14
C_S (Off)	18			pF typ	f = 1 MHz
C_D, C_S (On)	46			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or 3.6 V
			1	μA max	

[1] Temperature range is −40°C to +125°C.
[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
Analog Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	
5 V Operation	500 mA
3 V Operation	460 mA
Continuous Current, S or D	
5 V Operation	300 mA
3 V Operation	275 mA
Operating Temperature Range	
Automotive	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-66 Package (4-Layer Board)	
θ_{JA} Thermal Impedance	191°C/W
Lead-Free Reflow	
Peak Temperature	260 (+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at S or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 4. Truth Table

Logic (IN)	Switch 2 (S2)	Switch 1 (S1)
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

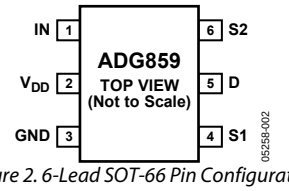

Figure 2. 6-Lead SOT-66 Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN	Logic Control Input.
2	V_{DD}	Most Positive Power Supply Potential.
3	GND	Ground (0 V) Reference.
4	S1	Source Terminal. Can be an input or an output.
5	D	Drain Terminal. Can be an input or an output.
6	S2	Source Terminal. Can be an input or an output.

TYPICAL PERFORMANCE CHARACTERISTICS

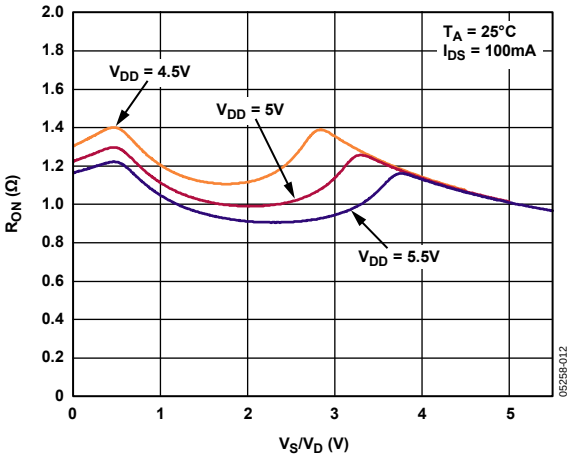

Figure 3. On Resistance vs. V_S (V_D), V_{DD} = 5 V ± 10%

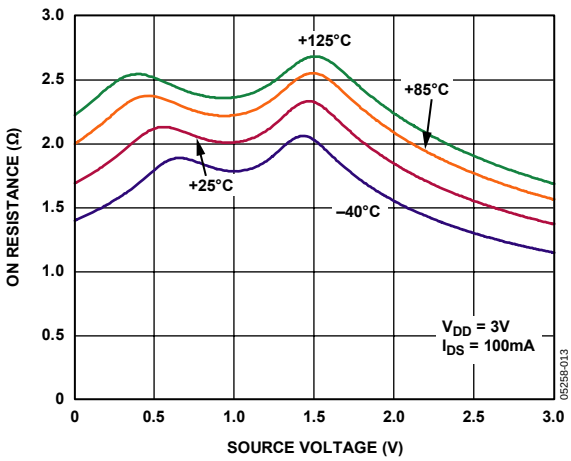

Figure 6. On Resistance vs. Source Voltage for Different Temperatures, V_{DD} = 3 V

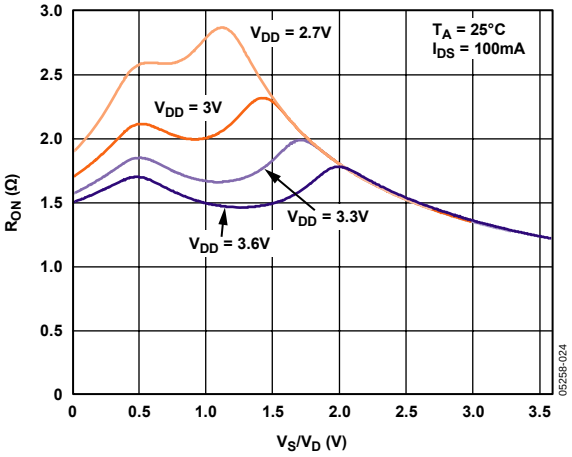

Figure 4. On Resistance vs. V_S (V_D), V_{DD} = 2.7 V to 3.6 V

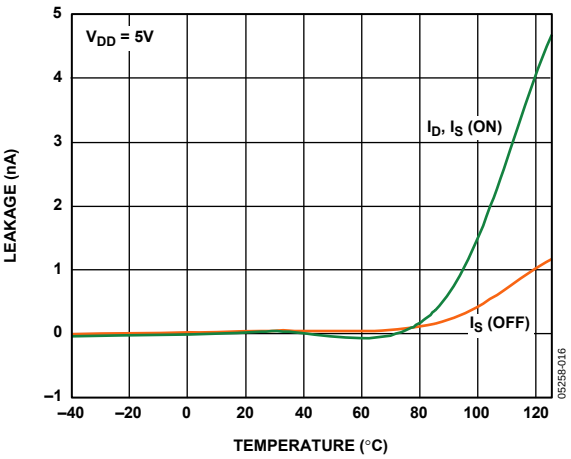

Figure 7. Leakage vs. Temperature, V_{DD} = 5 V

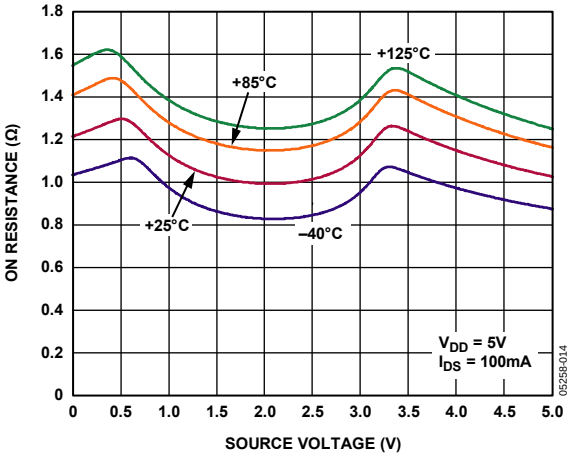

Figure 5. On Resistance vs. Source Voltage for Different Temperatures, V_{DD} = 5 V

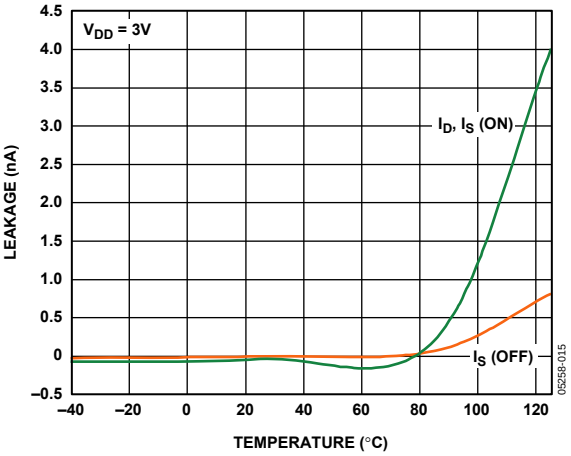

Figure 8. Leakage vs. Temperature, V_{DD} = 3 V

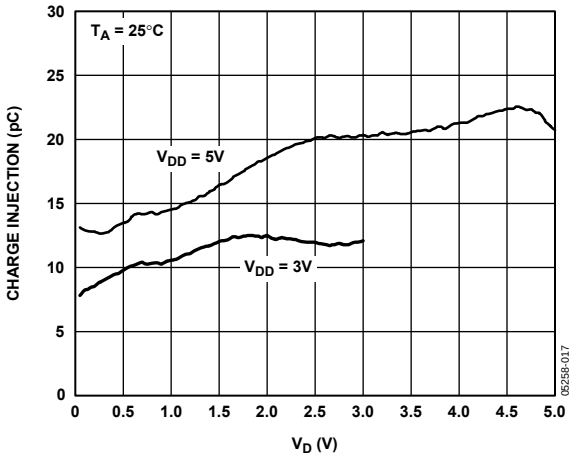

Figure 9. Charge Injection vs. Source Voltage

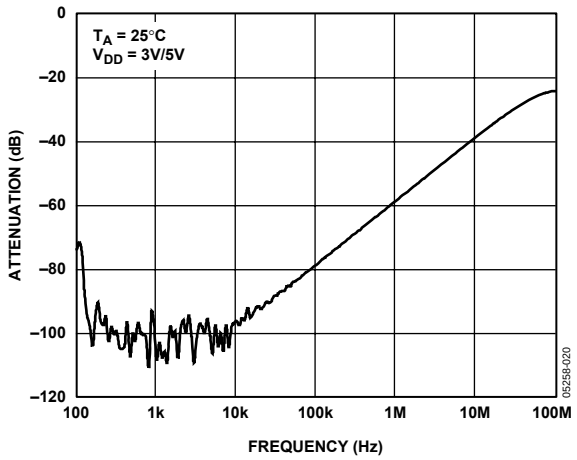

Figure 12. Off Isolation vs. Frequency

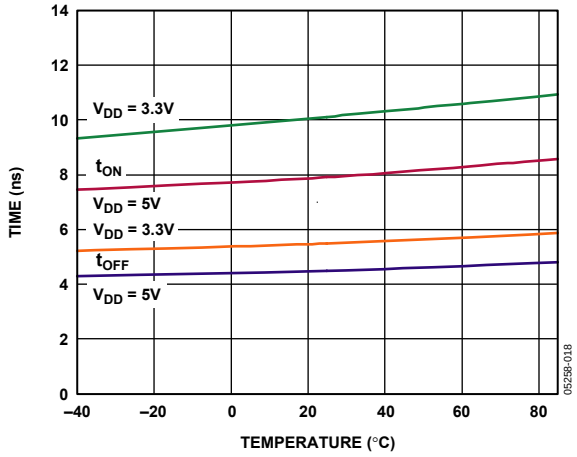

Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

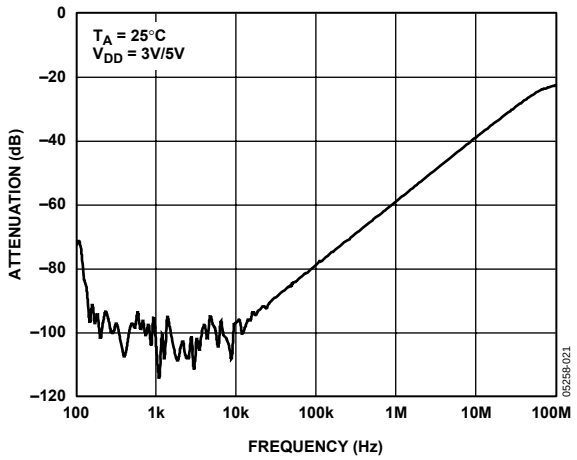

Figure 13. Crosstalk vs. Frequency

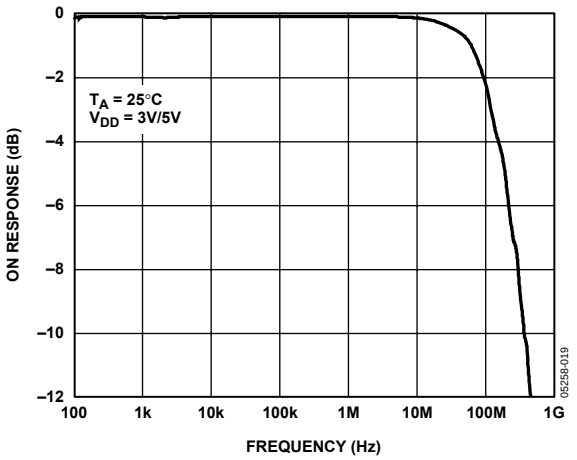

Figure 11. Bandwidth

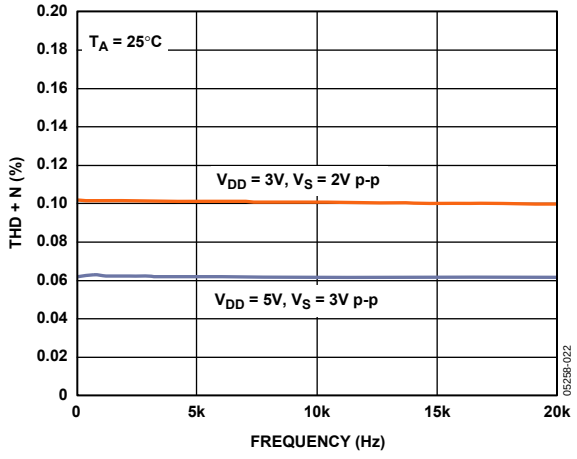

Figure 14. Total Harmonic Distortion + Noise

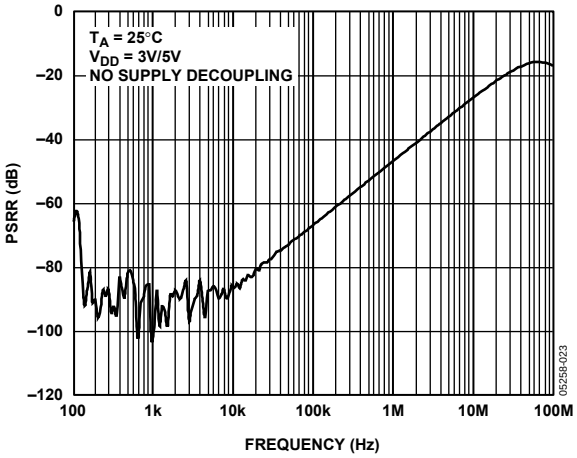

Figure 15. PSRR

TEST CIRCUITS

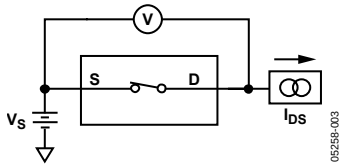

Figure 16. On Resistance

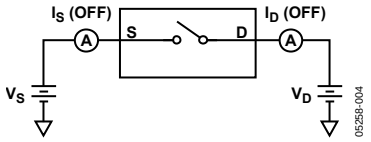

Figure 17. Off Leakage

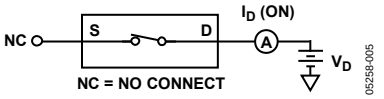

Figure 18. On Leakage

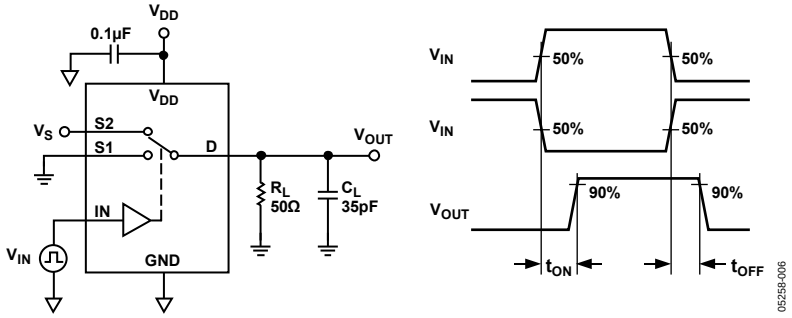

Figure 19. Switching Times, t_{ON}, t_{OFF}

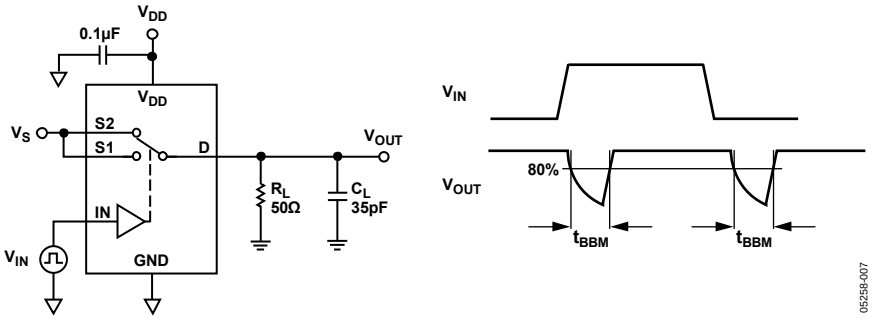

Figure 20. Break-Before-Make Time Delay, t_{BBM}

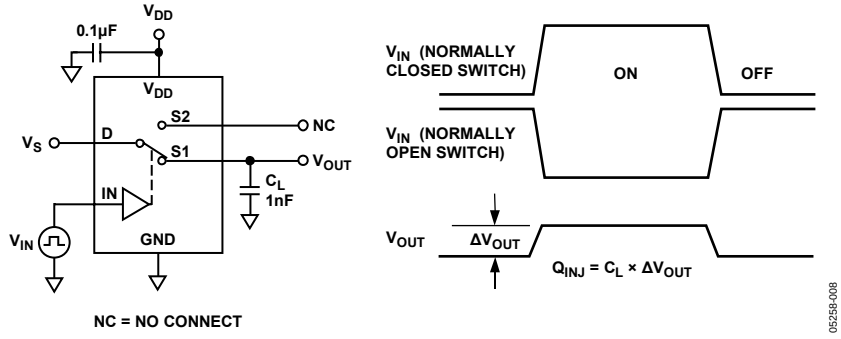

Figure 21. Charge Injection

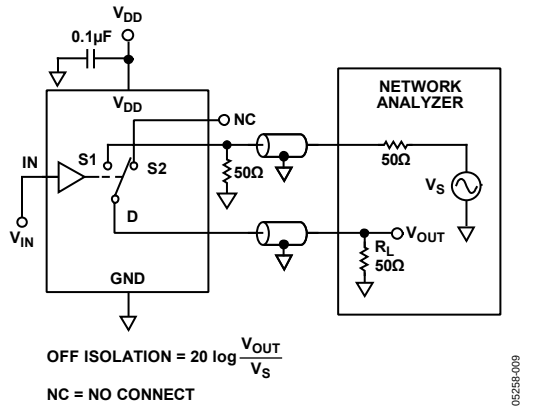

Figure 22. Off Isolation

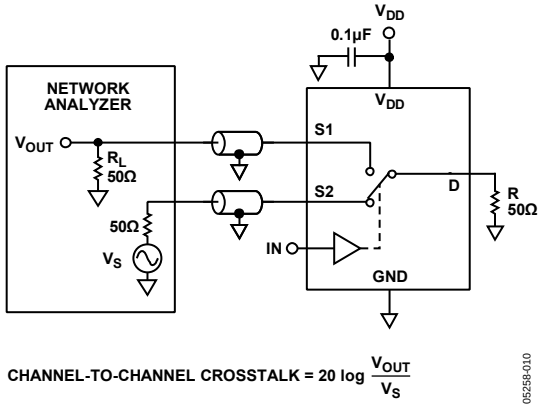

Figure 23. Channel-to-Channel Crosstalk

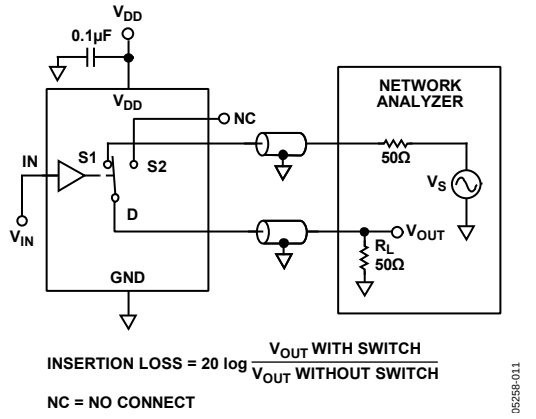

Figure 24. Bandwidth

TERMINOLOGY

V_{DD}
Most positive power supply potential.

I_{DD}
Positive supply current.

GND
Ground (0 V) reference.

S
Source terminal. Can be an input or an output.

D
Drain terminal. Can be an input or an output.

IN
Logic control input.

V_D (V_S)
Analog voltage on the D and S terminals.

R_{ON}
Ohmic resistance between the D and S terminals.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}
On resistance mismatch between any two channels.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (Off)
Off switch source capacitance. Measured with reference to ground.

C_D (Off)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

–3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of harmonic amplitudes plus noise of a signal to the fundamental.

OUTLINE DIMENSIONS

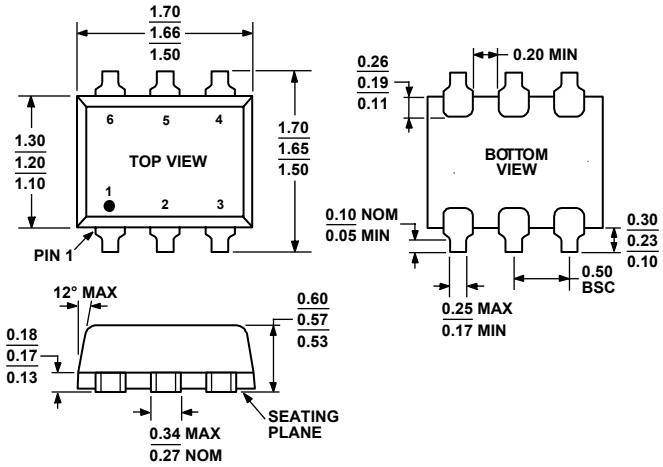

Figure 25. 6-Lead Small Outline Transistor Package [SOT-66]
(RY-6-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG859YRYZ-REEL[2]	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-66]	RY-6-1	04
ADG859YRYZ-REEL7[2]	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-66]	RY-6-1	04
ADG859BRYZ-REEL[2]	−40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-66]	RY-6-1	02
ADG859BRYZ-REEL7[2]	−40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-66]	RY-6-1	02
EVAL-ADG859EB		Evaluation Board		

[1] Branding on this package is limited to two characters due to space constraints.
[2] Z = Pb-free part.

NOTES

NOTES

NOTES

D05258-0-12/06(A)