

FEATURES

- 2 differential DSL channels comprising current feedback, high output current amplifiers with integrated feedback resistors plus biasing network
- Ideal for use as ADSL/ADSL2+ dual-channel central office (CO) line drivers
- Low power consumption using Class H technology
 - Single 12.5 V supply operation
 - 20.4 dBm line power, 1:1 transformer
 - Less than 600 mW per channel total power dissipation while driving 20.4 dBm (includes 110 mW line power)
 - Less than 275 mW per channel total power dissipation while driving 14.5 dBm (including line power)
- High output voltage and current drive
 - 43.4 V differential output voltage swing
- Low distortion
 - 65 dBc typical multitone power ratio (MTPR) at 20.4 dBm, 26 kHz to 2.2 MHz
- Low cost protection components enable ITU-T-K20 and GR-1089 compliance

APPLICATIONS

ADSL/ADSL2+ CO line drivers

GENERAL DESCRIPTION

The **ADLD8403** comprises two differential, high output current, low power consumption operational amplifiers. It is particularly well suited for the CO driver interface in digital subscriber line systems, such as ADSL and ADSL2+. The driver can deliver 20.4 dBm to a line while compensating for losses due to hybrid insertion and back termination resistors. The **ADLD8403** uses the Analog Devices, Inc., second generation Adaptive Linear Power™ (Class H) architecture to achieve unprecedented power efficiency using a single power supply. Additional functionality allows the shutdown of pumps for enhanced power savings for line powers of less than 14.5 dBm. This functionality yields the smallest printed circuit board (PCB) footprint and lowest total cost of ownership.

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the **ADLD8403** to be the CO line driver in ADSL and other xDSL systems.

INTERNAL SCHEMATIC

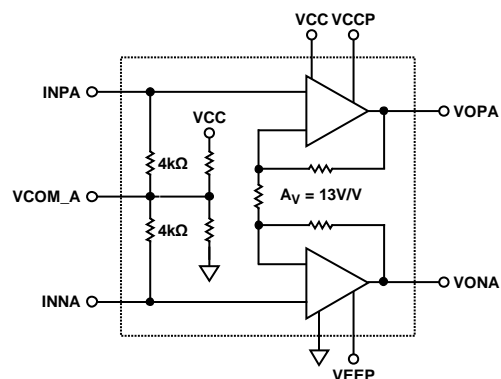


Figure 1. Channel A Internal Schematic

The **ADLD8403** is available in a 4 mm × 4 mm, 20-lead LFCSP.

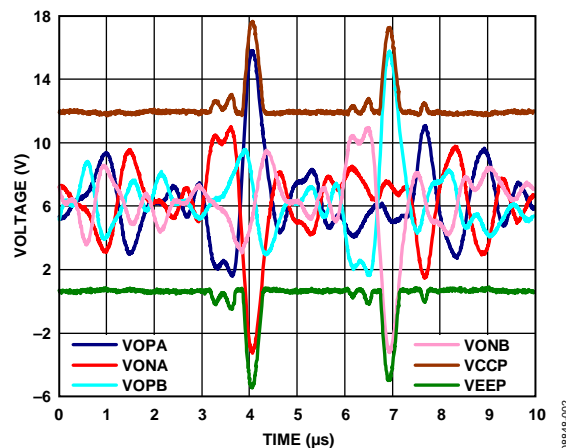


Figure 2. Outputs and Pumps Time Domain Response, Typical ADSL/ADSL2+ Application Circuit, $V_{CC} = 12.5\text{ V}$, $P_{OUT} = 20.4\text{ dBm}$, Crest Factor = 5.45

Rev. D

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ADLD8403* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/08/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADLD8403: Ultralow Power, Adaptive Linear Power, Dual-Port ADSL/ADSL2+ Line Driver Data Sheet

DESIGN RESOURCES

- ADLD8403 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADLD8403 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

3/2017—Rev. C to Rev. D

Changed LFCSP_WQ to LFCSP	Throughout
Change to Table 3	4
Updated Outline Dimensions	10
Changes to Ordering Guide	10

9/2014—Revision C: Initial Version

SPECIFICATIONS

$V_{CC} = 12.5\text{ V}$, $R_L = 100\ \Omega$, $G_{DIFF} = 13$ (fixed), $PD_A = 0$, $PD_B = 0$, $T = 25^\circ\text{C}$, typical DSL application circuit, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth		8		MHz	$V_{OUT} = 0.1\text{ V p-p}$, differential
–3 dB Large Signal Bandwidth		8		MHz	$V_{OUT} = 2\text{ V p-p}$, differential
Differential Gain	12.8	13	13.2	V/V	
NOISE/DISTORTION PERFORMANCE					
Multitone Power Ratio (MTPR)		–65		dBc	26 kHz to 2.2 MHz, $Z_{LINE} = 100\ \Omega$, differential load
Differential Output Noise		120		nV/ $\sqrt{\text{Hz}}$	$f = 10\text{ kHz}$
INPUT CHARACTERISTICS					
Referred to Output (RTO) Offset Voltage		<100		mV	Single-ended
		15	200	mV	Differential
Input Resistance		8		k Ω	Differential
Input Capacitance		1		pF	Differential
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing		43.4		V	ΔV_{OUT} , $R_L = 100\ \Omega$
POWER SUPPLY					
Operating Range, Single Supply	11.75	12.5		V	
Total Quiescent Current					Full chip
PD_A = 0, PD_B = 0, PD_PMP = 0		35.6	38	mA	Pumps are on, both channels active
PD_A = 0, PD_B = 0, PD_PMP = 1		22.0	25	mA	Pumps are off, both channels active
PD_A = 0, PD_B = 1, PD_PMP = 0		21.0	23.5	mA	Pumps are on, one channel active
PD_A = 0, PD_B = 1, PD_PMP = 1		10.6	13	mA	Pumps are off, one channel active
PD_A = 1, PD_B = 1		2.5	3.5	mA	Pumps are off, both channels inactive
Common-Mode Voltage		20		mV	With respect to midsupply
Threshold					
PD_A = 0, PD_B = 0			0.8	V	
PD_A = 1, PD_B = 1	2.4			V	
Input Current					
PD_A = 0, PD_B = 0		35	60	μA	0 \equiv 0.8 V
PD_A = 1, PD_B = 1		5	10	μA	1 \equiv 2.4 V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{CC}	13.2 V
Power Dissipation	See Figure 3
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified in still air with the exposed pad soldered to a 4-layer JEDEC test board. θ_{JC} is specified at the exposed pad.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP (CP-20-8)	36.1	5.7	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the [ADLD8403](#) is limited by its junction temperature on the die.

The maximum safe junction temperature of plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is 150°C. Exceeding this limit may temporarily cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding this limit for an extended period can result in device failure.

Figure 3 shows the maximum power dissipation in the package vs. the ambient temperature for the 20-lead LFCSP on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

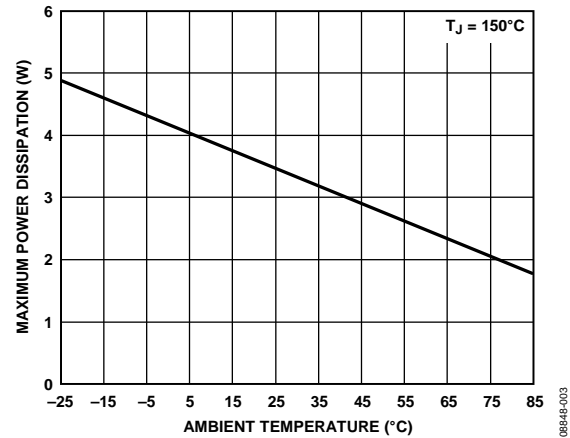


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

The power dissipated in the package (P_D) is easily computed by taking the total power consumed while driving a signal and subtracting the power dissipated in the load. The total power consumed is simply the product of the voltage between the supply pins (V_{CC} , $VEEP$, and V_{CCP}) times the supply current (I_s). Use rms voltages and currents.

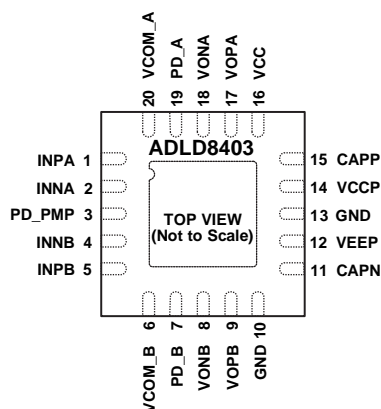
Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more copper in direct contact with the package leads from PCB traces, through holes, ground, and power planes reduces θ_{JA} .

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. CONNECT THE EXPOSED PAD TO THE GND PLANE FOR THE THERMAL PATH. NO INTERNAL ELECTRICAL CONNECTION EXISTS.

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Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INPA	Port A Input P
2	INNA	Port A Input N
3	PD_PMP	Control for Port A and Port B Pumps
4	INNB	Port B Input N
5	INPB	Port B Input P
6	VCOM_B	Port B V_{COM}
7	PD_B	Port B Shutdown
8	VONB	Port B Output N
9	VOPB	Port B Output P
10	GND	Ground
11	CAPN	Pump Capacitor Negative
12	VEEP	Dynamic Negative Supply
13	GND	Ground
14	VCCP	Dynamic Positive Supply
15	CAPP	Pump Capacitor Positive
16	VCC	Positive Power Supply
17	VOPA	Port A Output P
18	VONA	Port A Output N
19	PD_A	Port A Shutdown
20	VCOM_A	Port A V_{COM}
	EPAD	Exposed Pad. Connect the exposed pad to the GND plane for the thermal path. No internal electrical connection exists.

TYPICAL PERFORMANCE CHARACTERISTICS

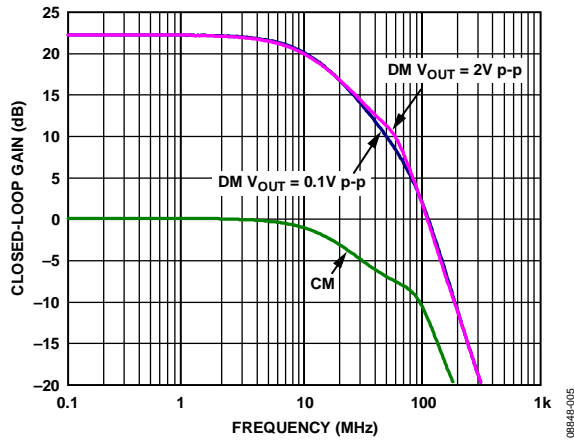
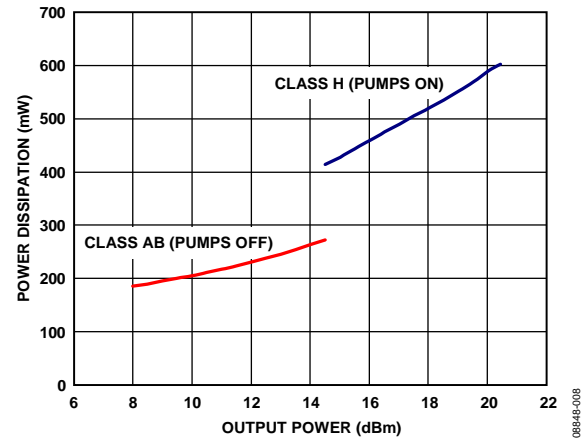
Figure 5. Closed-Loop Gain vs. Frequency, $R_L = 100\ \Omega$ 

Figure 8. Power Dissipation per Channel vs. Output Power; Includes Line Power

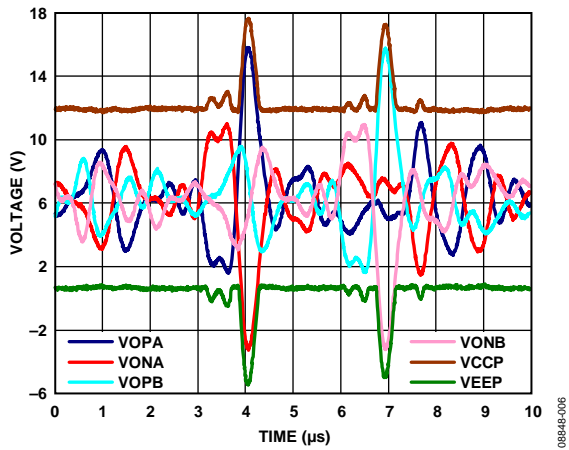
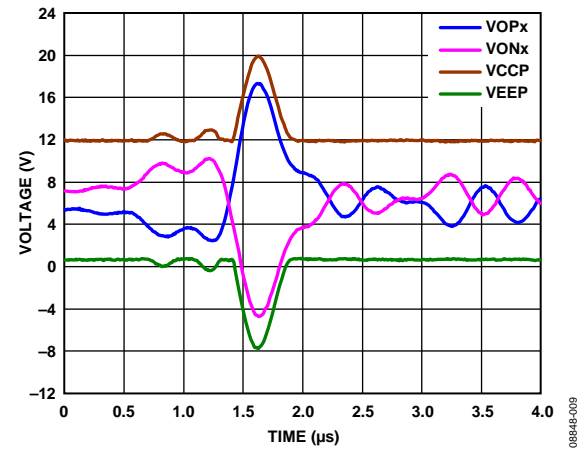
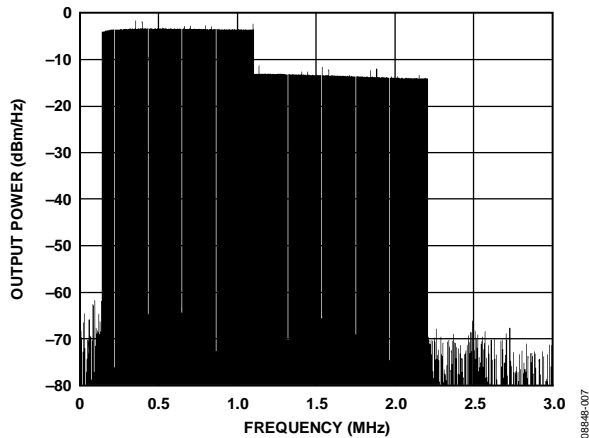
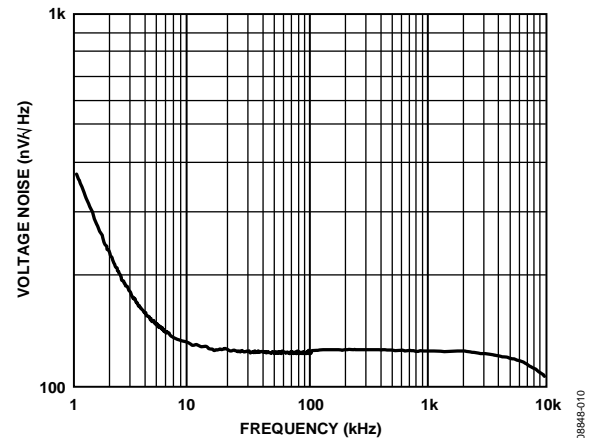
Figure 6. Outputs and Pumps Time Domain Response, Typical ADSL/ADSL2+ Application Circuit, $V_{CC} = 12.5\ V$, $P_{OUT} = 20.4\ dBm$, Crest Factor = 5.45Figure 9. Outputs and Pumps Time Domain Response, Typical ADSL/ADSL2+ Application Circuit, $V_{CC} = 12.5\ V$, $P_{OUT} = 19.8\ dBm$, Crest Factor = 6.9Figure 7. Multitone Power Ratio (MTPR), Typical ADSL/ADSL2+ Application Circuit, $V_{CC} = 12.5\ V$, $P_{OUT} = 20.4\ dBm$, Crest Factor = 5.45

Figure 10. Differential Output Voltage Noise vs. Frequency

THEORY OF OPERATION

A Class H DSL line driver achieves power savings by using internally developed, signal tracking, power supplies. These tracking power supplies are derived from a single V_{CC} power supply of 12.5 V nominal. The power savings occur due to minimum headroom provided by the tracking, or pumped, supplies to ensure nonsaturation of the output buffer amplifier. For Class H drivers, the average total power that the amplifier consumes is lower than that of conventional Class AB amplifier architectures using a fixed supply.

The ADLD8403 is the second implementation of a patented amplifier architecture developed by Analog Devices. This new architecture, known as Adaptive Linear Power (ALP), is optimized to process signals with occasional peaks that are much greater than the rms level, such as the discrete multitone (DMT) signals used in xDSL applications. Figure 11 shows the ADLD8403 block diagram. Included are two Class AB current feedback (CFB) amplifiers, along with the ALP unit and standard bias block. The architecture combines Class AB amplifiers with the ALP to provide a system that generates internal supplies (V_{CCP} and V_{EEP}) that move linearly with the input signal. This movement is

achieved by sampling the input signal via the input pins, $INPA$ and $INNA$, and applying the appropriate gain to create the variable supplies at the V_{CCP} and V_{EEP} pins.

The ADLD8403 contains two complete channels of ADSL2+ compliant drivers. Each channel has a power mode signal, or PD pin (PD_A and PD_B), that enables the output buffer. Additionally, in applications where less than 14.5 dBm of line power is required, a third PD_PMP signal is used to disable the signal tracking, power supplies. This feature reduces power consumption by approximately 125 mW for these reduced line powers. Because both channels share the pumped supplies in the ADLD8403, the PD_PMP pin is used only when both channels require less than 14.5 dBm of line power.

The ADLD8403 is intended for use in digital subscriber line access multiplexor (DSLAM) applications. The ADLD8403 a simple process and allows for ease of upgrading existing DSLAM systems.

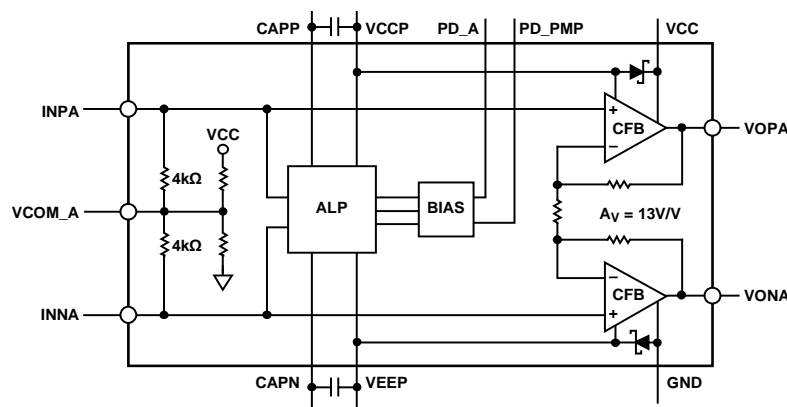


Figure 11. Block Diagram

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MULTITONE POWER RATIO (MTPR)

The DMT signal used in ADSL/ADSL2+ systems carries data in discrete tones or bins, which appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, the MTPR is commonly used to measure ac linearity. In general, designers are concerned with two types of MTPR: in-band and out-of-band. In-band MTPR is the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent empty tone. Out-of-band MTPR is the spurious emissions that occur in bands just below and above the transmit band. For ADSL2+ applications, the out-of-band MTPR is the receive band between 25.875 kHz and 138 kHz and the region above 2.208 MHz. Figure 13 shows the out-of-band MTPR for the ADLD8403.

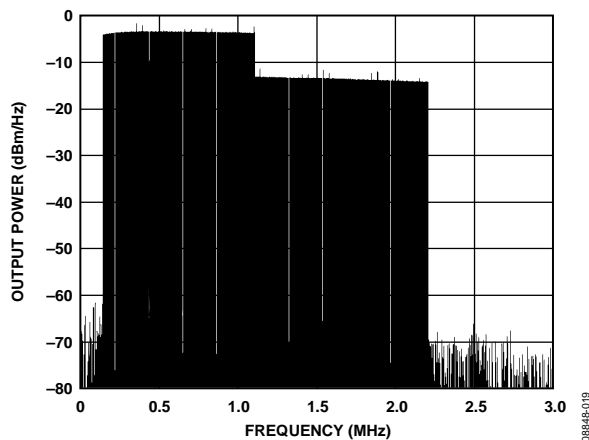


Figure 13. Out-of-Band MTPR

LIGHTNING AND AC POWER FAULT

As an ADSL/ADSL2+ line driver, the ADLD8403 is transformer coupled to the twisted pair telephone line. In this environment, the ADLD8403 is subject to large line transients resulting from events such as lightning strikes or downed power lines. Additional circuitry is required to protect the ADLD8403 from damage due to these events.

OUTLINE DIMENSIONS

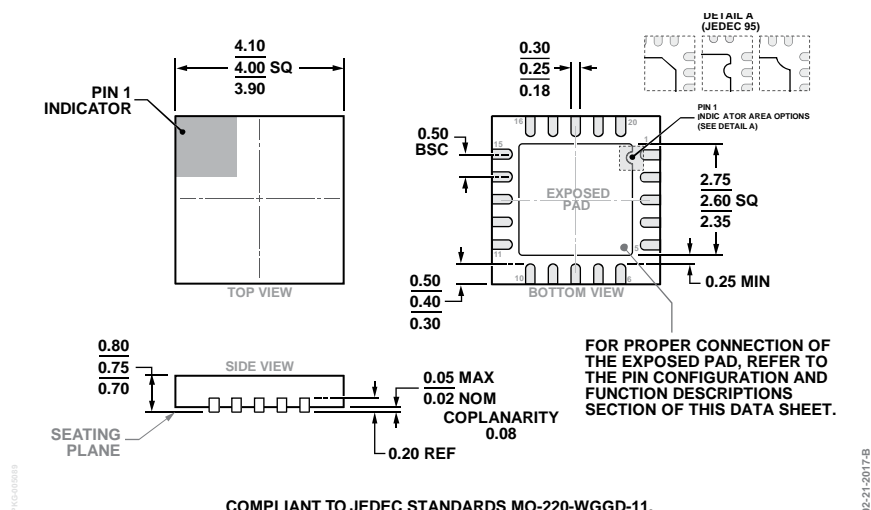


Figure 14. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADLD8403ACPZ-R2	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
ADLD8403ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
ADLD8403ACPZ-RL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8

¹ Z = RoHS Compliant Part.