

### FEATURES

**Input sensitivity: 3.5 mV p-p**  
**70 ps rise/fall times**  
**CML outputs: 750 mV p-p differential**  
**Bandwidth selectable for multirate 1×/2×/4× FC modules**  
**Optional LOS output inversion**  
**Programmable LOS detector: 3.5 mV to 35 mV**  
**Rx signal strength indicator (RSSI)**  
**SFF-8472-compliant average power measurement**  
**Single-supply operation: 3.3 V**  
**Low power dissipation: 160 mW**  
**Available in space-saving, 3 mm × 3 mm, 16-lead LFCSP**  
**Extended temperature range: –40°C to +95°C**  
**SFP reference design available**

### APPLICATIONS

**1×, 2×, and 4× FC transceivers**  
**SFP/SFF/GBIC optical transceivers**  
**GbE transceivers**  
**Backplane receivers**

### GENERAL DESCRIPTION

The ADN2892 is a 4.25 Gbps limiting amplifier with integrated loss of signal (LOS) detection circuitry and a received signal strength indicator (RSSI). This part is optimized for Fibre Channel (FC) and Gigabit Ethernet (GbE) optoelectronic conversion applications. The ADN2892 has a differential input sensitivity of 3.5 mV p-p and accepts up to a 2.0 V p-p differential input overload voltage. The ADN2892 has current mode logic (CML) outputs with controlled rise and fall times.

The ADN2892 has a selectable low-pass filter with a –3 dB cutoff frequency of 1.5 GHz. By setting BW\_SEL to Logic 0, the filter can limit the relaxation oscillation of a low cost CD laser used in a legacy 1 Gbps FC transmitter. The limited BW also reduces the rms noise and in turn improves the receiver optical sensitivity for a lower data rate application, such as 1× FC and GbE.

By monitoring the bias current through a photodiode, the on-chip RSSI detector measures the average power received with 2% typical linearity over the entire valid input range of the photodiode. The on-chip RSSI detector facilitates SFF-8472-compliant optical transceivers by eliminating the need for external RSSI detector circuitry.

Additional features include a programmable loss-of-signal (LOS) detector and output squelch. The ADN2892 is available in a 3 mm × 3 mm, 16-lead LFCSP.

### FUNCTIONAL BLOCK DIAGRAM

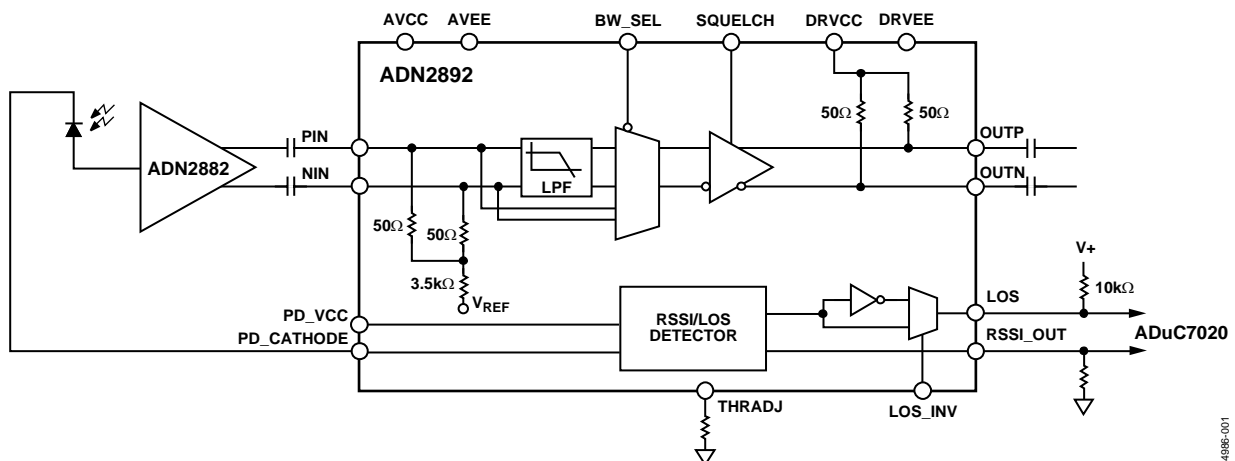


Figure 1. RSSI Function Capable—Applications Setup Block Diagram

04935-001

Rev. C

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADN2892 Evaluation Board

## DOCUMENTATION

### Data Sheet

- ADN2892: 3.3 V, 4.25 Gbps, Limiting Amplifier Data Sheet

## REFERENCE MATERIALS

### Informational

- Optical and High Speed Networking ICs
- SFP Chipset and Reference Design Simplify 4.25 GBPS Transceivers

## DESIGN RESOURCES

- ADN2892 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

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## SAMPLE AND BUY

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## TABLE OF CONTENTS

|   |    |   |    |
|---|----|---|----|
| Features .....                                    | 1  | Limiting Amplifier .....                        | 10 |
| Applications .....                                | 1  | Loss-of-Signal (LOS) Detector .....             | 10 |
| General Description .....                         | 1  | Received Signal Strength Indicator (RSSI) ..... | 10 |
| Functional Block Diagram .....                    | 1  | Squelch Mode .....                              | 10 |
| Revision History .....                            | 2  | BW_SEL (Bandwidth Selection) Mode .....         | 10 |
| Specifications .....                              | 3  | LOS_INV (Lose of Signal_Invert) Mode .....      | 10 |
| Absolute Maximum Ratings .....                    | 5  | Applications Information .....                  | 11 |
| Thermal Resistance .....                          | 5  | PCB Design Guidelines .....                     | 11 |
| ESD Caution .....                                 | 5  | Pad Coating and Pb-Free Soldering .....         | 12 |
| Pin Configuration and Function Descriptions ..... | 6  | Outline Dimensions .....                        | 13 |
| Typical Performance Characteristics .....         | 7  | Ordering Guide .....                            | 13 |
| Theory of Operation .....                         | 10 |   |    |

## REVISION HISTORY

### 3/2017—Rev. B to Rev. C

|                                  |    |
|----------------------------------|----|
| Changes to Figure 2 .....        | 6  |
| Changes to Figure 18 .....       | 11 |
| Updated Outline Dimensions ..... | 13 |
| Changes to Ordering Guide .....  | 13 |

### 2/2014—Rev. A to Rev. B

|                           |   |
|---------------------------|---|
| Changes to Figure 2 ..... | 6 |
|---------------------------|---|

### 7/2013—Rev. 0 to Rev. A

|   |    |
|---|----|
| Change to Output Voltage Swing Parameter, Table 1 ..... | 3  |
| Changes to Figure 2 .....                               | 6  |
| Updated Outline Dimensions .....                        | 13 |
| Changes to Ordering Guide .....                         | 13 |

### 4/2005—Revision 0: Initial Version

## SPECIFICATIONS

Test Conditions:  $V_{CC} = 2.9 \text{ V}$  to  $3.6 \text{ V}$ ,  $V_{EE} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+95^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                             | Min            | Typ  | Max            | Unit              | Test Conditions/Comments  |
|---------------------------------------|----------------|------|----------------|-------------------|---|
| QUANTIZER DC CHARACTERISTICS          |                |      |                |                   |   |
| Input Voltage Range                   | $V_{CC} - 1.2$ |      | $V_{CC} - 0.2$ | V                 | At PIN or NIN, dc-coupled   |
| Input Common Mode                     | 2.1            |      | 2.7            | V                 | DC-coupled  |
| Peak-to-Peak Differential Input Range |                |      | 2.0            | V p-p             | PIN – NIN, ac-coupled   |
| Input Sensitivity                     | 6.6            | 3.5  |                | mV p-p            | PIN – NIN, BER $\leq 1 \times 10^{-10}$   |
| Input Offset Voltage                  |                | 100  |                | $\mu\text{V}$     |   |
| Input RMS Noise                       |                | 235  |                | $\mu\text{V rms}$ |   |
| Input Resistance                      |                | 50   |                | $\Omega$          | Single-ended  |
| Input Capacitance                     |                | 0.65 |                | pF                |   |
| QUANTIZER AC CHARACTERISTICS          |                |      |                |                   |   |
| Input Data Rate                       | 1.0            |      | 4.25           | Gbps              |   |
| Small Signal Gain                     |                | 51   |                | dB                | Differential  |
| S11                                   |                | -10  |                | dB                | Differential, $f < 4.25 \text{ GHz}$  |
| S22                                   |                | -10  |                | dB                | Differential, $f < 4.25 \text{ GHz}$  |
| Random Jitter                         |                | 3.0  | 3.9            | ps rms            | Input $\geq 10 \text{ mV p-p}$ , 4× FC, K28.7 pattern                             |
| Deterministic Jitter                  |                | 10   | 21.0           | ps p-p            | Input $\geq 10 \text{ mV p-p}$ , 4× FC, K28.5 pattern                             |
| Low Frequency Cutoff                  |                | 30   |                | kHz               |   |
| Power Supply Rejection                |                | 45   |                | dB                | $100 \text{ kHz} < f < 10 \text{ MHz}$  |
| LOSS OF SIGNAL DETECTOR (LOS)         |                |      |                |                   |   |
| LOS Assert Level                      | 2.9            | 3.5  | 4.8            | mV p-p            | $R_{THRADJ} = 100 \text{ k}\Omega$  |
|                                       | 22.4           | 35   | 55.0           | mV p-p            | $R_{THRADJ} = 1 \text{ k}\Omega$  |
| Electrical Hysteresis                 | 2.5            | 5.0  |                | dB                | 1.0 Gbps, PRBS $2^{23} - 1$   |
|                                       | 2.8            | 5.0  |                | dB                | 4× FC, PRBS $2^{23} - 1$  |
| LOS Assert Time                       |                | 950  |                | ns                | DC-coupled  |
| LOS Deassert Time                     |                | 62   |                | ns                | DC-coupled  |
| RSSI                                  |                |      |                |                   |   |
| Input Current Range                   | 5              |      | 1000           | $\mu\text{A}$     |   |
| RSSI Output Linearity                 |                | 2    |                | %                 | $5 \mu\text{A} \leq I_{IN} \leq 1000 \mu\text{A}$                                 |
| Gain                                  |                | 1.0  |                | mA/mA             | $I_{RSSI}/I_{PD\_CATHODE}$  |
| Offset                                |                | 145  |                | nA                |   |
| Compliance Voltage (At PD_CATHODE)    | $V_{CC} - 0.4$ |      |                | V                 | $I_{PD\_CATHODE} = 5 \mu\text{A}$   |
|                                       | $V_{CC} - 0.9$ |      |                | V                 | $I_{PD\_CATHODE} = 1000 \mu\text{A}$  |
| BW_SEL (BANDWIDTH SELECTION)          |                |      |                |                   |   |
| Channel Bandwidth                     |                | 1.5  |                | GHz               | -3 dB cutoff frequency of the on-chip, two-pole, low-pass filter, when BW_SEL = 0 |
| POWER SUPPLIES                        |                |      |                |                   |   |
| $V_{CC}$                              | 2.9            | 3.3  | 3.6            | V                 |   |
| $I_{CC}$                              |                | 48   | 54             | mA                |   |
| OPERATING TEMPERATURE RANGE           |                |      |                |                   |   |
|                                       | -40            | +25  | +95            | $^\circ\text{C}$  | $T_{MIN}$ to $T_{MAX}$  |
| CML OUTPUT CHARACTERISTICS            |                |      |                |                   |   |
| Output Impedance                      |                | 50   |                | $\Omega$          | Single-ended  |
| Output Voltage Swing                  | 600            | 750  | 940            | mV p-p            | Differential  |
| Output Rise and Fall Time             |                | 70   | 103            | ps                | 20% to 80%  |

| Parameter                                   | Min | Typ | Max | Unit          | Test Conditions/Comments   |
|---|-----|-----|-----|---------------|--|
| LOGIC INPUTS (SQUELCH, LOS_INV, AND BW_SEL) |     |     |     |               |  |
| $V_{IH}$ , Input High Voltage               | 2.0 |     |     | V             |  |
| $V_{IL}$ , Input Low Voltage                |     |     | 0.8 | V             |  |
| Input Current (SQUELCH, LOS_INV)            |     |     | 39  | $\mu\text{A}$ | $I_{INH}$ , $V_{IN} = 2.4\text{ V}$ , 100 k $\Omega$ pull-down, on-chip resistor |
| Input Current (BW_SEL)                      |     |     | -38 | $\mu\text{A}$ | $I_{INL}$ , $V_{IN} = 0.0\text{ V}$ , 100 k $\Omega$ pull-up, on-chip resistor   |
| LOGIC OUTPUTS (LOS)                         |     |     |     |               |  |
| $V_{OH}$ , Output High Voltage              | 2.4 |     |     | V             | Open drain output, 4.7 k $\Omega$ – 10 k $\Omega$ pull-up resistor to VCC        |
| $V_{OL}$ , Output Low Voltage               |     |     | 0.4 | V             | Open drain output, 4.7 k $\Omega$ – 10 k $\Omega$ pull-up resistor to VCC        |

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter                                | Rating          |
|--|-----------------|
| Power Supply Voltage                     | 4.2 V           |
| Minimum Voltage (All Inputs and Outputs) | VEE – 0.4 V     |
| Maximum Voltage (All Inputs and Outputs) | VCC + 0.4 V     |
| Storage Temperature                      | –65°C to +150°C |
| Operating Temperature Range              | –40°C to +95°C  |
| Production Soldering Temperature         | J-STD-20        |
| Junction Temperature                     | 125°C           |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for 4-layer PCB with exposed paddle soldered to GND.

Table 3.

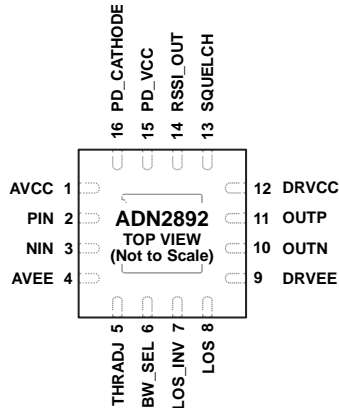
| Package Type               | $\theta_{JA}$ | Unit |
|----------------------------|---------------|------|
| 3 mm × 3 mm, 16-lead LFCSP | 28            | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



### NOTES

1. THERE IS AN EXPOSED PAD ON THE BOTTOM OF THE PACKAGE THAT MUST BE CONNECTED TO THE GND PLANE WITH FILLED VIAS.

04986-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No.     | Mnemonic   | I/O Type <sup>1</sup> | Description  |
|-------------|------------|-----------------------|--|
| 1           | AVCC       | P                     | Analog Power Supply.   |
| 2           | PIN        | AI                    | Differential Data Input, Positive Port, 50 $\Omega$ On-Chip Termination.   |
| 3           | NIN        | AI                    | Differential Data Input, Negative Port, 50 $\Omega$ On-Chip Termination.   |
| 4           | AVEE       | P                     | Analog Ground.   |
| 5           | THRAdj     | AO                    | LOS Threshold Adjust Resistor.   |
| 6           | BW_SEL     | DI                    | With one 100 k $\Omega$ on-chip, pull-up resistor, BW_SEL = 0 for 1 $\times$ /2 $\times$ FC, BW_SEL = 1 for 4 $\times$ FC. |
| 7           | LOS_INV    | DI                    | With one 100 k $\Omega$ on-chip, pull-down resistor, LOS_INV = 1 inverts the LOS output to be active low for SFF.          |
| 8           | LOS        | DO                    | LOS Detector Output, Open Collector.   |
| 9           | DRVVEE     | P                     | Output Buffer Ground.  |
| 10          | OUTN       | DO                    | Differential Data Output, CML, Negative Port, 50 $\Omega$ , On-Chip Termination.   |
| 11          | OUTP       | DO                    | Differential Data Output, CML, Positive Port, 50 $\Omega$ , On-Chip Termination.   |
| 12          | DRVCC      | P                     | Output Buffer Power Supply.  |
| 13          | SQUELCH    | DI                    | Disable Outputs, 100 k $\Omega$ On-Chip, Pull-Down Resistor.   |
| 14          | RSSI_OUT   | AO                    | Average Current Output.  |
| 15          | PD_VCC     | P                     | Power Input for RSSI Measurement.  |
| 16          | PD_CATHODE | AO                    | Photodiode Bias Voltage.   |
| Exposed Pad | Pad        | P                     | Connect to Ground.   |

<sup>1</sup> P = power; DI = digital input; DO = digital output; AI = analog input; and AO = analog output.

## TYPICAL PERFORMANCE CHARACTERISTICS

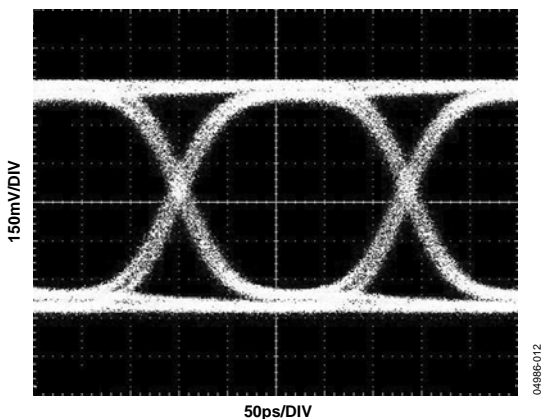


Figure 3. Eye of ADN2892 at 25°C, 4.25 Gbps, and 10 mV Input

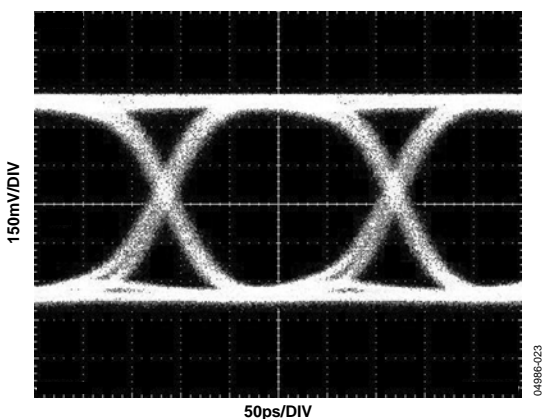


Figure 4. Eye of ADN2892 at 95°C, 4.25 Gbps, and 10 mV Input

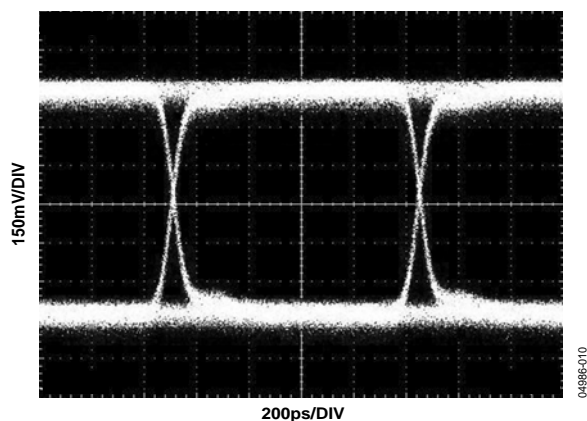
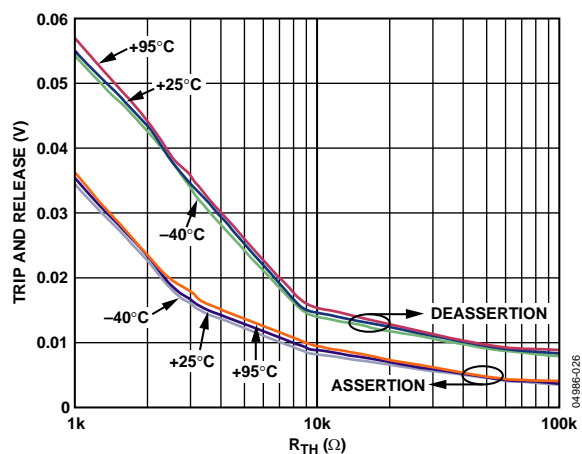
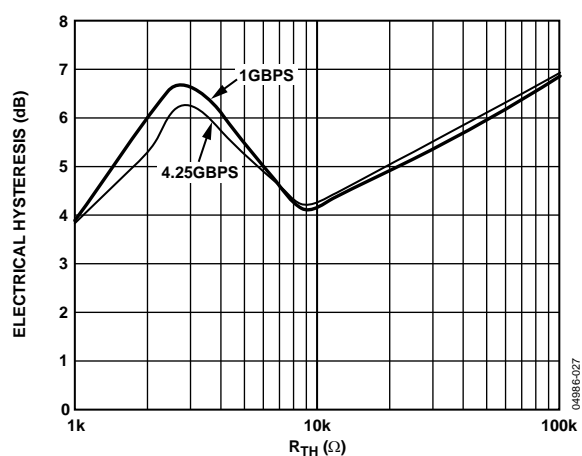
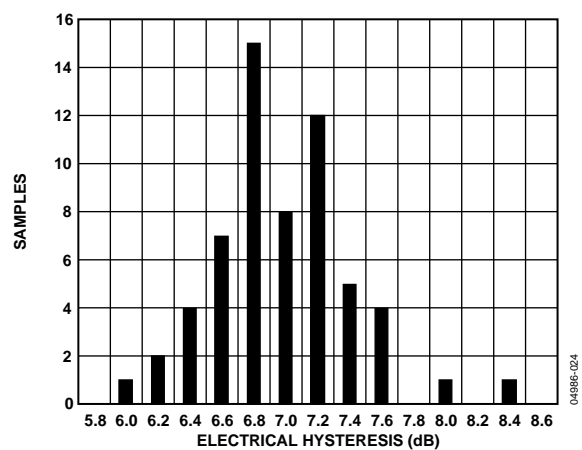


Figure 5. Eye of ADN2892 at 25°C, 1.063 Gbps, and 10 mV Input (BW\_SEL = 0)

Figure 6. LOS Trip and Release vs.  $R_{TH}$  at 4.25 GbpsFigure 7. LOS Electrical Hysteresis vs.  $R_{TH}$  at 25°CFigure 8. Sample Lot Distribution—Worst-Case Condition:  
Conditions = 4.25 Gbps, 100 kΩ at -40°C, 3.6 V



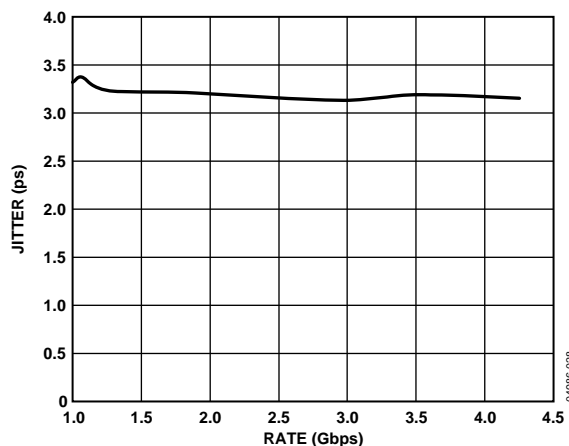


Figure 9. Random Jitter vs. Data Rate

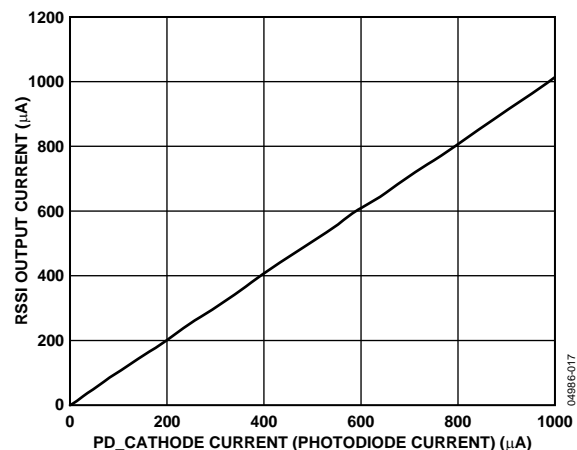


Figure 12. RSSI Output vs. Average Photodiode Current

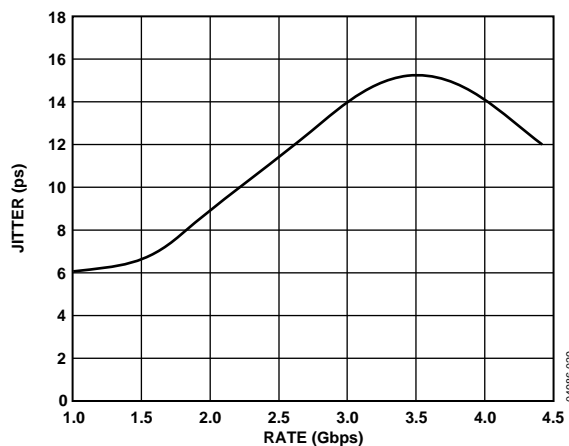


Figure 10. Deterministic Jitter vs. Data Rate

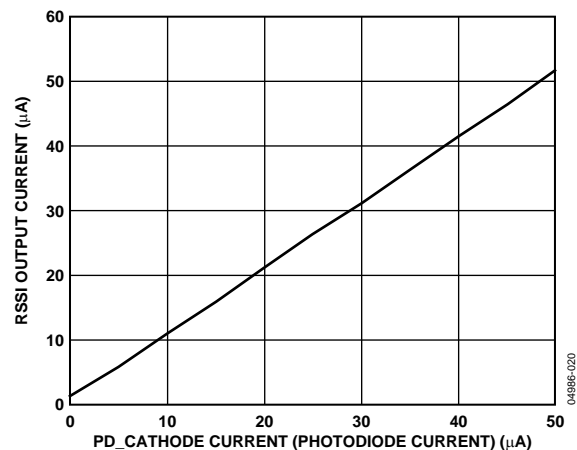


Figure 13. RSSI Output vs. Average Photodiode Current (Zoomed)

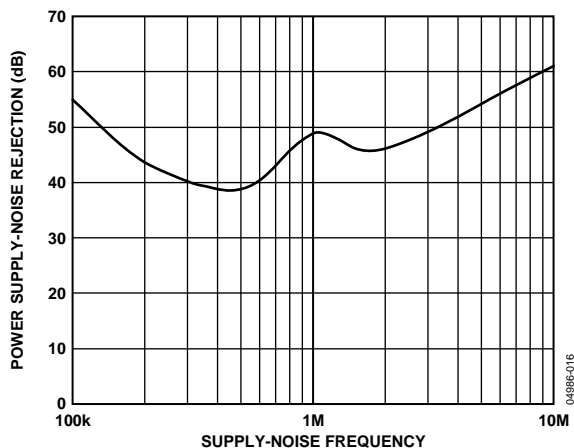


Figure 11. PSRR vs. Supply-Noise Frequency

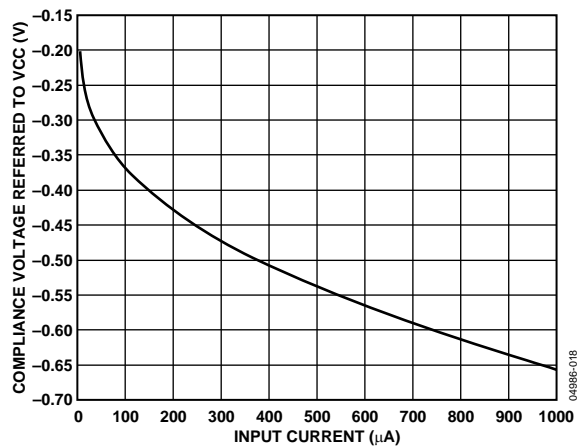


Figure 14. PD\_CATHODE Compliance Voltage vs. Input Current RSSI (Refer to VCC)

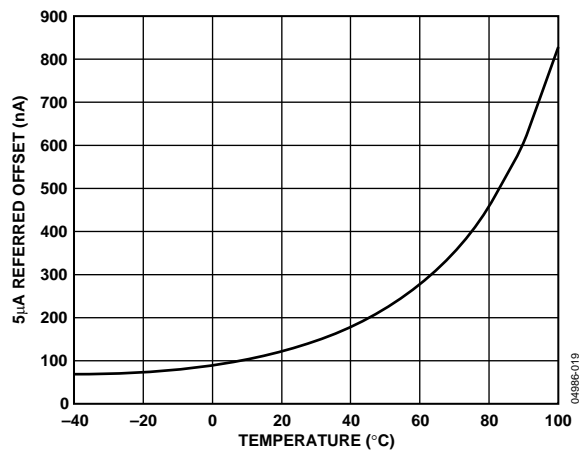


Figure 15. RSSI Offset—Difference Between Measured RSSI Output and PD\_CATHODE (Input) Current of 5  $\mu$ A

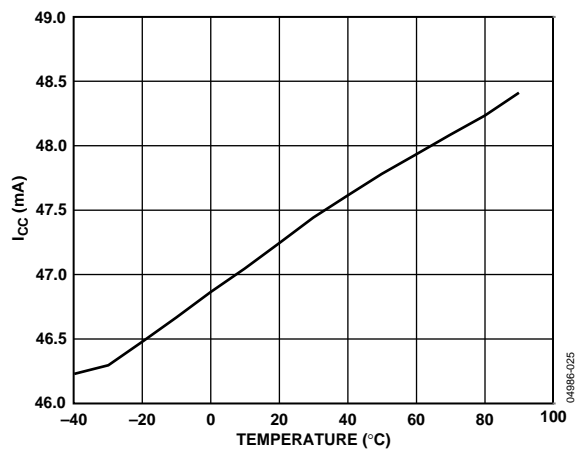


Figure 17. ADN2892 I<sub>CC</sub> Current vs. Temperature

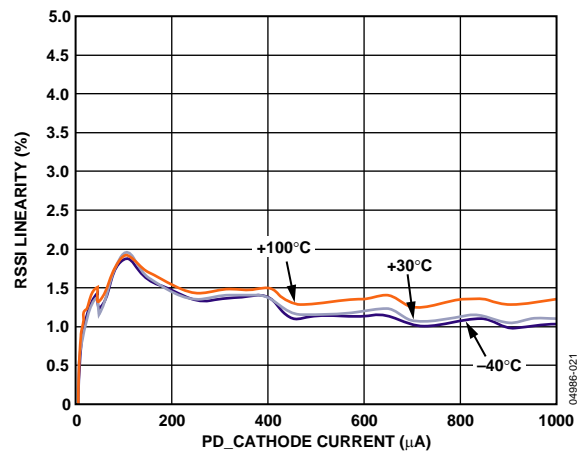


Figure 16. RSSI Linearity % vs. PD\_CATHODE Current

## THEORY OF OPERATION

### LIMITING AMPLIFIER

#### Input Buffer

The ADN2892 limiting amplifier provides differential inputs (PIN/NIN), each with a single-ended, on-chip 50  $\Omega$  termination. The amplifier can accept either dc-coupled or ac-coupled signals; however, an ac-coupled signal is recommended. Using a dc-coupled signal, the amplifier needs a nominal  $V_{CC} - 0.7$  V common-mode voltage and  $\pm 0.5$  V headroom. If the input common-mode voltage is 2.4 V, the available headroom is reduced down to  $\pm 0.3$  V.

The ADN2892 limiting amplifier is a high gain device. It is susceptible to dc offsets in the signal path. The pulse width distortion presented in the NRZ data or a distortion generated by the TIA may appear as dc offset or a corrupted signal to the ADN2892 inputs. An internal offset correction loop can compensate for certain levels of offset.

#### CML Output Buffer

The ADN2892 provides differential CML outputs, OUTP and OUTN. Each output has an internal 50  $\Omega$  termination to VCC.

### LOSS-OF-SIGNAL (LOS) DETECTOR

The on-chip LOS circuit drives LOS to logic high when the input signal level falls below a user-programmable threshold. The threshold level can be set anywhere from 3.5 mV p-p to 35 mV p-p typical by a resistor connected between the THRAdj pin and VEE. See Figure 6 and Figure 7 for the LOS threshold vs. THRAdj. The ADN2892 LOS circuit has an electrical hysteresis greater than 2.5 dB to prevent chatter at the LOS signal. The LOS output is an open-collector output that must be pulled up externally with a 4.7 k $\Omega$  to 10 k $\Omega$  resistor.

### RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

The ADN2892 has an on-chip, RSSI circuit. By monitoring the current supplied to the photodiode, the RSSI circuit provides an accurate, average power measurement. The output of the RSSI is a current that is directly proportional to the average amount of PIN photodiode current. Placing a resistor between the RSSI\_OUT pin and GND converts the current to a GND referenced voltage. This function eliminates the need for external RSSI circuitry for SFF-8472-compliant optical receivers. For more information, see Figure 12 to Figure 16.

Connect the PD\_VCC, PD\_CATHODE, and RSSI\_OUT pins to AVCC to disable the RSSI feature.

### SQUELCH MODE

Driving the SQUELCH input to logic high disables the limiting amplifier outputs. Using LOS output to drive the SQUELCH input, the limiting amplifier outputs stop toggling anytime a signal input level to the limiting amplifier drops below the programmed LOS threshold.

The SQUELCH pin has a 100 k $\Omega$ , internal pull-down resistor.

### BW\_SEL (BANDWIDTH SELECTION) MODE

Driving the BW\_SEL input signal to logic high, the amplifier provides a 3.8 GHz bandwidth. Driving the BW\_SEL input signal to logic low, the amplifier accepts input signals through a 1.5 GHz, 2-pole, low-pass filter that improves receiving sensitivity.

The low-pass filter reduces the possible relaxation oscillation of low speed, low cost laser source by limiting the input signal bandwidth.

The BW\_SEL pin has a 100 k $\Omega$ , on-chip pull-up resistor. Setting the BW\_SEL pin open disables the low-pass filter.

### LOS\_INV (LOSE OF SIGNAL\_INVERT) MODE

Some applications, such as SFF, need the LOS assertion and deassertion voltage reversed. When the LOS\_INV pin is pulled to logic high, the LOS output assertion is pulled down to electrical low.

The LOS\_INV pin has a 100 k $\Omega$  on-chip, pull-down resistor.

## APPLICATIONS INFORMATION

### PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used to ensure optimal performance.

#### Output Buffer Power Supply and Ground Planes

Pin 9 (DRVEE) and Pin 12 (DRVCC) are the power supply and ground pins that provide current to the differential output buffer. To reduce possible series inductance, Pin 9, which is the ground return of the output buffer, should connect to ground directly. If the ground plane is an internal plane and connections to the ground plane are vias, multiple vias in parallel to ground can reduce series inductance.

Similarly, to reduce the possible series inductance, Pin 12, which supplies power to the high speed differential OUTP/OUTN output buffer, should connect to the power plane directly. If the power plane is an internal plane and connections to the power plane are vias, multiple vias in parallel can reduce the series inductance, especially on Pin 12. See Figure 18 for the recommended connections.

The exposed pad should connect to the GND plane using filled vias so that solder does not leak through the vias during reflow. Using filled vias in parallel under the package greatly reduces the thermal resistance and enhances the reliability of the connectivity of the exposed pad to the GND plane during reflow.

To reduce power supply noise, a 10  $\mu\text{F}$  electrolytic decoupling capacitor between power and ground should be close to where the 3.3 V supply enters the PCB. The other 0.1  $\mu\text{F}$  and 1 nF ceramic chip decoupling capacitors should be close to the VCC and VEE pins to provide optimal supply decoupling and a shorter current return loop.

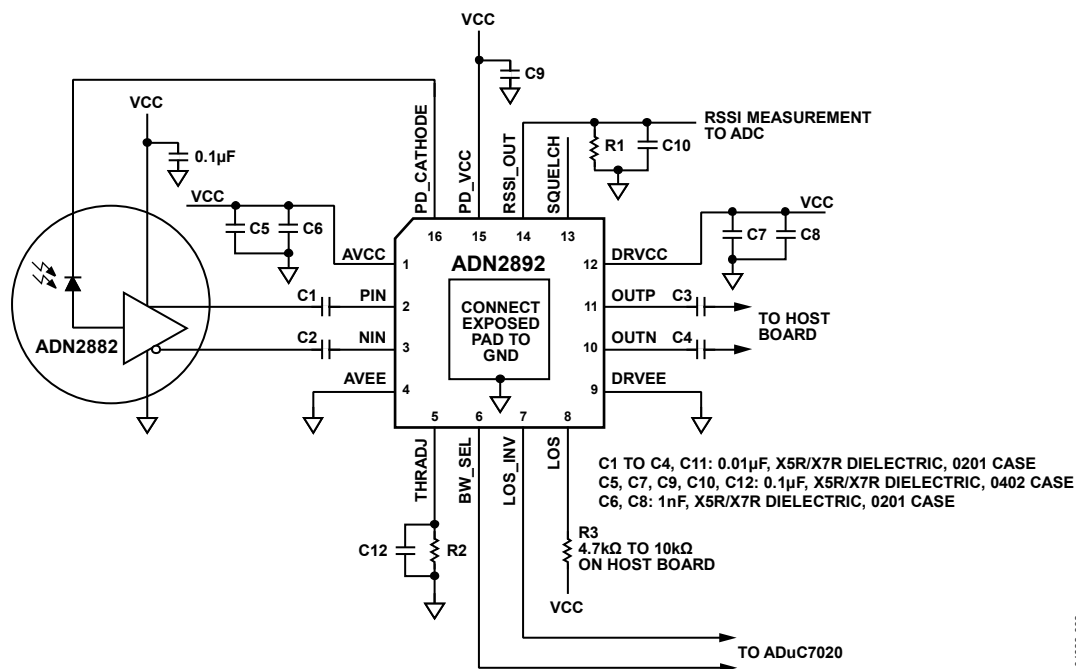


Figure 18. Typical ADN2892 Applications Circuit

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PCB Layout

Figure 19 shows the recommended PCB layout. The 50 Ω transmission lines are the traces that bring the high frequency input and output signals (PIN, NIN, OUTP, and OUTN) from a terminated source to a terminated load with minimum reflection. To avoid a signal skew between the differential traces, each differential PIN/NIN and OUTP/OUTN pair should have matched trace lengths from a differential source to a differential load. C1, C2, C3, and C4 are ac coupling capacitors in series with the high speed, signal input/output paths. To minimize the possible mismatch, the ac coupling capacitor pads should be the same width as the 50 Ω transmission line trace width. To reduce supply noise, a 1 nF decoupling capacitor should be placed as close as possible to the VCC pins on the same layer and not through vias. A 0.1 μF decoupling capacitor can be placed on the bottom of the PCB directly underneath the 1 nF capacitor. All high speed, CML outputs have internal 50 Ω resistor termination between the output pin and VCC. The high speed inputs, PIN and NIN, also have the internal 50 Ω termination to an internal reference voltage.

As with any high speed, mixed-signal design, keep all high speed digital traces away from sensitive analog nodes.

Soldering Guidelines for the LFCSP

The lands on the 16-lead LFCSP are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central exposed pad. The pad on the printed circuit board should be at least as large as the exposed pad. Users must connect the exposed pad to VEE using filled vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

PAD COATING AND PB-FREE SOLDERING

Table 5.

| Pad Coating              | Matt-Tin  |
|--------------------------|-----------|
| Pb-Free Reflow Portfolio | J-STD-20B |

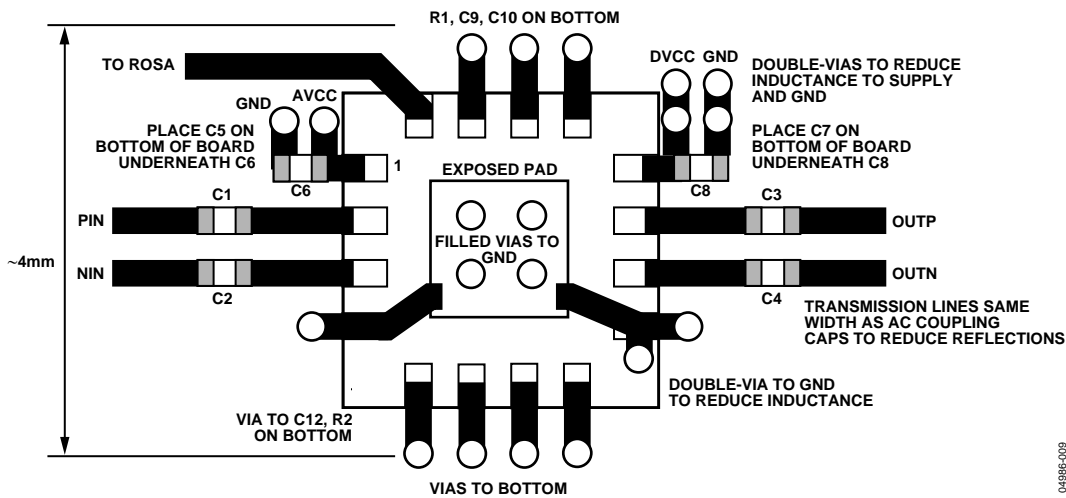
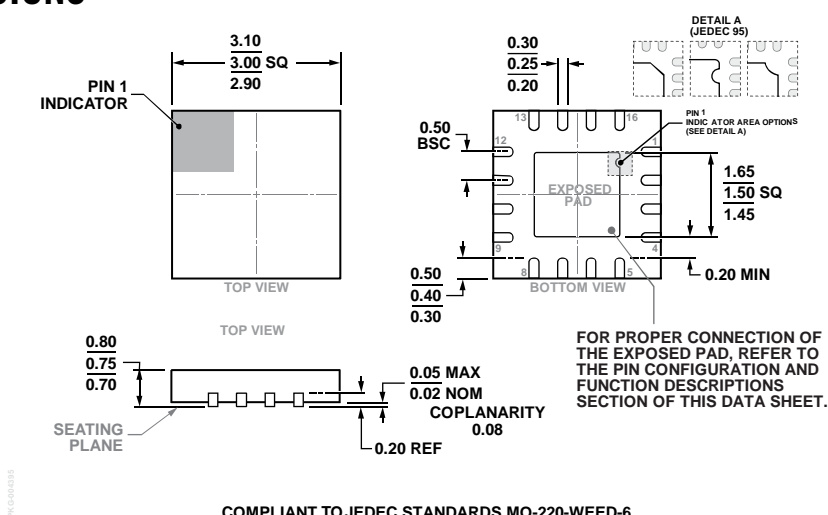


Figure 19. Recommended ADN2892 PCB Layout (Top View)

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 20. 16-Lead Lead Frame Chip Scale Package [LFCSP]  
3 mm × 3 mm Body and 0.75 mm Package Height  
(CP-16-27)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description         | Package Option | Branding |
|--------------------|-------------------|-----------------------------|----------------|----------|
| ADN2892ACPZ-500RL7 | –40°C to +95°C    | 16-Lead LFCSP, 500 pieces   | CP-16-27       | F05      |
| ADN2892ACPZ-RL7    | –40°C to +95°C    | 16-Lead LFCSP, 1,500 pieces | CP-16-27       | F05      |
| EVAL-ADN2892EBZ    |                   | Evaluation Board            |                |          |

<sup>1</sup> Z = RoHS-Compliant Part.

**NOTES**

## NOTES



**NOTES**