1 A, Low Dropout, CMOS Linear Regulator

Data Sheet

ADP1706/ADP1707/ADP1708

FEATURES

- Maximum output current: 1 A
- Input voltage range: 2.5 V to 5.5 V
- Low shutdown current: <1 µA
- Low dropout voltage: 345 mV at 1 A load
- Initial accuracy: ±1%
- Accuracy over line, load, and temperature: ±2.5%
- 16 fixed output voltage options with soft start
  - 0.75 V to 3.3 V (ADP1706)
- 16 fixed output voltage options with tracking
  - 0.75 V to 3.3 V (ADP1707)
- Adjustable output voltage option
  - 0.8 V to 5.0 V (ADP1708)
- Stable with small 4.7 µF ceramic output capacitor
- Excellent load/line transient response
- Current limit and thermal overload protection
- Logic-controlled enable
- Available in an 8-lead, exposed paddle SOIC and a 3 mm × 3 mm, 8-lead exposed paddle LFCSP

APPLICATIONS

- Notebook computers
- Memory components
- Telecommunications equipment
- Network equipment
- DSP/FPGA/microprocessor supplies
- Instrumentation equipment/data acquisition systems

TYPICAL APPLICATION CIRCUITS

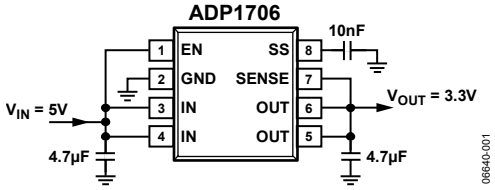

Figure 1. ADP1706 with Fixed Output Voltage, 3.3 V

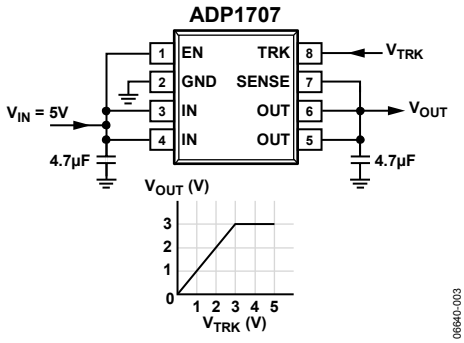

Figure 2. ADP1707 with Output Voltage Tracking

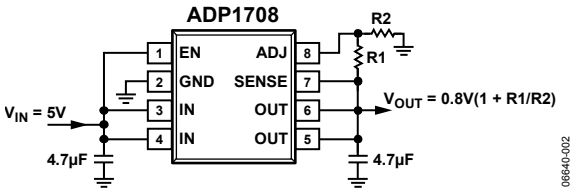

Figure 3. ADP1708 with Adjustable Output Voltage, 0.8 V to 5.0 V

GENERAL DESCRIPTION

The ADP1706/ADP1707/ADP1708 are CMOS, low dropout linear regulators that operate from 2.5 V to 5.5 V and provide up to 1 A of output current. Using an advanced proprietary architecture, they provide high power supply rejection and achieve excellent line and load transient response with a small 4.7 µF ceramic output capacitor.

The ADP1706/ADP1707 are available in 16 fixed output voltage options. The ADP1708 is available in an adjustable version, which allows output voltages that range from 0.8 V to 5.0 V via an external divider. The ADP1706 allows an external soft start capacitor to be connected to program the start-up time; the ADP1707 and ADP1708 contain internal soft start capacitors that give a typical start-up time of 100 µs. The ADP1707 includes a tracking feature that allows the output to follow an external voltage rail or reference.

The ADP1706/ADP1707/ADP1708 are available in an 8-lead, exposed paddle SOIC package and an 8-lead, 3 mm × 3 mm exposed paddle LFCSP, making them not only very compact solutions but also providing excellent thermal performance for applications requiring up to 1 A of output current in a small, low profile footprint.

Rev. A

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REVISION HISTORY

5/2016—Rev. 0 to Rev. A

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Added Table 6 ... 8
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 19

6/2007—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.6 V) or 2.5 V (whichever is greater), I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 4.7 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.5		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 mA		50		µA
		I_{OUT} = 100 mA		310		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			390	µA
		I_{OUT} = 1 A		1.2		mA
		I_{OUT} = 1 A, T_J = −40°C to +125°C			1.55	mA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy (ADP1706 and ADP1707)	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		I_{OUT} = 100 µA to 1 A	−1.5		+1.5	%
		100 µA < I_{OUT} < 1 A, T_J = −40°C to +125°C	−2.5		+2.5	%
Adjustable Output Voltage Accuracy (ADP1708)[1]	V_{OUT}	I_{OUT} = 10 mA	0.792	0.8	0.808	V
		I_{OUT} = 100 µA to 1 A	0.788		0.812	V
		100 µA < I_{OUT} < 1 A, T_J = −40°C to +125°C	0.780		0.820	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.6 V) to 5.5 V, T_J = −40°C to +125°C	−0.1		+0.1	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 1 A, T_J = −40°C to +125°C			0.001	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} ≥ 3.3 V		33		mV
		I_{OUT} = 100 mA, V_{OUT} ≥ 3.3 V, T_J = −40°C to +125°C			55	mV
		I_{OUT} = 1 A, V_{OUT} ≥ 3.3 V		345		mV
		I_{OUT} = 1 A, V_{OUT} ≥ 3.3 V, T_J = −40°C to +125°C			600	mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.3 V		35		mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.3 V, T_J = −40°C to +125°C			60	mV
		I_{OUT} = 1 A, 2.5 V ≤ V_{OUT} < 3.3 V		365		mV
		I_{OUT} = 1 A, 2.5 V ≤ V_{OUT} < 3.3 V, T_J = −40°C to +125°C			630	mV
START-UP TIME[4]	$t_{START-UP}$					
ADP1707 and ADP1708				100		µs
ADP1706		C_{SS} = 10 nF		7.3		ms
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		1.1	1.5	1.8	A
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
SOFT START SOURCE CURRENT (ADP1706)	$SS_{I-SOURCE}$	SS = GND	0.6	1.1	1.6	µA
V_{OUT} to V_{TRK} ACCURACY (ADP1707)	$V_{TRK-ERROR}$	0 V ≤ V_{TRK} ≤ (0.5 × $V_{OUT\ (NOM)}$), $V_{OUT\ (NOM)}$ ≤ 1.8 V, T_J = −40°C to +125°C	−40		+40	mV
		0 V ≤ V_{TRK} ≤ (0.5 × $V_{OUT\ (NOM)}$), $V_{OUT\ (NOM)}$ > 1.8 V, T_J = −40°C to +125°C	−60		+60	mV
EN INPUT						
EN Input Logic High	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.8			V
EN Input Logic Low	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = IN or GND		0.1	1	µA
ADJ INPUT BIAS CURRENT (ADP1708)	ADJ_{I-BIAS}			30	100	nA
SENSE INPUT BIAS CURRENT	SNS_{I-BIAS}			4		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = 0.75 V		125		μV rms
		10 Hz to 100 kHz, V_{OUT} = 3.3 V		450		μV rms
POWER SUPPLY REJECTION RATIO	PSRR	1 kHz, V_{OUT} = 0.75 V		70		dB
		1 kHz, V_{OUT} = 3.3 V		56		dB

[1] Accuracy when OUT is connected directly to ADJ. When OUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of resistors used.
[2] Based on an end-point calculation using 10 mA and 1 A loads. See Figure 11 for typical load regulation performance for loads less than 10 mA.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.
[4] Start-up time is defined as the time between the rising edge of EN to OUT being at 95% of its nominal value.
[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	−0.3 V to +6 V
OUT to GND	−0.3 V to IN
EN to GND	−0.3 V to +6 V
SS/ADJ/TRK to GND	−0.3 V to +6 V
SENSE to GND	−0.3 V to +6 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

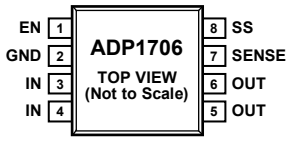
Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC (Exposed Paddle)	58	°C/W
8-Lead 3 mm × 3 mm LFCSP (Exposed Paddle)	66	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

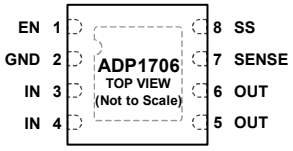
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GND INSIDE THE PACKAGE. IT IS RECOMMENDED TO CONNECT THE EXPOSED PAD TO THE GROUND PLANE ON THE BOARD.

06640-004

Figure 4. 8-Lead SOIC, ADP1706



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06640-007

Figure 5. 8-Lead LFCSP, ADP1706

Table 4. ADP1706 Pin Function Descriptions

Pin No.			
SOIC	**LFCSP**	**Mnemonic**	**Description**
1	1	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
2	2	GND	Ground.
3, 4	3, 4	IN	Regulator Input Supply. Bypass IN to GND with a 4.7 µF or greater capacitor.
5, 6	5, 6	OUT	Regulated Output Voltage. Bypass OUT to GND with a 4.7 µF or greater capacitor.
7	7	SENSE	Sense. Measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load.
8	8	SS	Soft Start. A capacitor connected to this pin determines the soft start time.
0	0	EP	Exposed Pad. The exposed pad enhances thermal performance and is electrically connected to GND inside the package. It is recommended to connect the exposed pad to the ground plane on the board.

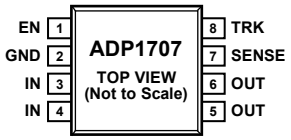

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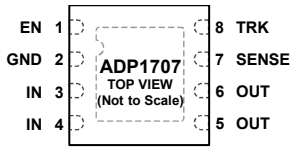
Figure 6. 8-Lead SOIC, ADP1707



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06640-009

Figure 7. 8-Lead LFCSP, ADP1707

Table 5. ADP1707 Pin Function Descriptions

Pin No.			
SOIC	**LFCSP**	**Mnemonic**	**Description**
1	1	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
2	2	GND	Ground.
3, 4	3, 4	IN	Regulator Input Supply. Bypass IN to GND with a 4.7 µF or greater capacitor.
5, 6	5, 6	OUT	Regulated Output Voltage. Bypass OUT to GND with a 4.7 µF or greater capacitor.
7	7	SENSE	Sense. Measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load.
8	8	TRK	Track. The output follows the voltage applied at the TRK pin. See the Theory of Operation section for a more detailed description.
0	0	EP	Exposed Pad. The exposed pad enhances thermal performance and is electrically connected to GND inside the package. It is recommended to connect the exposed pad to the ground plane on the board.

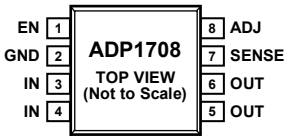

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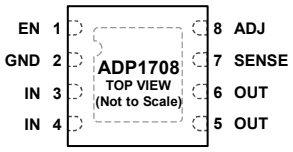
Figure 8. 8-Lead SOIC, ADP1708



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06640-008

Figure 9. 8-Lead LFCSP, ADP1708

Table 6. ADP1708 Pin Function Descriptions

Pin No.			
SOIC	**LFCSP**	**Mnemonic**	**Description**
1	1	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
2	2	GND	Ground.
3, 4	3, 4	IN	Regulator Input Supply. Bypass IN to GND with a 4.7 µF or greater capacitor.
5, 6	5, 6	OUT	Regulated Output Voltage. Bypass OUT to GND with a 4.7 µF or greater capacitor.
7	7	SENSE	Sense. Measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load.
8	8	ADJ	Adjust. A resistor divider from OUT to ADJ sets the output voltage.
0	0	EP	Exposed Pad. The exposed pad enhances thermal performance and is electrically connected to GND inside the package. It is recommended to connect the exposed pad to the ground plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8 V, I_{OUT} = 100 mA, C_{IN} = 4.7 µF, C_{OUT} = 4.7 µF, T_A = 25°C, unless otherwise noted.

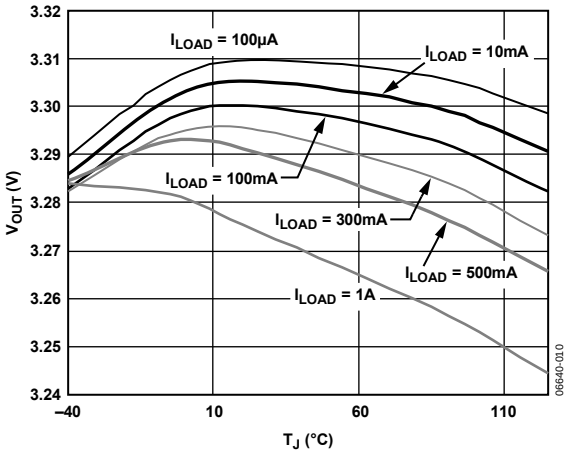


Figure 10. Output Voltage vs. Junction Temperature

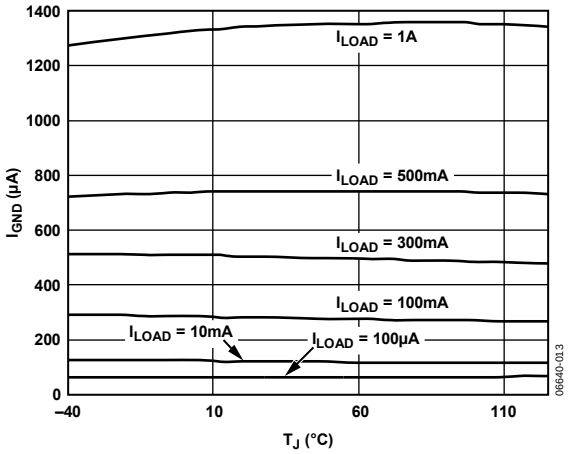


Figure 13. Ground Current vs. Junction Temperature

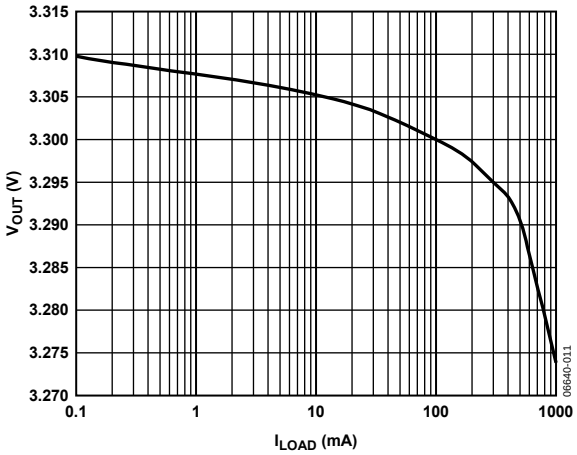


Figure 11. Output Voltage vs. Load Current

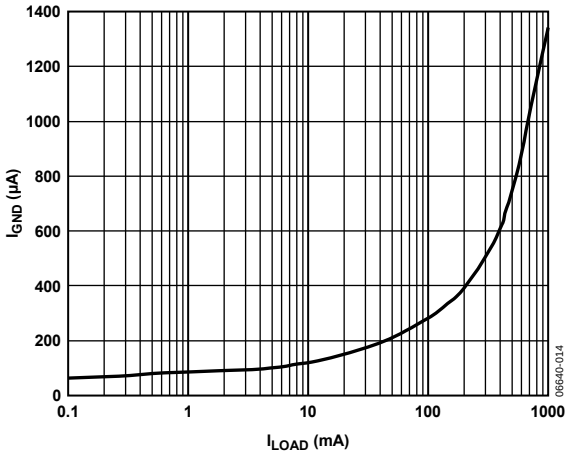


Figure 14. Ground Current vs. Load Current

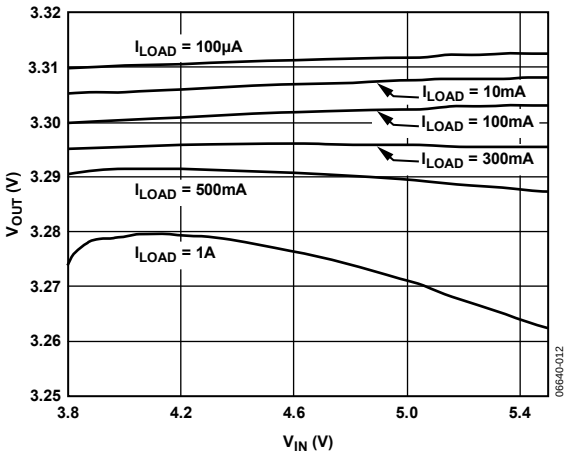


Figure 12. Output Voltage vs. Input Voltage

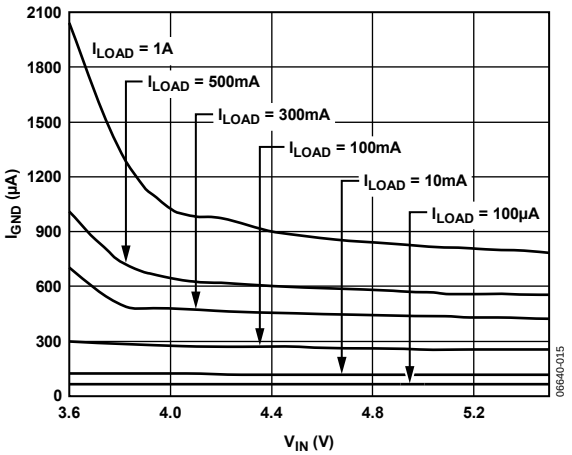


Figure 15. Ground Current vs. Input Voltage

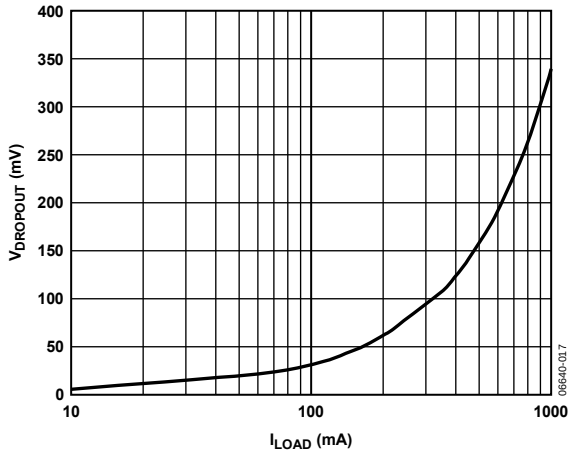


Figure 16. Dropout Voltage vs. Load Current

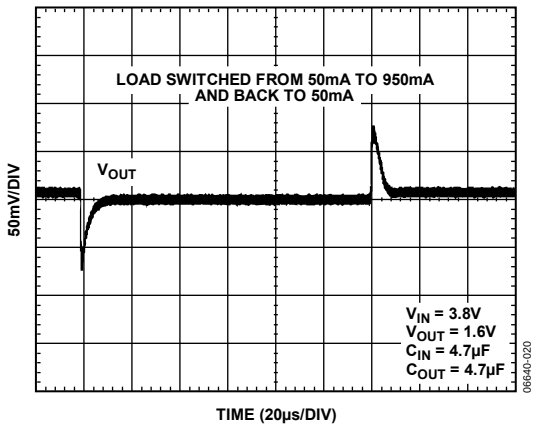


Figure 19. Load Transient Response, C_{IN} = 4.7 µF, C_{OUT} = 4.7 µF

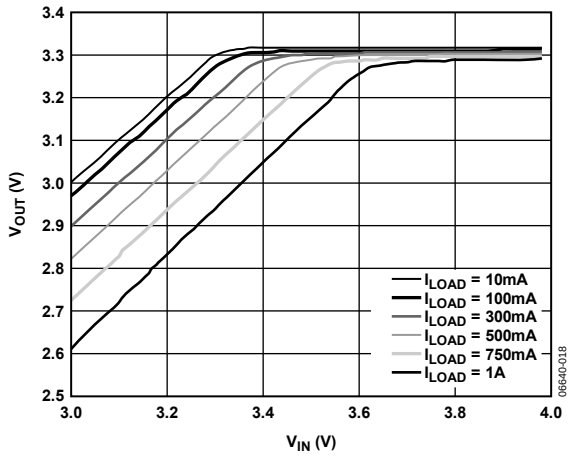


Figure 17. Output Voltage vs. Input Voltage (in Dropout)

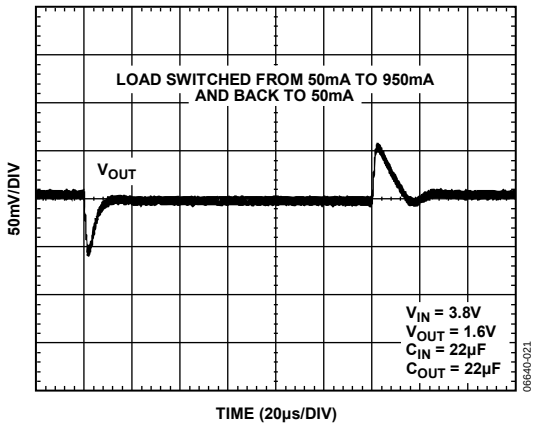


Figure 20. Load Transient Response, C_{IN} = 22 µF, C_{OUT} = 22 µF

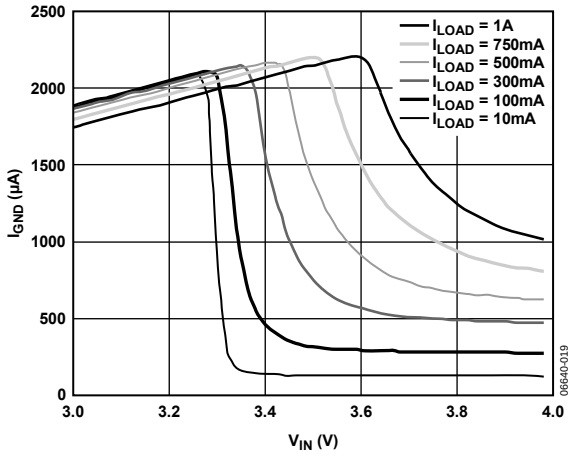


Figure 18. Ground Current vs. Input Voltage (in Dropout)

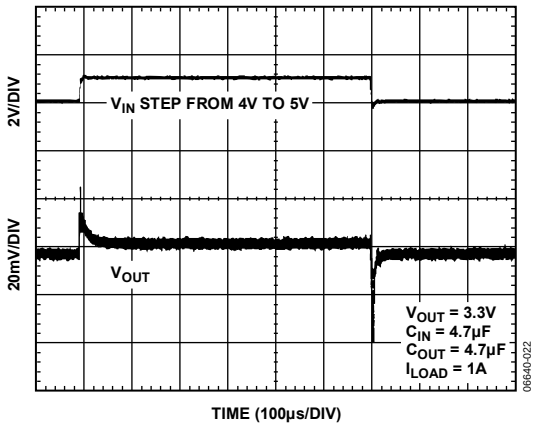


Figure 21. Line Transient Response

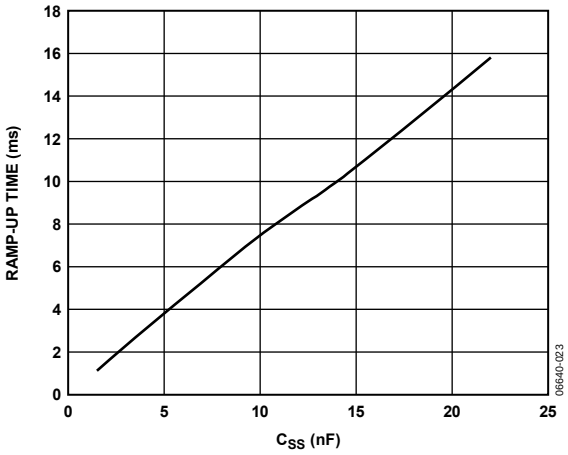


Figure 22. Output Voltage Ramp-Up Time vs. Soft Start Capacitor Value

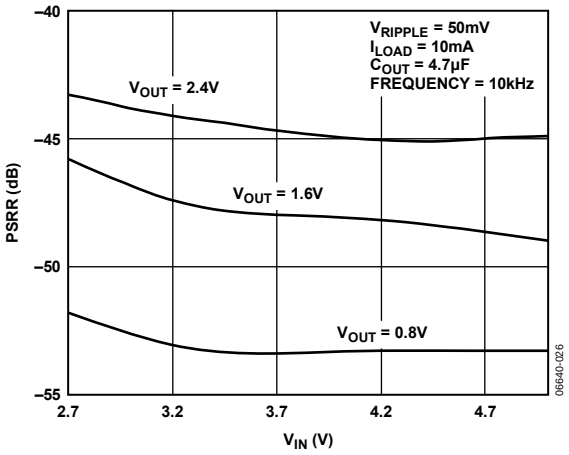


Figure 25. ADP1708 Power Supply Rejection Ratio vs. Input Voltage

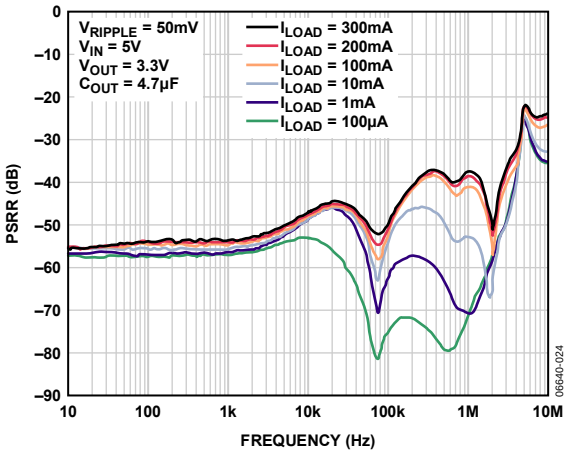


Figure 23. ADP1706 Power Supply Rejection Ratio vs. Frequency

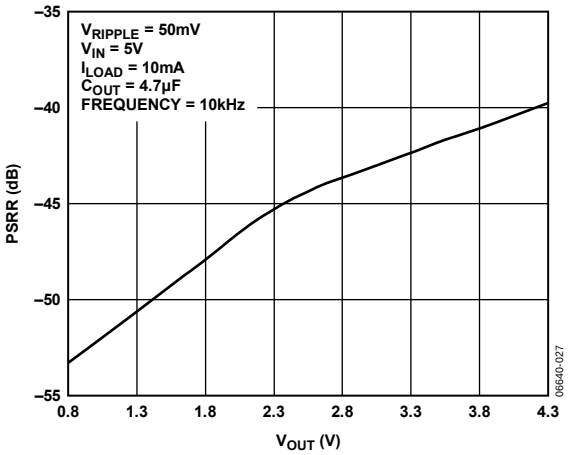


Figure 26. ADP1708 Power Supply Rejection Ratio vs. Output Voltage

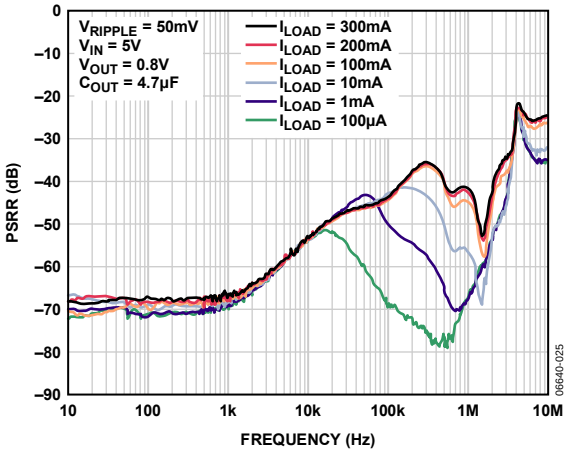


Figure 24. ADP1708 Power Supply Rejection Ratio vs. Frequency

THEORY OF OPERATION

The ADP1706/ADP1707/ADP1708 are low dropout linear regulators that use an advanced, proprietary architecture to provide high power supply rejection ratio (PSRR) and excellent line and load transient response with a small 4.7 µF ceramic output capacitor. All devices operate from a 2.5 V to 5.5 V input rail and provide up to 1 A of output current. Supply current in shutdown mode is typically 100 nA.

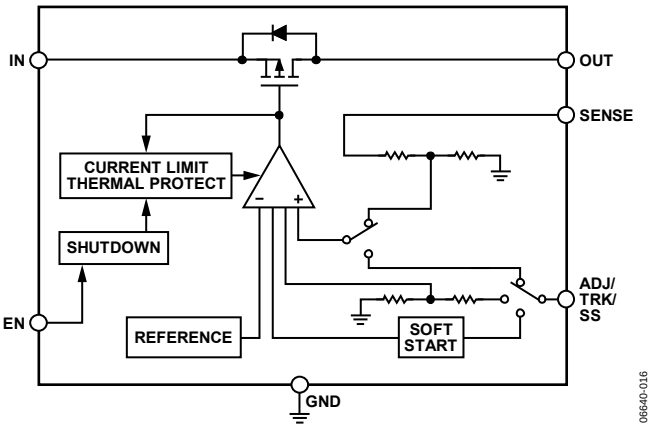


Figure 27. Internal Block Diagram

Internally, the ADP1706/ADP1707/ADP1708 consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP1706/ADP1707 are available in 16 fixed output voltage options between 0.75 V and 3.3 V. The ADP1706 allows for connection of an external soft start capacitor, which controls the output voltage ramp during startup. The ADP1707 features a TRK pin that allows the output voltage to follow the voltage at this pin. The ADP1708 is available in an adjustable version with an output voltage that can be set to between 0.8 V and 5.0 V by an external voltage divider. All devices are controlled by an enable pin (EN).

SOFT START FUNCTION (ADP1706)

For applications that require a controlled startup, the ADP1706 provides a programmable soft start function. The programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. To implement a soft start, connect a small ceramic capacitor from SS to GND. Upon startup, a 1.2 µA current source charges this capacitor. The ADP1706 start-up output voltage is limited by the voltage at SS, providing a smooth ramp-up to the nominal output voltage. The soft start time is calculated by

$$T_{SS} = V_{REF} \times (C_{SS}/I_{SS}) \quad (1)$$

where:
T_{SS} is the soft start period.
V_{REF} is the 0.8 V reference voltage.
C_{SS} is the soft start capacitance from SS to GND.
I_{SS} is the current sourced from SS (1.2 µA).

When the ADP1706 is disabled (using EN), the soft start capacitor is discharged to GND through an internal 100 Ω resistor.

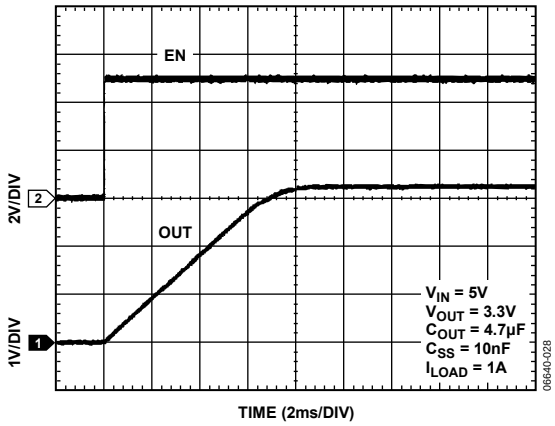


Figure 28. OUT Ramp-Up with External Soft Start Capacitor

The ADP1707 and ADP1708 have no pins for soft start; therefore, the function is switched to an internal soft start capacitor, which sets the soft start ramp-up period to approximately 48 µs. Note that the ramp-up period is the time it takes OUT to go from 0% to 90% of the nominal value and is different from the start-up time in Table 1, which is the time between the rising edge of EN to OUT being at 90% of the nominal value. For the worst-case output voltage of 5 V, using the suggested 4.7 µF output capacitor, the resulting input inrush current is approximately 490 mA, which is less than the maximum 1 A load current.

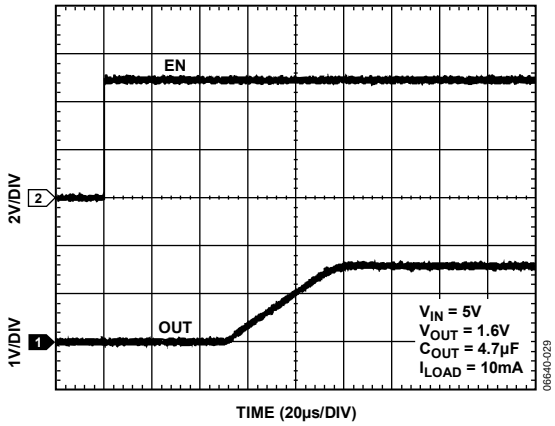


Figure 29. OUT Ramp-Up with Internal Soft Start

ADJUSTABLE OUTPUT VOLTAGE (ADP1708)

The ADP1708 can have its output voltage set over a 0.8 V to 5.0 V range. The output voltage is set by connecting a resistive voltage divider from OUT to ADJ. The output voltage is calculated by

$$V_{OUT} = 0.8\ V\ (1 + R1/R2) \quad (2)$$

where:
R1 is the resistor from OUT to ADJ.
R2 is the resistor from ADJ to GND.

The maximum bias current into ADJ is 100 nA, so for less than 0.5% error due to the bias current, use values less than 60 kΩ for R2.

TRACK MODE (ADP1707)

The ADP1707 includes a tracking mode feature. As shown in Figure 30, if the voltage applied at the TRK pin is less than the nominal output voltage, OUT is equal to the voltage at TRK. Otherwise, OUT regulates to its nominal output value.

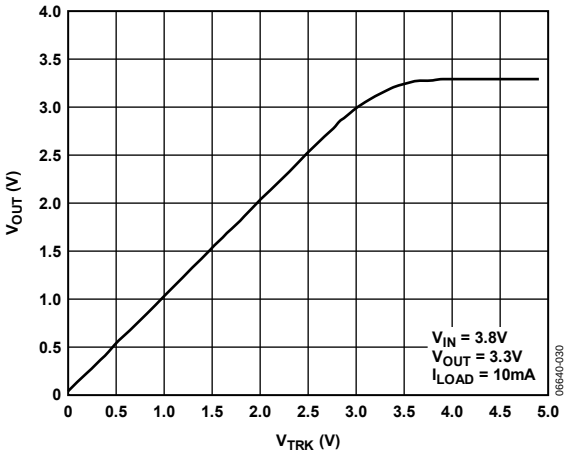


Figure 30. ADP1707 Output Voltage vs. Tracking Voltage

For example, consider an ADP1707 with a nominal output voltage of 3.3 V. If the voltage applied to its TRK pin is greater than 3.3 V, OUT maintains a nominal output voltage of 3.3 V. If the voltage applied to TRK is reduced below 3.3 V, OUT tracks this voltage. OUT can track the TRK pin voltage from the nominal value all the way down to 0 V. A voltage divider is present from TRK to the error amplifier input with a divider ratio equal to the divider from OUT to the error amplifier, which sets the output voltage equal to the tracking voltage. Both divider ratios are set by postpackage trim, depending on the desired output voltage.

ENABLE FEATURE

The ADP1706/ADP1707/ADP1708 use the EN pin to enable and disable the OUT pin under normal operating conditions. As shown in Figure 31, when a rising voltage on EN crosses the active threshold, OUT turns on. When a falling voltage on EN crosses the inactive threshold, OUT turns off.

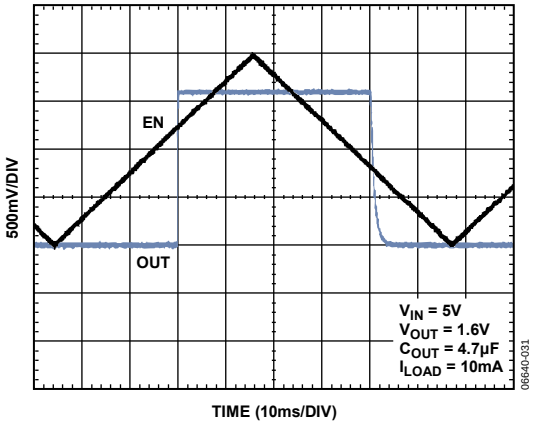


Figure 31. ADP1706 Typical EN Pin Operation

As shown in Figure 31, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the IN voltage. Therefore, these thresholds vary when changing the input voltage. Figure 32 shows typical EN active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

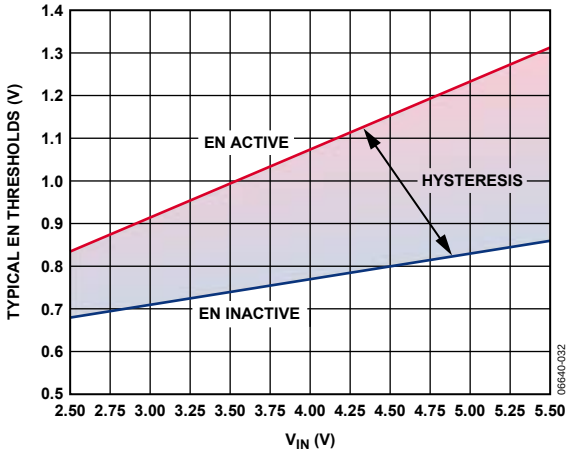


Figure 32. Typical EN Pin Thresholds vs. Input Voltage

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1706/ADP1707/ADP1708 are designed for operation with small, space-saving ceramic capacitors, but they function with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 4.7 µF capacitance with an ESR of 500 mΩ or less is recommended to ensure stability of the ADP1706/ADP1707/ADP1708. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1706/ADP1707/ADP1708 to large changes in load current. Figure 33 and Figure 34 show the transient responses for output capacitance values of 4.7 µF and 22 µF, respectively.

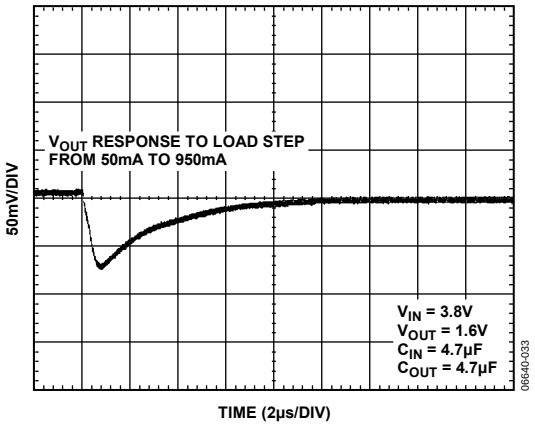


Figure 33. Output Transient Response, C_{OUT} = 4.7 µF

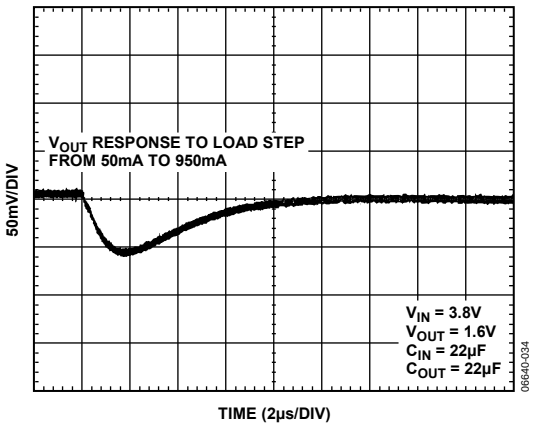


Figure 34. Output Transient Response, C_{OUT} = 22 µF

Input Bypass Capacitor

Connecting a 4.7 µF capacitor from the IN pin to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces, or high source impedance, is encountered. If greater than 4.7 µF of output capacitance is required, it is recommended that the input capacitor be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP1706/ADP1707/ADP1708, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

VOLTAGE TRACKING APPLICATIONS

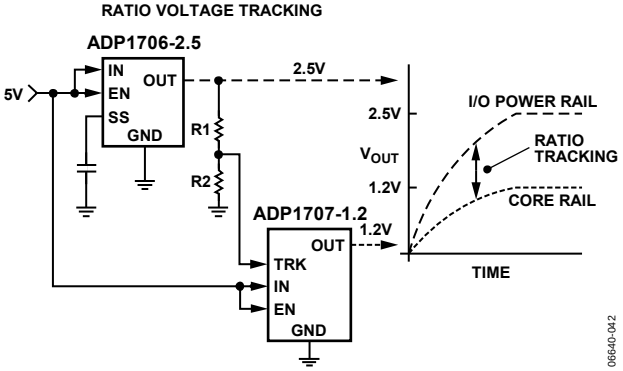


Figure 35. Voltage Tracking Feature Using the ADP1707

Figure 35 shows an application where the ADP1707 tracking feature is used. An ADP1706 powers the input/output of a microprocessor and an ADP1707 powers the core. At startup, the output of the ADP1706 ramps to 2.5 V, which is divided down via a voltage divider (R1 and R2) to a lower voltage at the TRK pin of the ADP1707. The output of the ADP1707 thus follows the TRK pin and ramps up steadily to 1.2 V. This implementation ensures that the core of the processor powers up after the input/output.

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1706/ADP1707/ADP1708 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP1706/ADP1707/ADP1708 are designed to reach current limit when the output load reaches 1.5 A (typical). When the output load exceeds 1.5 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C (typical), the output is turned on again and output current is restored to its nominal value.

Consider the case where a hard short from OUT to ground occurs. At first, the ADP1706/ADP1707/ADP1708 reach current limit so that only 1.5 A is conducted into the short. If self-heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 1.5 A into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 1.5 A and 0 A that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation should be externally limited so junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1706/ADP1707/ADP1708 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered on the PCB. Table 7 shows typical θ_{JA} values of the 8-lead SOIC and 8-lead LFCSP for various PCB copper sizes.

Table 7. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W), SOIC	θ_{JA} (°C/W), LFCSP
0[1]	57.6	65.9
50	53.1	62.3
100	52.3	61.2
300	51.3	59.7
500	51.3	59.4

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP1706/ADP1707/ADP1708 can be calculated by

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{OUT}) \times I_{LOAD}) + (V_{IN} \times I_{GND}) \quad (4)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are the input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + (((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \theta_{JA}) \quad (5)$$

As shown in Equation 5, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure the junction temperature does not rise above 125°C. Figure 36 to Figure 41 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

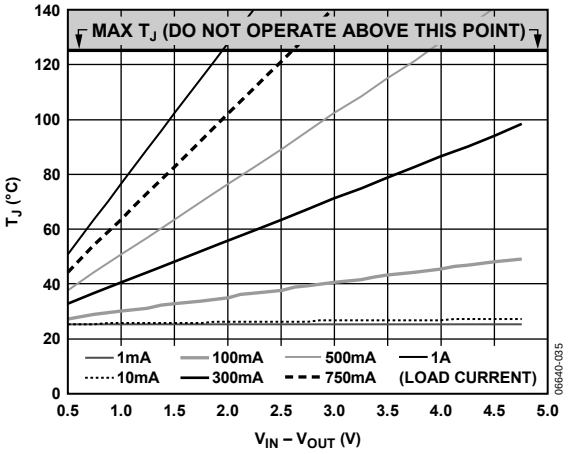


Figure 36. 500 mm² of PCB Copper, T_A = 25°C, SOIC

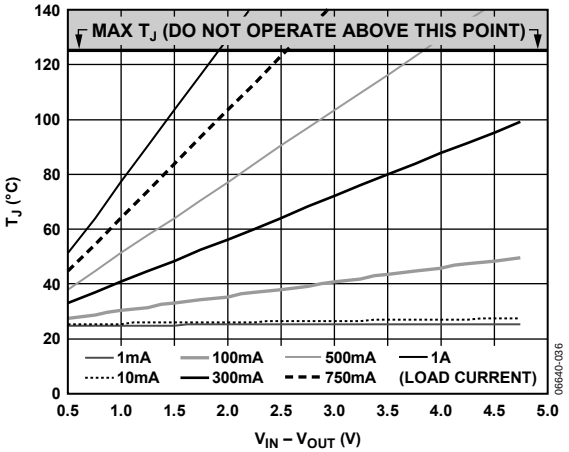


Figure 37. 100 mm² of PCB Copper, T_A = 25°C, SOIC

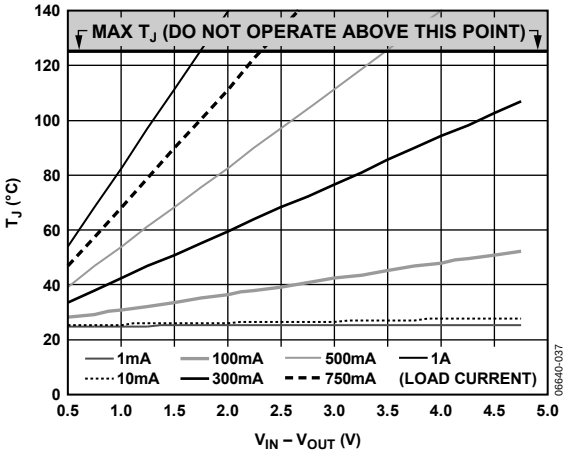


Figure 38. 0 mm² of PCB Copper, T_A = 25°C, SOIC

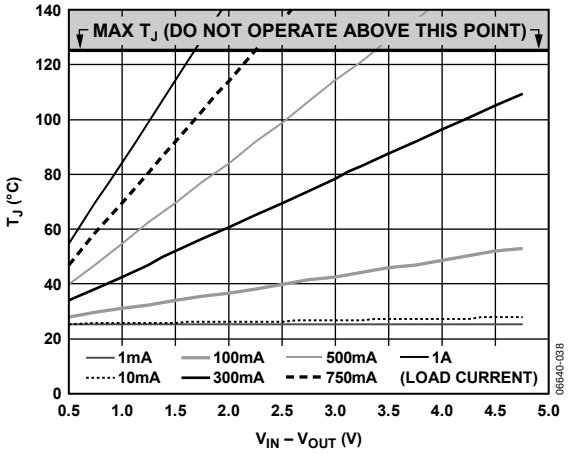


Figure 39. 500 mm² of PCB Copper, T_A = 25°C, LFCSP

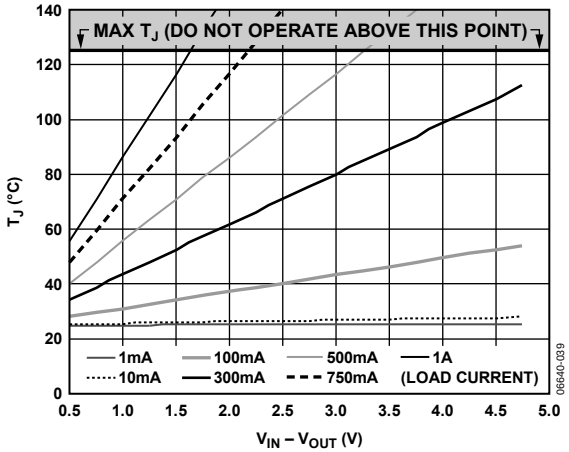


Figure 40. 100 mm² of PCB Copper, T_A = 25°C, LFCSP

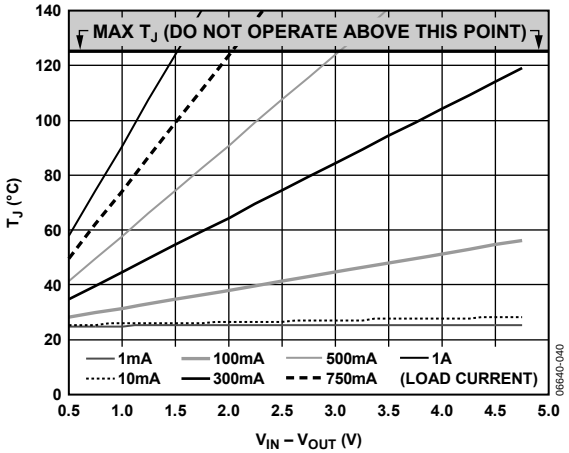


Figure 41. 0 mm² of PCB Copper, T_A = 25°C, LFCSP

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP1706/ADP1707/ADP1708. However, as can be seen from Table 7, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

The ADP1706/ADP1707/ADP1708 feature an exposed pad on the bottom of both the SOIC and LFCSP packages to improve thermal performance. Because the exposed pad is electrically connected to GND inside the package, it is recommended that it also be connected to the ground plane on the PCB with a sufficient amount of copper.

Here are a few general tips when designing PCBs:

- Place the input capacitor as close as possible to the IN and GND pins.
- Place the output capacitor as close as possible to the OUT and GND pins.
- For the ADP1706, place the soft start capacitor as close as possible to the SS pin.
- Connect the load as close as possible to the OUT and SENSE pins.

Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

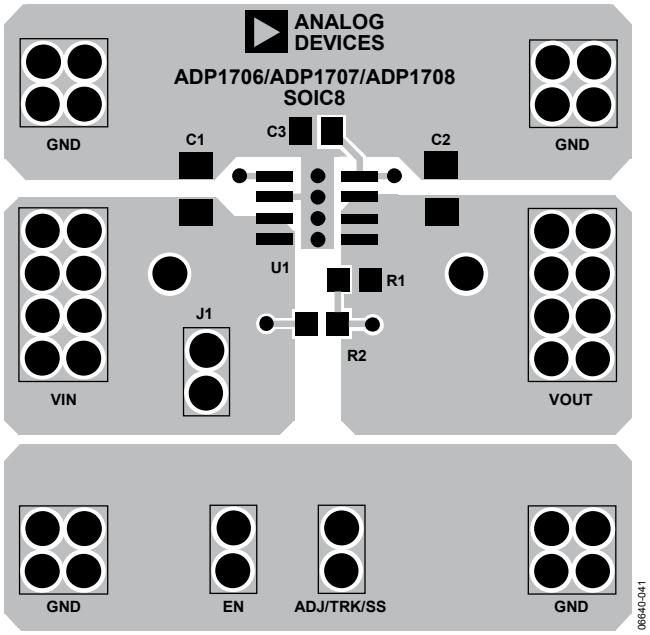
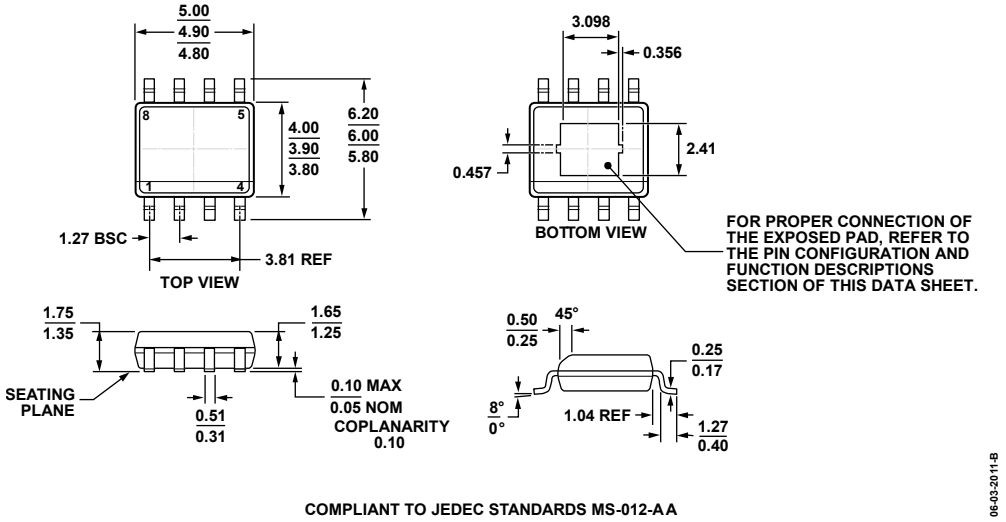


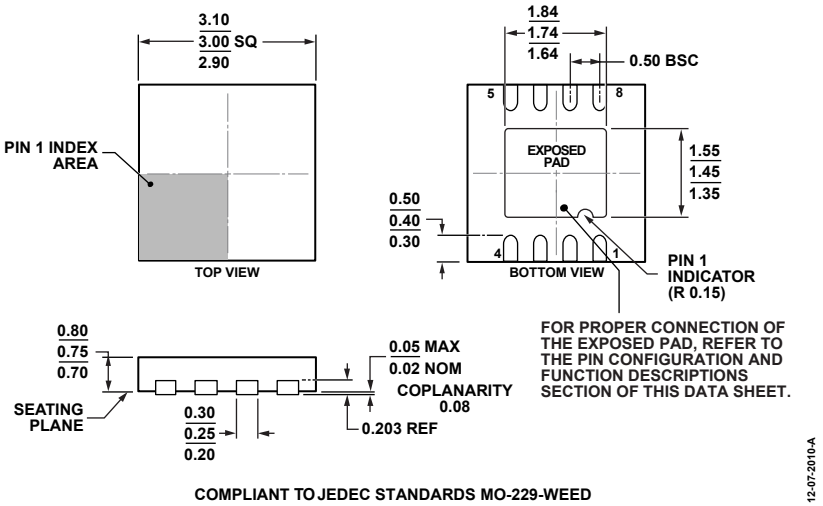
Figure 42. Example PCB Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

Figure 43. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 44. 8-Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP1706ARDZ-0.75R7	–40°C to +125°C	0.75	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-0.8-R7	–40°C to +125°C	0.8	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-0.9-R7	–40°C to +125°C	0.9	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.0-R7	–40°C to +125°C	1.0	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.1-R7	–40°C to +125°C	1.1	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.15R7	–40°C to +125°C	1.15	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.2-R7	–40°C to +125°C	1.2	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.3-R7	–40°C to +125°C	1.3	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.5-R7	–40°C to +125°C	1.5	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-1.8-R7	–40°C to +125°C	1.8	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-2.5-R7	–40°C to +125°C	2.5	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-3.0-R7	–40°C to +125°C	3.0	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ARDZ-3.3-R7	–40°C to +125°C	3.3	8-Lead SOIC_N_EP	RD-8-2	
ADP1706ACPZ-1.0-R7	–40°C to +125°C	1.0	8-Lead LFCSP	CP-8-13	L65
ADP1706ACPZ-1.05R7	–40°C to +125°C	1.05	8-Lead LFCSP	CP-8-13	L67
ADP1706ACPZ-1.1-R7	–40°C to +125°C	1.1	8-Lead LFCSP	CP-8-13	L66
ADP1706ACPZ-1.2-R7	–40°C to +125°C	1.2	8-Lead LFCSP	CP-8-13	L6A
ADP1706ACPZ-1.3-R7	–40°C to +125°C	1.3	8-Lead LFCSP	CP-8-13	L6C
ADP1706ACPZ-1.5-R7	–40°C to +125°C	1.5	8-Lead LFCSP	CP-8-13	L6D
ADP1706ACPZ-1.8-R7	–40°C to +125°C	1.8	8-Lead LFCSP	CP-8-13	L6H
ADP1706ACPZ-2.5-R7	–40°C to +125°C	2.5	8-Lead LFCSP	CP-8-13	L6E
ADP1706ACPZ-3.3-R7	–40°C to +125°C	3.3	8-Lead LFCSP	CP-8-13	L6G
ADP1707ARDZ-1.0-R7	–40°C to +125°C	1.0	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-1.1-R7	–40°C to +125°C	1.1	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-1.2-R7	–40°C to +125°C	1.2	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-1.3-R7	–40°C to +125°C	1.3	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-1.5-R7	–40°C to +125°C	1.5	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-1.8-R7	–40°C to +125°C	1.8	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-2.5-R7	–40°C to +125°C	2.5	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-3.0-R7	–40°C to +125°C	3.0	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ARDZ-3.3-R7	–40°C to +125°C	3.3	8-Lead SOIC_N_EP	RD-8-2	
ADP1707ACPZ-1.3-R7	–40°C to +125°C	1.3	8-Lead LFCSP	CP-8-13	L6Z
ADP1707ACPZ-1.8-R7	–40°C to +125°C	1.8	8-Lead LFCSP	CP-8-13	L71
ADP1707ACPZ-2.5-R7	–40°C to +125°C	2.5	8-Lead LFCSP	CP-8-13	L72
ADP1707ACPZ-3.0-R7	–40°C to +125°C	3.0	8-Lead LFCSP	CP-8-13	L73
ADP1707ACPZ-3.3-R7	–40°C to +125°C	3.3	8-Lead LFCSP	CP-8-13	L74
ADP1708ARDZ-R7	–40°C to +125°C	0.8 to 5.0	8-Lead SOIC_N_EP	RD-8-2	
ADP1708ACPZ-R7	–40°C to +125°C	0.8 to 5.0	8-Lead LFCSP	CP-8-13	L7P
ADP1706-3.3-EVALZ		3.3	Evaluation Board		
ADP1707-3.3-EVALZ		3.3	Evaluation Board		
ADP1708-EVALZ		Adjustable, but set to 1.6 V	Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES