Dual, 200 mA, High Performance RF LDO with Load Switch

ADP5030

FEATURES

- Input voltage range: 2.5 V to 5.5 V
- Dual, 200 mA low dropout voltage regulators
- Tiny, 16-ball, 1.6 mm × 1.6 mm WLCSP
- Initial accuracy: ±0.7%
- Stable with 1 µF ceramic output capacitors
- Overcurrent and thermal protection
- High PSRR
  - 76 dB up to 1 kHz
  - 70 dB at 10 kHz
  - 60 dB at 100 kHz
  - 40 dB at 1 MHz
- Low output noise
  - 27 µV rms typical output noise at V_{OUTx} = 1.2 V
  - 50 µV rms typical output noise at V_{OUTx} = 2.8 V
- Excellent transient response
- Low dropout voltage: 175 mV at 200 mA load
- 60 µA typical ground current at no load, both LDOs enabled
- Guaranteed 200 mA output current per regulator
- Load switch with low RDS_{ON} of 100 mΩ at 1.8 V
- High-to-low voltage and low-to-high voltage level shifting logic
- −40°C to +125°C junction temperature

APPLICATIONS

- RF subsystems
- GPS devices

GENERAL DESCRIPTION

The ADP5030 combines two high performance, low dropout (LDO) voltage regulators, a low RDS_{ON} load switch, and level shifting logic in a tiny, 16-ball, 1.6 mm × 1.6 mm WLCSP to meet demanding performance and board space requirements.

The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5030 LDOs extend the battery life of portable devices. The ADP5030 LDOs maintain power supply rejection greater than 60 dB for frequencies as high as 100 kHz while operating with a low headroom voltage.

The ADP5030 can be configured in two different activation modes for LDO2 and the load switch; these modes are selected by a dedicated pin (MSEL).

FUNCTIONAL BLOCK DIAGRAM

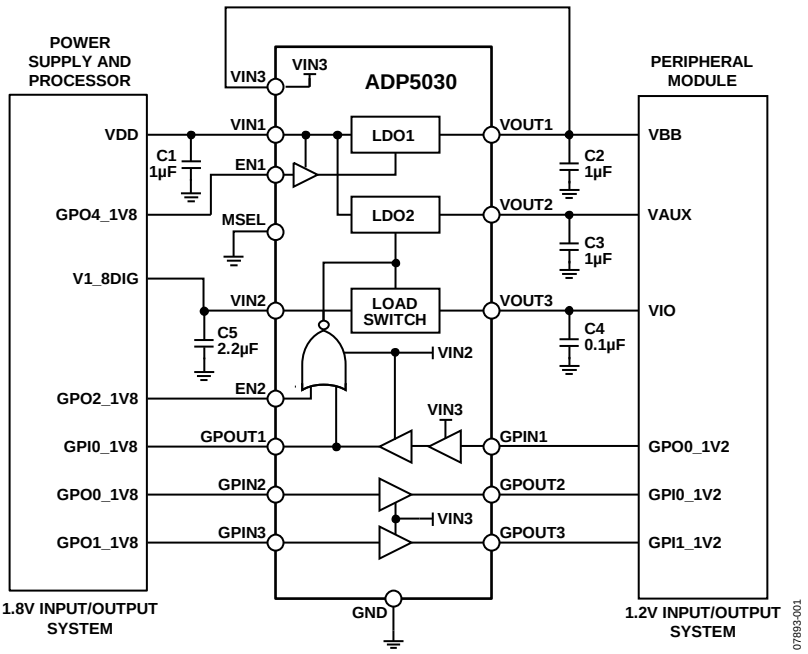

Figure 1.

Rev. B

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ADP5030* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-1072: How to Successfully Apply Low Dropout Regulators

Data Sheet

- ADP5030: Dual, 200 mA, High Performance RF LDO with Load Switch Data Sheet

TOOLS AND SIMULATIONS

- ADI Linear Regulator Design Tool and Parametric Search
- ADIsimPower™ Voltage Regulator Design Tool

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Integrated Power Solutions for Altera FPGAs
- Integrated, High Power Solutions for Xilinx FPGAs

DESIGN RESOURCES

- ADP5030 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5030 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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9/09—Rev. 0 to Rev. A

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Changes to Table 3 and Table 4 ... 5
Changes to Input and Output Capacitor Properties Section ... 15

6/09—Revision 0: Initial Version

SPECIFICATIONS

V_{IN1} = (V_{OUT2} + 0.5 V) or 2.5 V (whichever is greater), $V_{IN1} \geq V_{IN2} \geq V_{IN3}$, $I_{OUT1} = I_{OUT2}$ = 10 mA, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE[1]	V_{IN1}	T_J = −40°C to +125°C	2.5		5.5	V
	V_{IN2}	T_J = −40°C to +125°C	1.1	1.8	3.6	V
	V_{IN3}	T_J = −40°C to +125°C	1.1		V_{IN2}	V
OPERATING SUPPLY CURRENT WITH BOTH REGULATORS ON	I_{GND}			60		µA
		I_{OUT1}, I_{OUT2} = 0 µA		60		µA
		I_{OUT1}, I_{OUT2} = 0 µA, T_J = −40°C to +125°C			120	µA
		I_{OUT1}, I_{OUT2} = 10 mA		70		µA
		I_{OUT1}, I_{OUT2} = 10 mA, T_J = −40°C to +125°C			140	µA
		I_{OUT1}, I_{OUT2} = 200 mA		120		µA
		I_{OUT1}, I_{OUT2} = 200 mA, T_J = −40°C to +125°C			220	µA
SHUTDOWN CURRENT		EN1 = GND, GPIN2 = GPIN1 = V_{IH}				
From VIN1 Pin	I_{IN1-SD}	V_{IN1} = 5.5 V, T_J = −40°C to +125°C		0.4	2.0	µA
From VIN2 Pin	I_{IN2-SD}	V_{IN2} = 1.8 V, T_J = −40°C to +85°C		0.4	2.0	µA
From VIN3 Pin	I_{IN3-SD}	V_{IN3} = 1.2 V, T_J = −40°C to +125°C		0.2	1.5	µA
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT1}, V_{OUT2}		−0.7		+0.7	%
		100 µA < I_{OUT1}, I_{OUT2} < 200 mA, V_{IN1} = (V_{OUT2} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−2.0		+1	%
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN1} = (V_{OUT2} + 0.5 V) to 5.5 V		0.01		%/V
		V_{IN1} = (V_{OUT2} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.03		+0.03	%/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT1}, I_{OUT2} = 1 mA to 200 mA		0.001		%/mA
		I_{OUT1}, I_{OUT2} = 1 mA to 200 mA, T_J = −40°C to +125°C			0.003	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	V_{OUT2} = 2.8 V				
		I_{OUT1}, I_{OUT2} = 10 mA		9		mV
		I_{OUT1}, I_{OUT2} = 10 mA, T_J = −40°C to +125°C			13	mV
		I_{OUT1}, I_{OUT2} = 200 mA		175		mV
		I_{OUT1}, I_{OUT2} = 200 mA, T_J = −40°C to +125°C			250	mV
START-UP TIME[3]	$t_{START-UP}$	V_{OUT2} = 2.8 V		240		µs
		V_{OUT1} = 1.2 V		120		µs
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT1}, I_{LIMIT2}		240	300	440	mA
LOAD SWITCH OUTPUT CURRENT	I_{OUT3}				500	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		155		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN1, MSEL INPUTS						
EN1, MSEL Input Logic High	V_{IH1}	2.5 V ≤ V_{IN1} ≤ 5.5 V	1.2			V
EN1, MSEL Input Logic Low	V_{IL1}	2.5 V ≤ V_{IN1} ≤ 5.5 V			0.4	V
EN1, MSEL Input Leakage Current	$I_{LEAKAGE1}$	EN1 = MSEL = V_{IN1} or GND		0.2		µA
		EN1 = MSEL = V_{IN1} or GND, T_J = −40°C to +125°C			1	µA
EN2 INPUT						
EN2 Input Logic High	V_{IH2}	1.2 V ≤ V_{IN2} ≤ 3.6 V	0.65 × V_{IN2}			V
EN2 Input Logic Low	V_{IL2}	1.2 V ≤ V_{IN2} ≤ 3.6 V			0.35 × V_{IN2}	V
EN2 Input Leakage Current	$I_{LEAKAGE2}$	EN2 = V_{IN2} or GND		0.2		µA
		EN2 = V_{IN2} or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT (V_{IN1})	UVLO					
Input Voltage Rising	$UVLO_{RISE}$				2.45	V
Input Voltage Falling	$UVLO_{FALL}$		2.2			V
Hysteresis	$UVLO_{HYS}$			100		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN1} = 5 V, V_{OUTx} = 2.8 V		50		µV rms
		10 Hz to 100 kHz, V_{IN1} = 3.6 V, V_{OUTx} = 1.2 V		27		µV rms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	V_{IN1} = 2.5 V, V_{OUT1} = 1.2 V, I_{OUT} = 100 mA				
		100 Hz		76		dB
		1 kHz		76		dB
		10 kHz		70		dB
		100 kHz		60		dB
		1 MHz		40		dB
		V_{IN1} = 3.8 V, V_{OUT2} = 2.8 V, I_{OUT} = 100 mA				
		100 Hz		68		dB
		1 kHz		68		dB
		10 kHz		68		dB
		100 kHz		60		dB
		1 MHz		40		dB
LOAD SWITCH						
VIN2 to VOUT3 Resistance	RDS_{ON}	I_{LOAD} = 200 mA, EN2 = V_{IH2}, MSEL = GPIN1 = GND				
		V_{IN2} = 3.6 V		70		mΩ
		V_{IN2} = 2.5 V		80		mΩ
		V_{IN2} = 1.8 V		100	130	mΩ
		V_{IN2} = 1.8 V, T_J = −40°C to +125°C			160	mΩ
Turn-On Times		V_{IN2} = 1.8 V, I_{LOAD} = 100 mA, C_{LOAD} = 0.1 µF, EN2 = V_{IH2}, MSEL = GPIN1 = GND				
Turn-On Delay Time	t_{ON_DLY}	EN2 rising to 10% of turn-on value		5	15	µs
Turn-On Rise Time	t_{ON_RISE}	V_{OUT3} rising from 10% to 90% of turn-on value		8	12	µs
LEVEL SHIFTER		V_{IN1} = 3.6 V, 1.2 V ≤ V_{IN3} ≤ 3.6 V, T_J = −40°C to +125°C				
GPIN1 Input Logic High	V_{IH}		0.65 × V_{IN3}			V
GPIN1 Input Logic Low	V_{IL}				0.35 × V_{IN3}	V
GPOUT1 Output Logic High	V_{OH}	I_{OH} = 2 mA, V_{IN2} = 1.8 V	1.6			V
GPOUT1 Output Logic Low	V_{OL}	I_{OL} = 1 mA, V_{IN2} = 1.8 V			0.16	V
GPOUT1 Output Logic Low	V_{OL}	I_{OL} = 2 mA, V_{IN2} = 1.8 V			0.31	V
GPIN1 to GPOUT1 Propagation Delay	t_{PHL}, t_{PLH}	C_{LOAD} = 30 pF, R_{LOAD} = 1 MΩ, V_{IN2} = 1.8 V			20	ns
GPIN2, GPIN3 Input Logic High	V_{IH}		0.65 × V_{IN3}			V
GPIN2, GPIN3 Input Logic Low	V_{IL}				0.35 × V_{IN3}	V
GPOUT2, GPOUT3 Output Logic High	V_{OH}	I_{OH} = 2 mA, V_{IN3} = 1.2 V	0.95			V
GPOUT2, GPOUT3 Output Logic Low	V_{OL}	I_{OL} = 1 mA, V_{IN3} = 1.2 V			0.17	V
		I_{OL} = 2 mA, V_{IN3} = 1.2 V			0.33	V
GPIN2, GPIN3 to GPOUT2, GPOUT3 Propagation Delay	t_{PHL}, t_{PLH}	C_{LOAD} = 30 pF, R_{LOAD} = 1 MΩ			20	ns
GPIN1, GPIN2, GPIN3 Input Leakage Current	$I_{LEAKAGE-GPIN}$	GPIN1, GPIN2, GPIN3 = V_{IN3} or GND, T_A = 25°C		0.1		µA
		GPIN1, GPIN2, GPIN3 = V_{IN3} or GND			1	µA

[1] V_{IN2} minimum supply voltage is 1.1 V or V_{IN3}, whichever is greater. V_{IN2} maximum supply voltage is 3.6 V or V_{IN1}, whichever is smaller.
[2] Dropout voltage is the input-to-output voltage differential when the input voltage is set to the nominal output voltage. It applies only to output voltages above 2.5 V.
[3] Start-up time is defined as the time between the rising edge of EN1 to V_{OUT1} being at 90% of its nominal value.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE (LDO1, LDO2)[1]	C_{MIN}	T_A = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		1	Ω

[1] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during capacitor selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with this LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN1, EN1, MSEL to GND	−0.3 V to +6.5 V
VOUT1, VOUT2 to GND	−0.3 V to V_{IN1}
VIN2, VIN3, EN2, GPIN1, GPIN2, GPIN3 to GND	−0.3 V to +3.6 V
VOUT3, GPOUT1 to GND	−0.3 V to V_{IN2}
GPOUT2, GPOUT3 to GND	−0.3 V to V_{IN3}
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP5030 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required.

The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4-inch × 3-inch circuit board. Refer to JEDEC JESD51-9 for detailed information about board construction. For more information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package* at www.analog.com.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JEDEC JESD51-12 document, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path, as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package, as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to the JEDEC JESD51-8 and JESD51-12 documents for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
16-Ball, 0.4 mm Pitch WLCSP	66.6	18.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

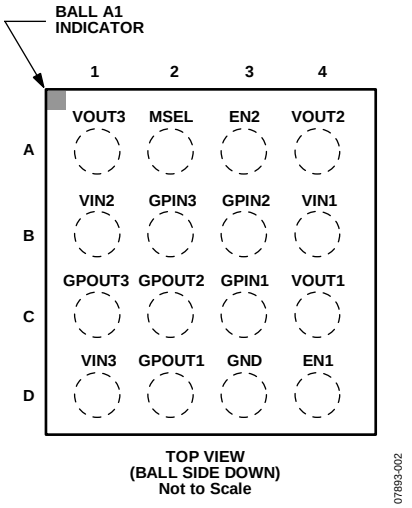

Figure 2. Pin Configuration, Top View

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VOUT3	Load Switch Output.
A2	MSEL	Select Activation Logic for LDO2 and Load Switch. Connect MSEL to GND to select Mode 1. Connect MSEL to VIN1 to select Mode 2.
A3	EN2	Enable VOUT2 and VOUT3. When MSEL is set to Logic 0 (Mode 1), VOUT2/VOUT3 activation is the logic NOR of EN2 with GPIN1. When MSEL is set to Logic 1 (Mode 2), VOUT2/VOUT3 activation is the logic AND of EN2 with NOT GPIN1.
A4	VOUT2	LDO2 Output.
B1	VIN2	Digital Supply Input.
B2	GPIN3	Input to Level Shifter.
B3	GPIN2	Input to Level Shifter.
B4	VIN1	System Supply.
C1	GPOUT3	Output of Level Shifter.
C2	GPOUT2	Output of Level Shifter.
C3	GPIN1	Input to Level Shifter.
C4	VOUT1	LDO1 Output.
D1	VIN3	Logic Translator Supply.
D2	GPOUT1	Output of Level Shifter.
D3	GND	Ground.
D4	EN1	Enable VOUT1.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 3.3 V, V_{OUT1} = 1.2 V, V_{OUT2} = 2.8 V, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = C_{OUT1} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

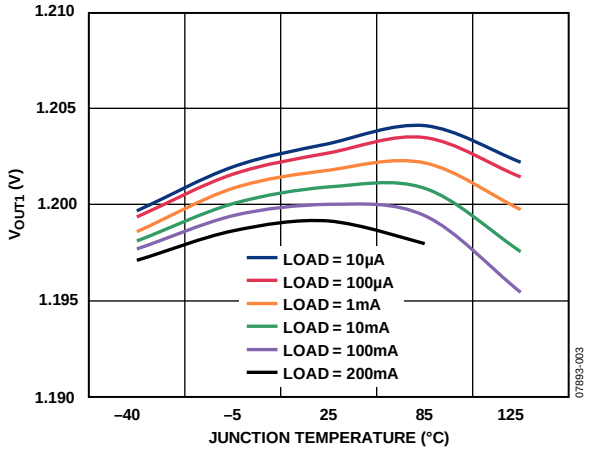

Figure 3. V_{OUT1} Output Voltage vs. Junction Temperature

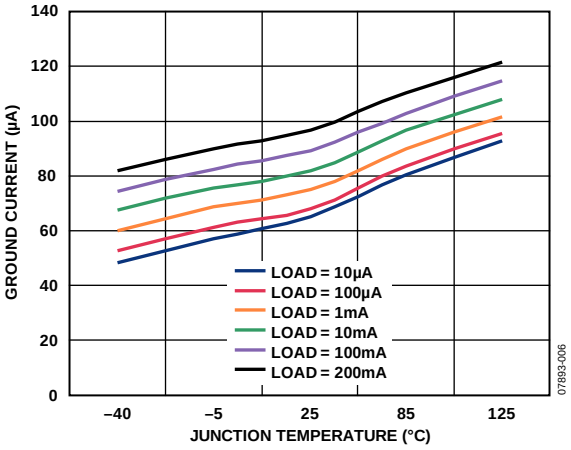

Figure 6. Ground Current vs. Junction Temperature, V_{OUT2} Loaded

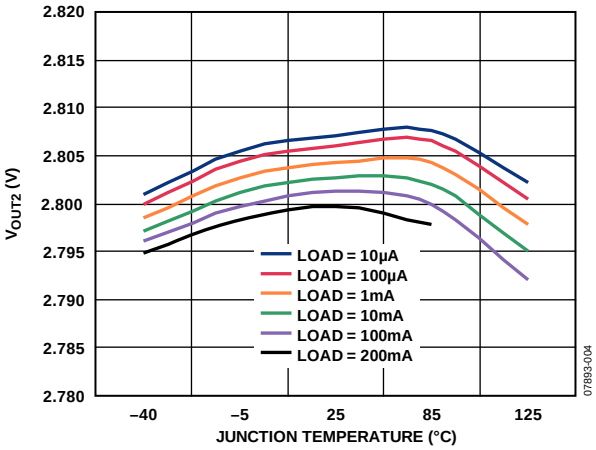

Figure 4. V_{OUT2} Output Voltage vs. Junction Temperature

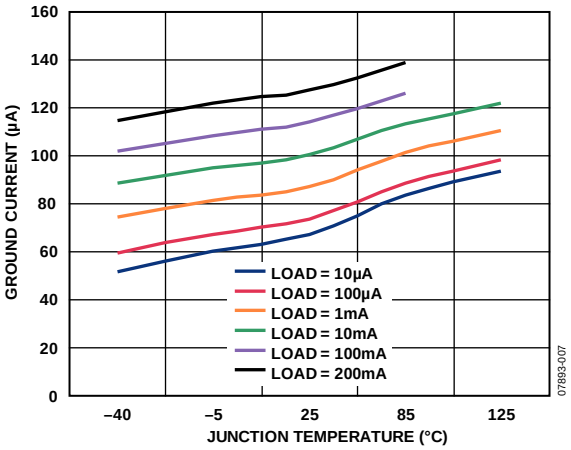

Figure 7. Ground Current vs. Junction Temperature, Both LDOs Loaded

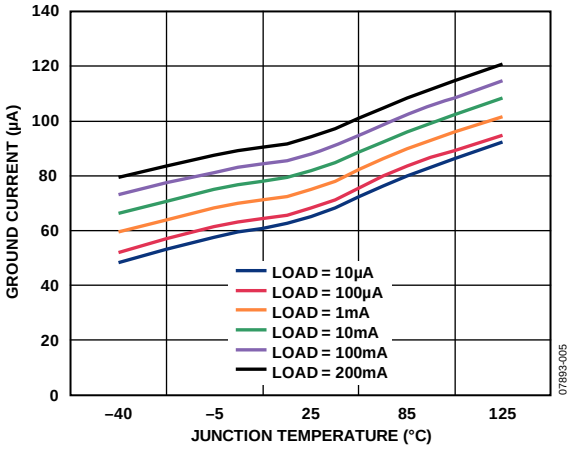

Figure 5. Ground Current vs. Junction Temperature, V_{OUT1} Loaded

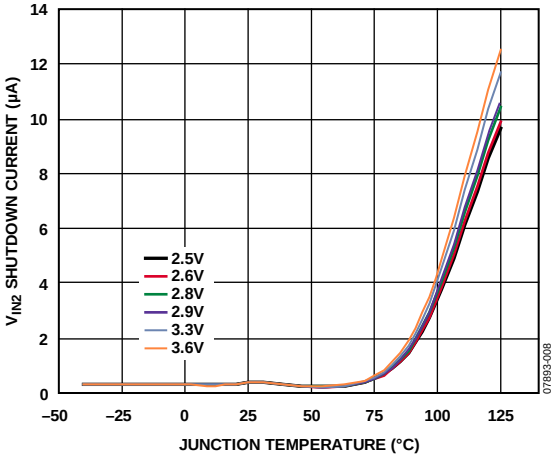

Figure 8. V_{IN2} Shutdown Current vs. Junction Temperature at Various Input Voltages

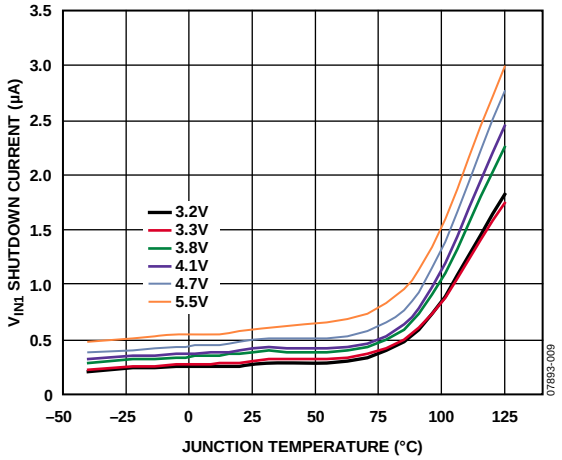

Figure 9. V_{IN1} Shutdown Current vs. Junction Temperature at Various Input Voltages

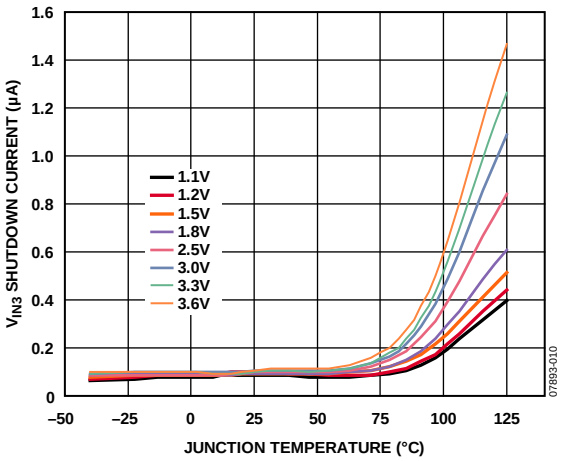

Figure 10. V_{IN3} Shutdown Current vs. Junction Temperature at Various Input Voltages

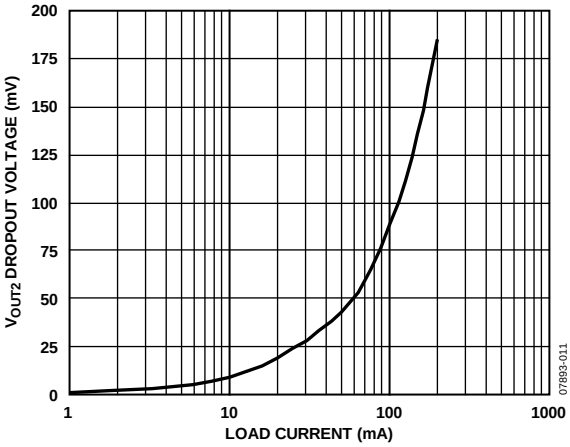

Figure 11. V_{OUT2} Dropout Voltage vs. Load Current

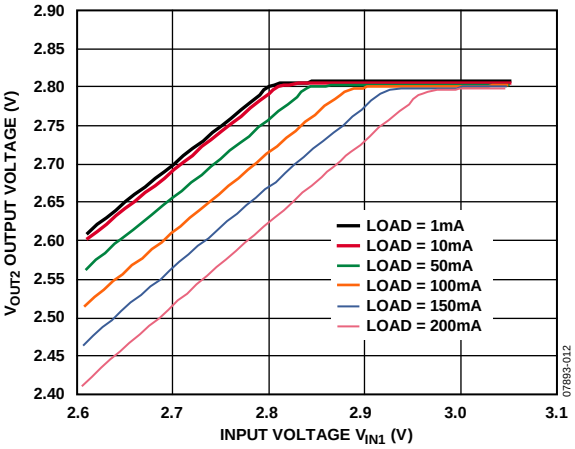

Figure 12. V_{OUT2} Output Voltage vs. Input Voltage (in Dropout) and Load Current

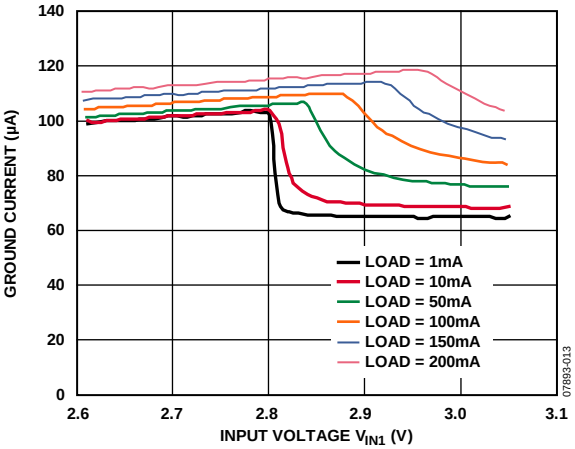

Figure 13. Ground Current for V_{OUT2} (in Dropout) vs. Input Voltage and Load Current

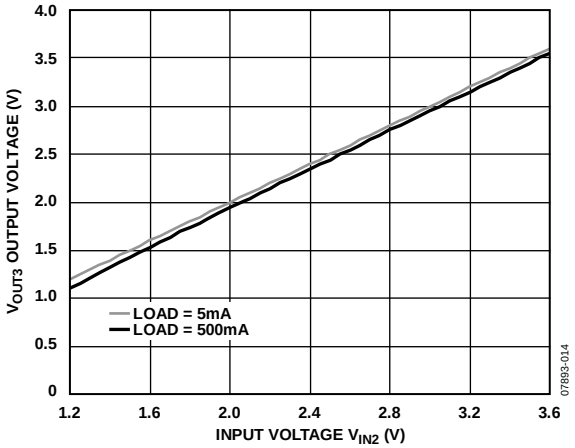

Figure 14. Load Switch (V_{OUT3}) Output Voltage vs. Input Voltage and Load Current

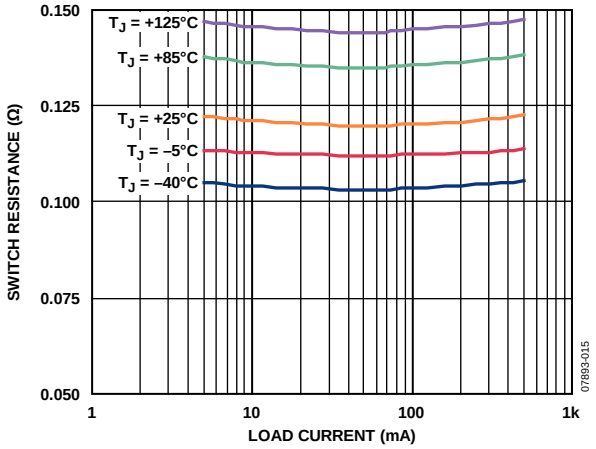

Figure 15. Load Switch RDS_{ON} vs. Load Current, V_{IN2} = 1.8 V

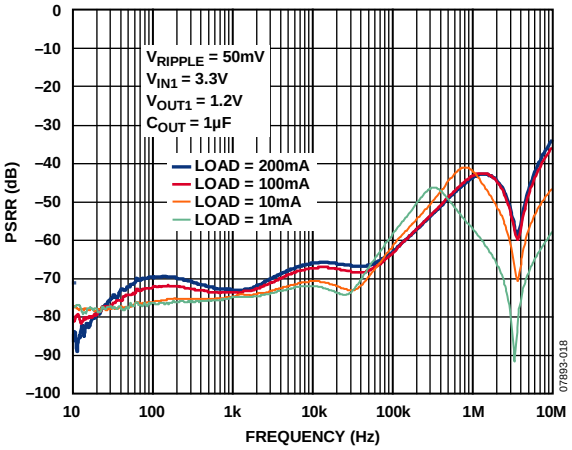

Figure 18. Power Supply Rejection Ratio vs. Frequency, V_{IN1} = 3.3 V, V_{OUT1} = 1.2 V

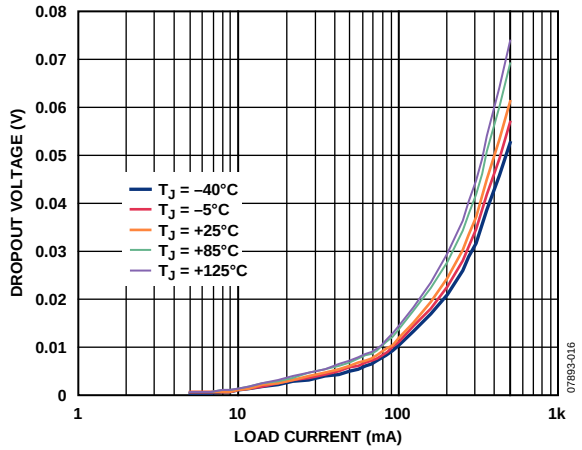

Figure 16. Load Switch Dropout Voltage vs. Load Current, V_{IN2} = 1.8 V

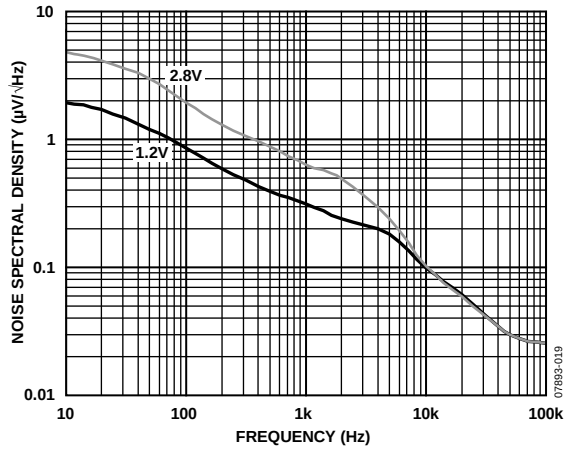

Figure 19. Output Noise Spectral Density vs. Output Voltage, V_{IN1} = 5 V, I_{LOAD} = 10 mA

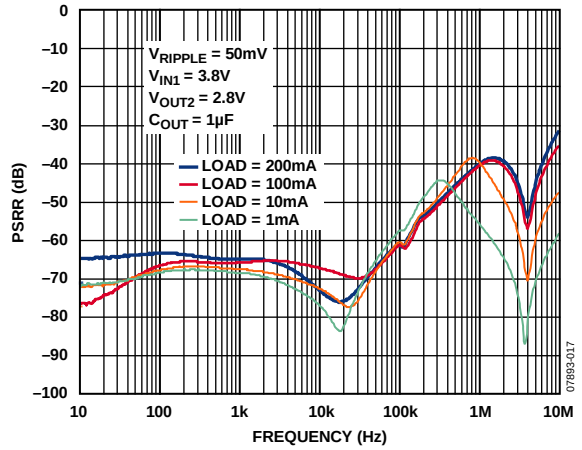

Figure 17. Power Supply Rejection Ratio vs. Frequency, V_{IN1} = 3.8 V, V_{OUT2} = 2.8 V

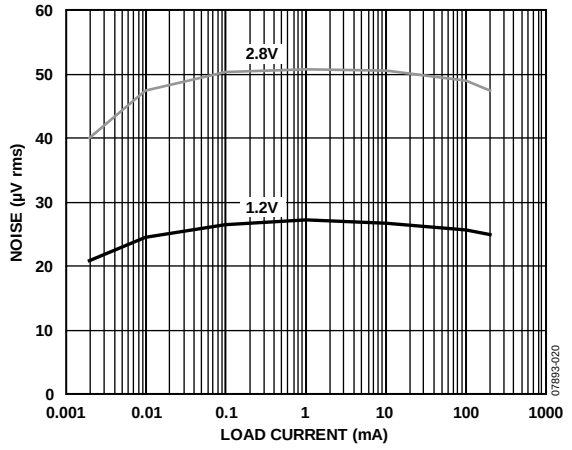

Figure 20. RMS Output Noise vs. Load Current and Output Voltage, V_{IN1} = 5 V

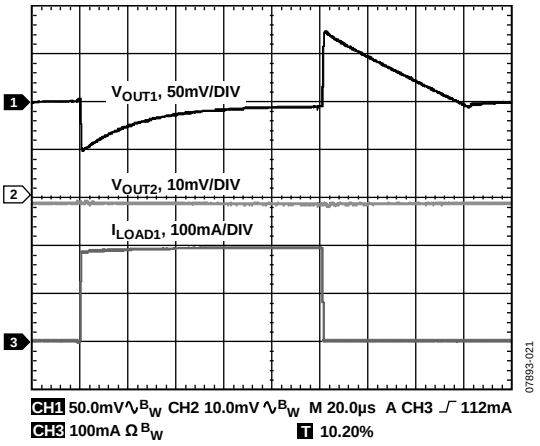

Figure 21. Load Transient Response, I_{LOAD1} = 1 mA to 200 mA, I_{LOAD2} = 1 mA, CH1 = V_{OUT1}, CH2 = V_{OUT2}, CH3 = I_{LOAD1}, C_{OUT} = 1 µF

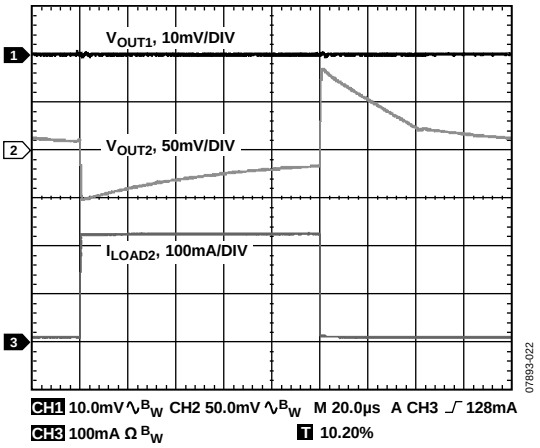

Figure 22. Load Transient Response, I_{LOAD1} = 1 mA, I_{LOAD2} = 1 mA to 200 mA, CH1 = V_{OUT1}, CH2 = V_{OUT2}, CH3 = I_{LOAD2}

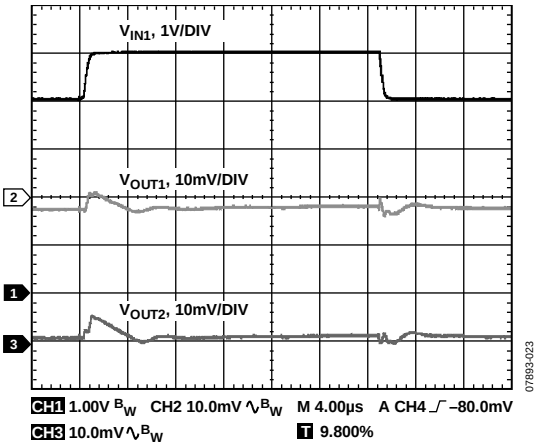

Figure 23. Line Transient Response, V_{IN1} = 4 V to 5 V, I_{LOAD1} = 1 mA, I_{LOAD2} = 1 mA, CH1 = V_{IN1}, CH2 = V_{OUT1}, CH3 = V_{OUT2}

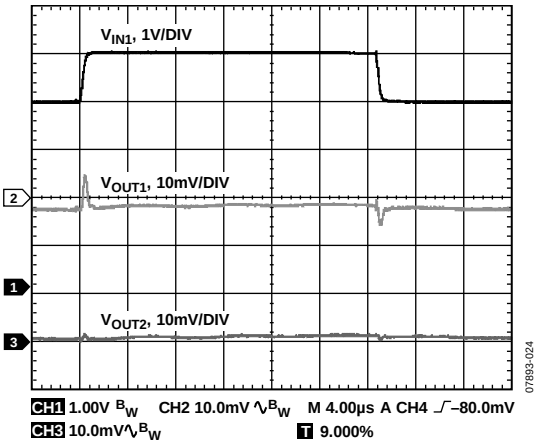

Figure 24. Line Transient Response, V_{IN1} = 4 V to 5 V, I_{LOAD1} = 200 mA, I_{LOAD2} = 200 mA, CH1 = V_{IN1}, CH2 = V_{OUT1}, CH3 = V_{OUT2}

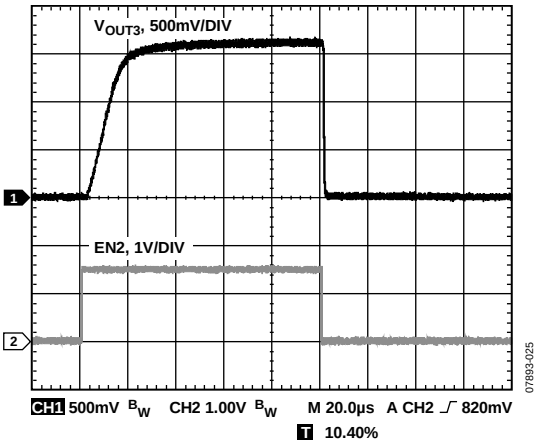

Figure 25. Load Switch Typical Switching Time, I_{LOAD3} = 500 mA, CH1 = V_{OUT3}, CH2 = EN2

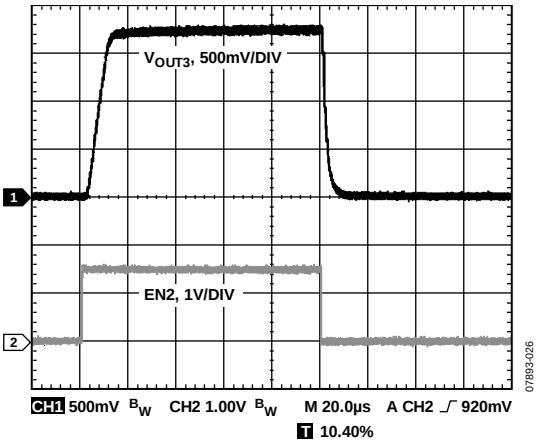

Figure 26. Load Switch Typical Switching Time, I_{LOAD3} = 100 mA, CH1 = V_{OUT3}, CH2 = EN2

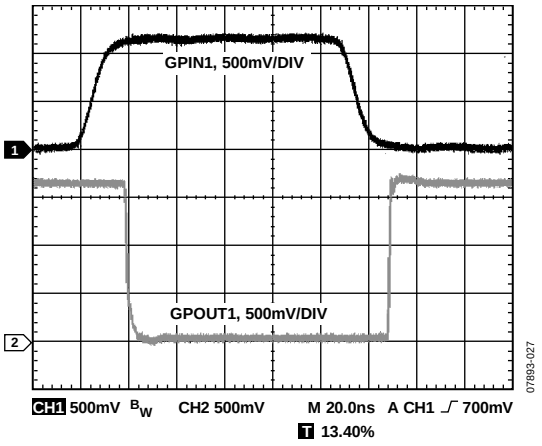

Figure 27. GPOUT1 Output vs. GPIN1 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 820 Ω Pull-Down, MSEL High, CH1 = GPIN1, CH2 = GPOUT1

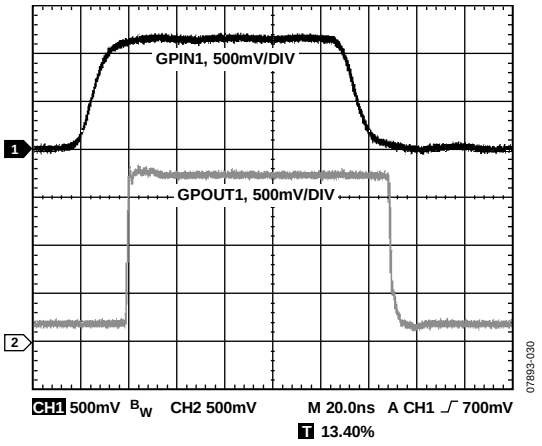

Figure 30. GPOUT1 Output vs. GPIN1 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 820 Ω Pull-Up, MSEL Low, CH1 = GPIN1, CH2 = GPOUT1

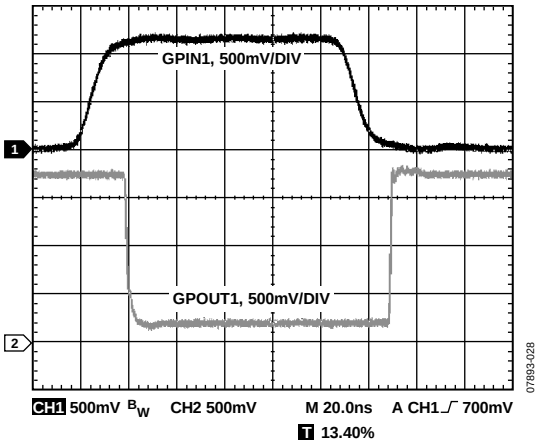

Figure 28. GPOUT1 Output vs. GPIN1 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 820 Ω Pull-Up, MSEL High, CH1 = GPIN1, CH2 = GPOUT1

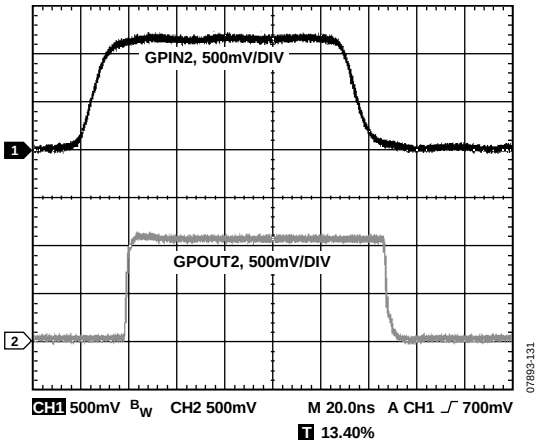

Figure 31. GPOUT2 Output vs. GPIN2 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 600 Ω Pull-Down, CH1 = GPIN2, CH2 = GPOUT2

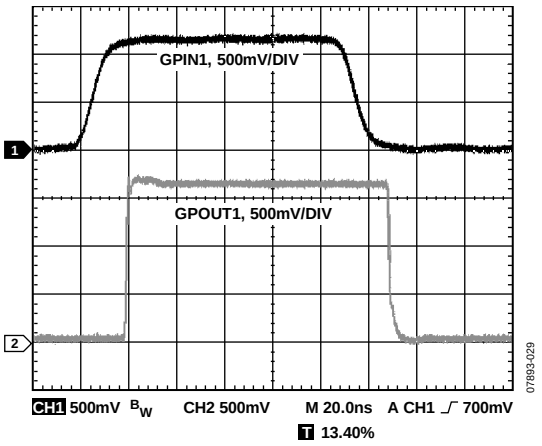

Figure 29. GPOUT1 Output vs. GPIN1 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 820 Ω Pull-Down, MSEL Low, CH1 = GPIN1, CH2 = GPOUT1

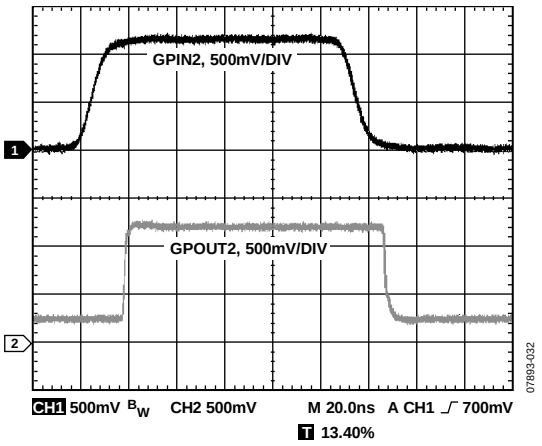

Figure 32. GPOUT2 Output vs. GPIN2 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 600 Ω Pull-Up, CH1 = GPIN2, CH2 = GPOUT2

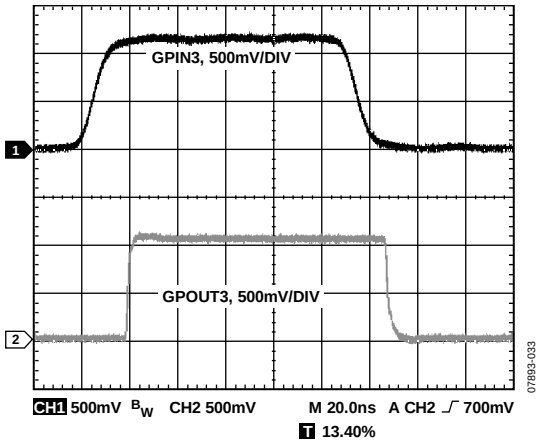

Figure 33. GPOUT3 Output vs. GPIN3 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 600 Ω Pull-Down, CH1 = GPIN3, CH2 = GPOUT3

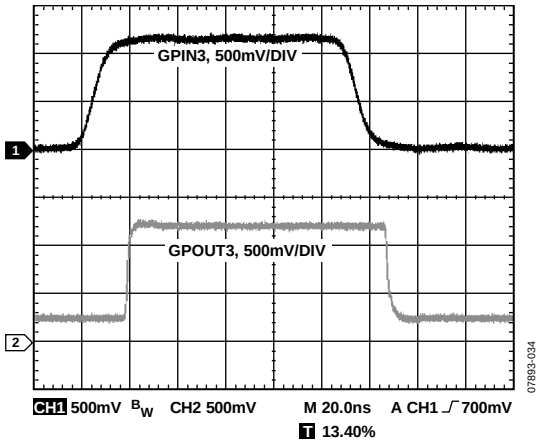

Figure 34. GPOUT3 Output vs. GPIN3 Input, V_{IN2} = 1.8 V, V_{IN3} = 1.2 V, 600 Ω Pull-Up, CH1 = GPIN3, CH2 = GPOUT3

THEORY OF OPERATION

The ADP5030 combines two high performance, low dropout voltage regulators and a low RDS_{ON} high-side load switch that operate from a 2.5 V to 5.5 V supply. Level shifting logic that operates from 1.2 V to 3.6 V supplies is also included to facilitate interfacing to system components. The ADP5030 can provide up to 200 mA of current from each LDO output and switch up to 500 mA. Drawing a low 220 µA quiescent current (maximum) at full load makes the ADP5030 ideal for battery-operated portable equipment. Shutdown current consumption is typically 400 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP5030 provides excellent transient performance.

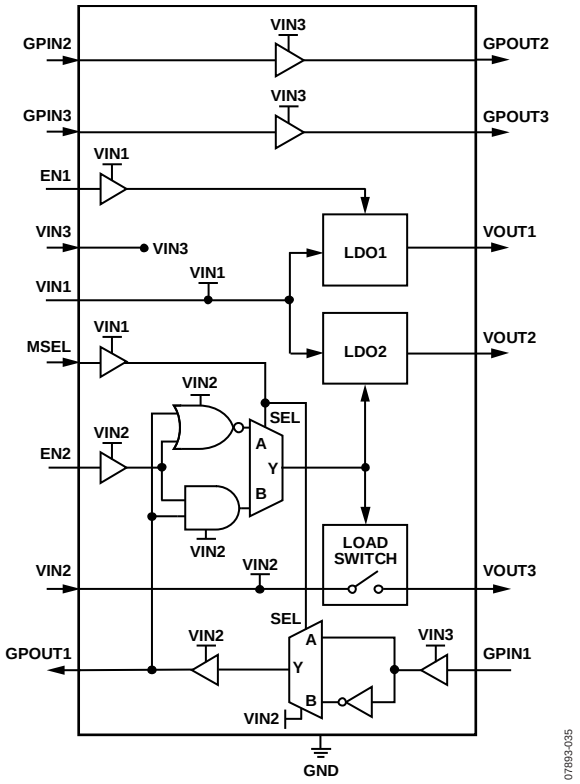

Figure 35. Internal Block Diagram

Internally, the ADP5030 LDOs consist of a reference, two error amplifiers, two feedback voltage dividers, and two PMOS pass transistors. Output current is delivered via the PMOS pass transistor, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

The ADP5030 high-side PMOS load switch is designed for supply operation from 1.2 V to 3.6 V and is designed for a low on resistance of 100 mΩ at V_{IN2} = 1.8 V. The load switch can carry 500 mA of continuous current.

The ADP5030 level shifting logic translates logic levels from the control signal operating on VIN2 to the circuitry operating on VIN3 and vice versa.

The ADP5030 uses the EN1 and EN2 pins to control the VOUTx pins under normal operating conditions. The MSEL pin is used to select the activation logic for LDO2. When MSEL is set to Logic 0, LDO2 and load switch activation is the logic NOR of EN2 with GPIN1. When MSEL is set to Logic 1, the load switch activation and LDO2 is the logic AND of EN2 with NOT GPIN1.

APPLICATIONS INFORMATION

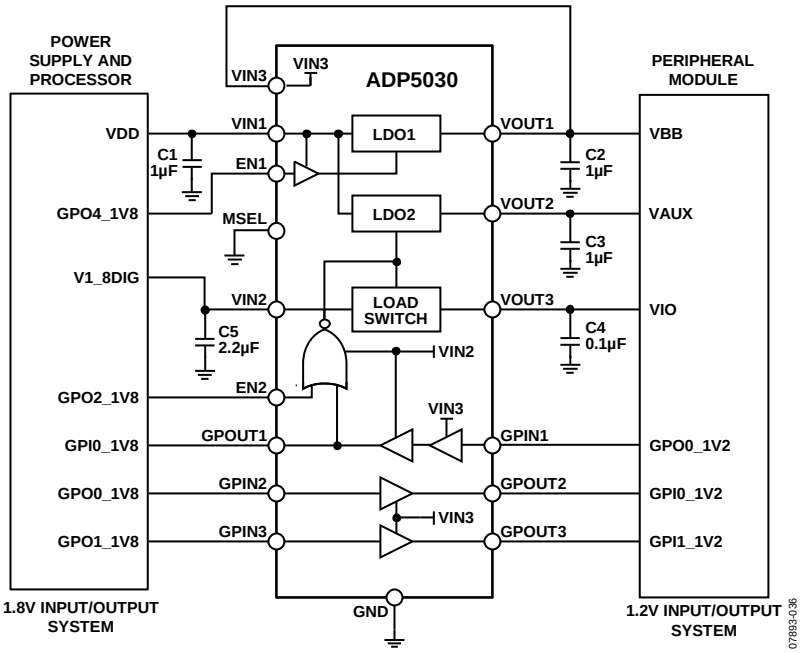

Figure 36. Application Diagram (MSEL Low)

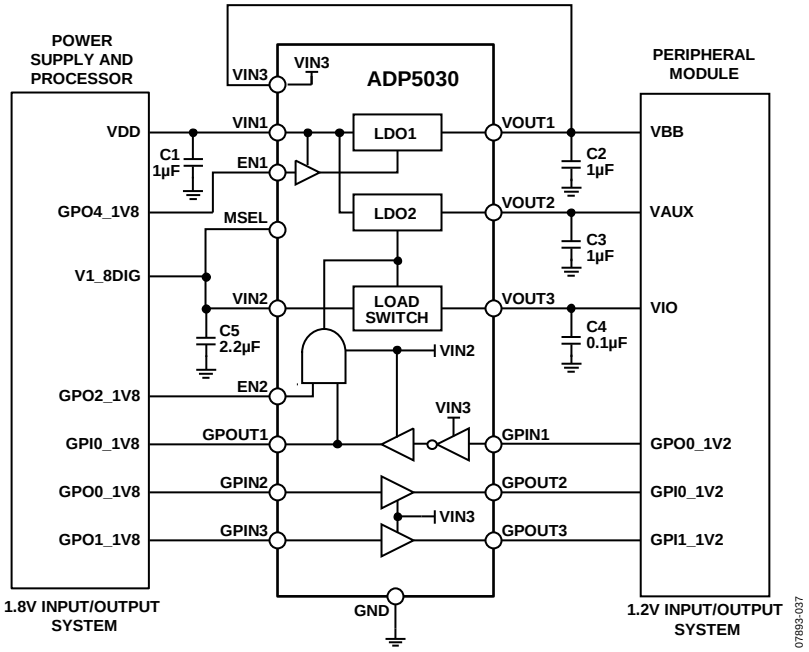

Figure 37. Application Diagram (MSEL High)

LDO2 AND LOAD SWITCH ACTIVATION LOGIC

The activation logic for LDO2 and the load switch is selected through the MSEL pin. When MSEL is set to Logic 0, LDO2 and load switch activation is the logic NOR of EN2 with GPIN1. When MSEL is set to Logic 1, LDO2 and load switch activation is the logic AND of EN2 with NOT GPIN1 (see Table 6). In both modes, VIN3 is a dedicated input for the logic translators.

Table 6. Truth Table for LDO2 and Load Switch Activation

MSEL	EN2	GPIN1	LDO2 State	Load Switch State
0	0	0	On	Closed
0	1	0	Off	Off
0	0	1	Off	Off
0	1	1	Off	Off
1	0	0	Off	Off
1	1	0	On	Closed
1	0	1	Off	Off
1	1	1	Off	Off

SEQUENCING

The input supply voltage V_{IN1} must be present before applying V_{IN2} and V_{IN3}.

During a thermal shutdown event, LDO1, LDO2, and the load switch output turn off and are placed in a high impedance state. When the die temperature decreases below the recovery threshold, LDO1, LDO2, and the load switch output turn on if the respective enabling signal is still active.

CAPACITOR SELECTION

Output Capacitor

The ADP5030 LDOs are designed for operation with small, space-saving ceramic capacitors, but the part functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP5030. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5030 to large changes in load current. Figure 21 shows the transient response for an output capacitance value of 1 µF.

Input Bypass Capacitor

Connecting a 1 µF capacitor from VINx to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If an output capacitance greater than 1 µF is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADP5030, as long as the capacitor meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 38 shows the capacitance vs. voltage bias characteristics of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package size or voltage rating.

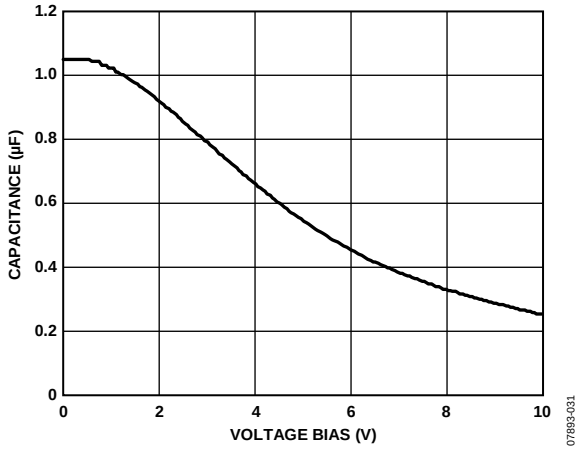

Figure 38. Capacitance vs. Voltage Bias Characteristics

Equation 1 can be used to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be ±15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 0.94 µF at 1.8 V, as shown in Figure 38.

Substituting these values into Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5030, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP5030 has an internal undervoltage lockout circuit on V_{IN1} that disables the inputs and outputs to the LDOs and the load switch when the input voltage is less than approximately 2.2 V. This ensures that the inputs and outputs of the ADP5030 behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP5030 uses the ENx pins to enable and disable the VOUTx pins under normal operating conditions. As shown in Figure 39 and Figure 40, when a rising voltage on ENx crosses the active threshold, VOUTx turns on. When a falling voltage on ENx crosses the inactive threshold, VOUTx turns off.

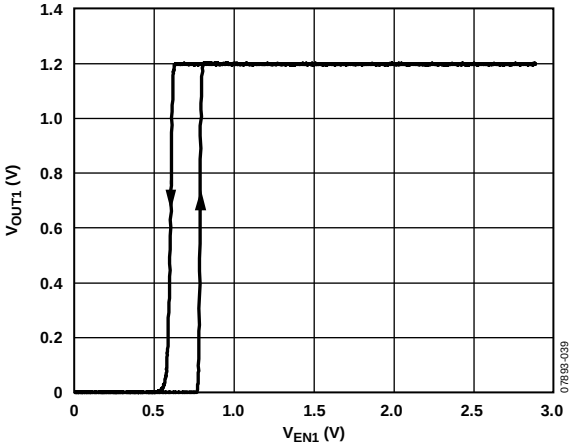

Figure 39. Typical EN1 Pin Operation

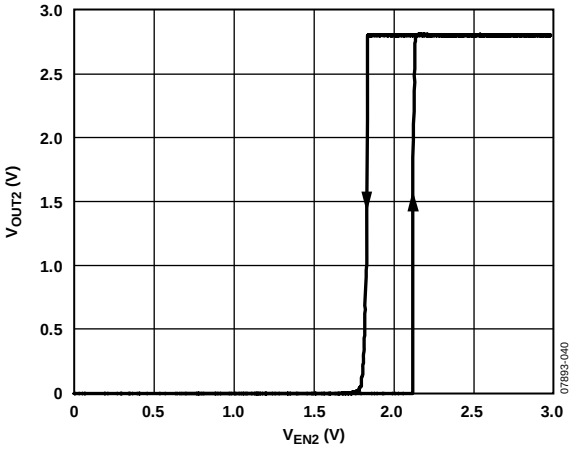

Figure 40. Typical EN2 Pin Operation

As shown in Figure 39 and Figure 40, the ENx pins have built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the ENx pins as they pass through the threshold points.

The active/inactive thresholds of the ENx pin are derived from the VINx voltage. Therefore, these thresholds vary with changing input voltage. Figure 41 and Figure 42 show typical ENx active/inactive thresholds when the input voltages vary from minimum to maximum.

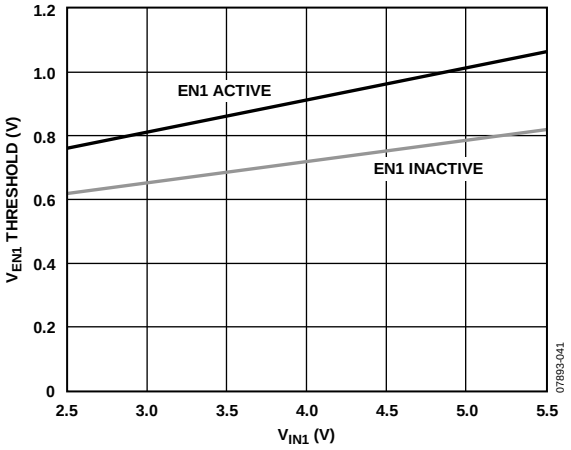

Figure 41. Typical EN1 Pin Thresholds vs. Input Voltage

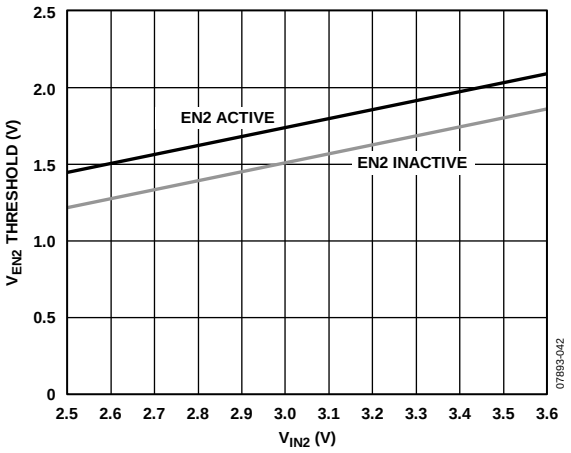

Figure 42. Typical EN2 Pin Thresholds vs. Input Voltage

The ADP5030 uses an internal soft start to limit the inrush current when the outputs are enabled. The typical start-up time for a 2.8 V output is approximately 240 µs from the time that the ENx active threshold is crossed to when the output reaches 90% of its final value. The start-up time for a 1.2 V output is about 120 µs. The start-up time is somewhat dependent on the output voltage setting and increases slightly as the output voltage increases. Figure 43 and Figure 44 show the typical start-up times for 1.2 V and 2.8 V outputs, respectively.

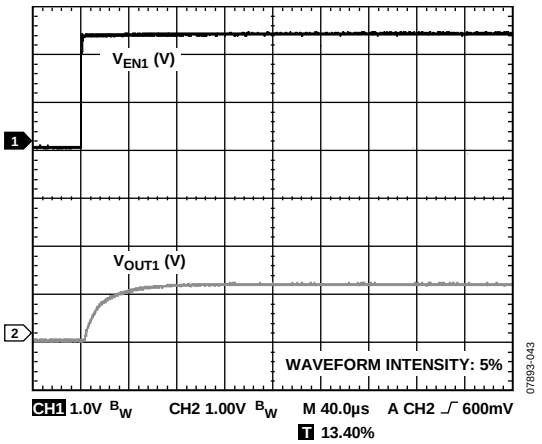

Figure 43. Typical Start-Up Time, V_{OUT1} = 1.2 V

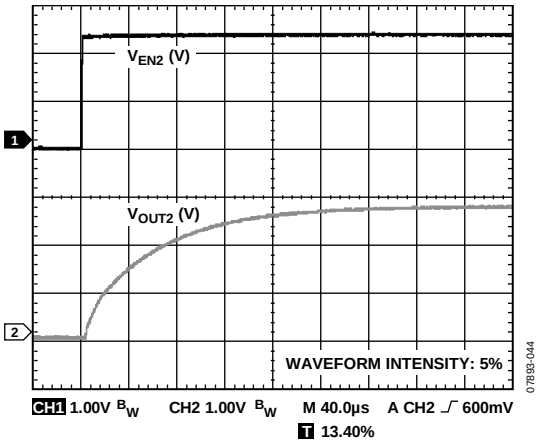

Figure 44. Typical Start-Up Time, V_{OUT2} = 2.8 V

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP5030 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP5030 is designed to reach current limit when the output load reaches 300 mA (typical). When the output load exceeds 300 mA, the output voltage is reduced to maintain a constant current limit.

The load switch is not current-limited so care must be taken to ensure that the output of the load switch is not shorted to ground under any conditions. In the event of a short to ground, the load switch current is limited by the maximum output current of the source.

Thermal overload protection is built in, which limits the junction temperature to a maximum of 155°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature begins to rise above 155°C, the output is turned off, reducing the output current to 0 mA. When the junction temperature drops below 140°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUTx to GND occurs. At first, the ADP5030 reaches current limit, so that only 300 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 155°C, thermal shutdown is activated, turning off the output and reducing the output current to 0 mA. As the junction temperature cools and drops below 140°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 155°C. This thermal oscillation between 140°C and 155°C causes a current oscillation between 0 mA and 300 mA that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

Due to high efficiency, the ADP5030 does not dissipate a lot of heat in most applications. However, in applications with a high ambient temperature and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum specified junction temperature of 125°C.

When the junction temperature exceeds 155°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 140°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP5030 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds used and the amount of copper to which the pins of the package are soldered on the PCB. Table 7 shows typical θ_{JA} values for the ADP5030 for various PCB copper sizes.

Table 7. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	200
50	173
100	135
300	95
500	76

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP5030 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = \Sigma[(V_{IN} - V_{OUT}) \times I_{LOAD}] + \Sigma(V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_A + \{\Sigma[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 45 through Figure 49 show junction temperature calculations for different ambient temperatures, total power dissipation, and areas of PCB copper.

In cases where the board temperature is known, the thermal characterization parameter Ψ_{JB} can be used to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and the power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical Ψ_{JB} value for the 16-ball WLCSP is 18.5°C/W.

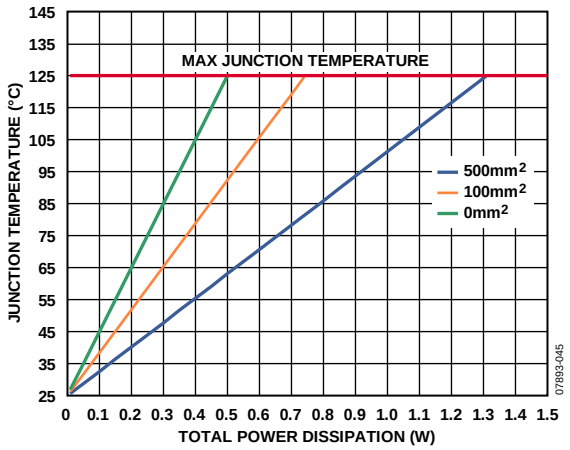

Figure 45. Junction Temperature vs. Total Power Dissipation, T_A = 25°C

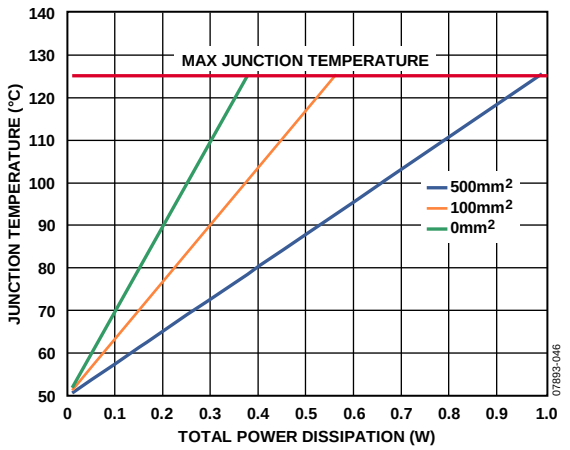

Figure 46. Junction Temperature vs. Total Power Dissipation, T_A = 50°C

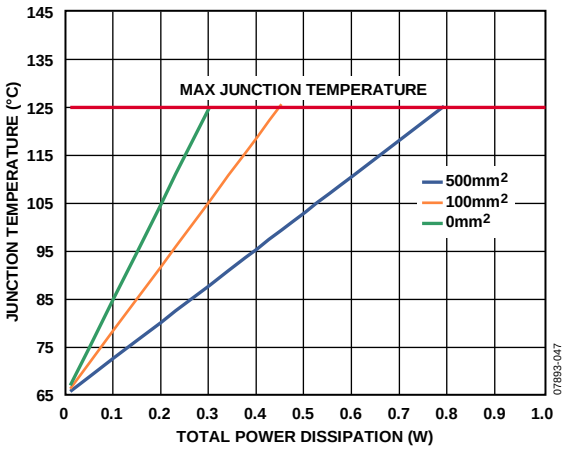

Figure 47. Junction Temperature vs. Total Power Dissipation, T_A = 65°C

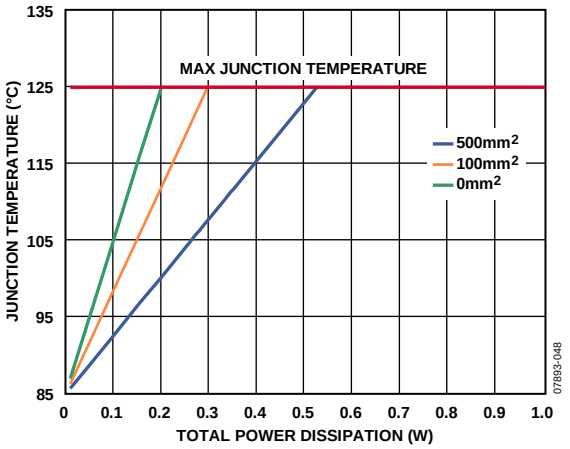

Figure 48. Junction Temperature vs. Total Power Dissipation, T_A = 85°C

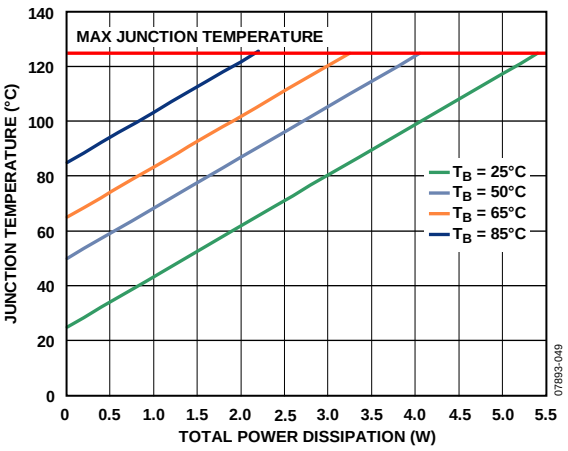

Figure 49. Junction Temperature vs. Total Power Dissipation and Board Temperature

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP5030. However, as shown in Table 7, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VINx and GND pins. Place the output capacitors as close as possible to the VOUTx and GND pins. Use 0402 or 0603 size capacitors and resistors to achieve the smallest possible footprint solution on boards where area is limited.

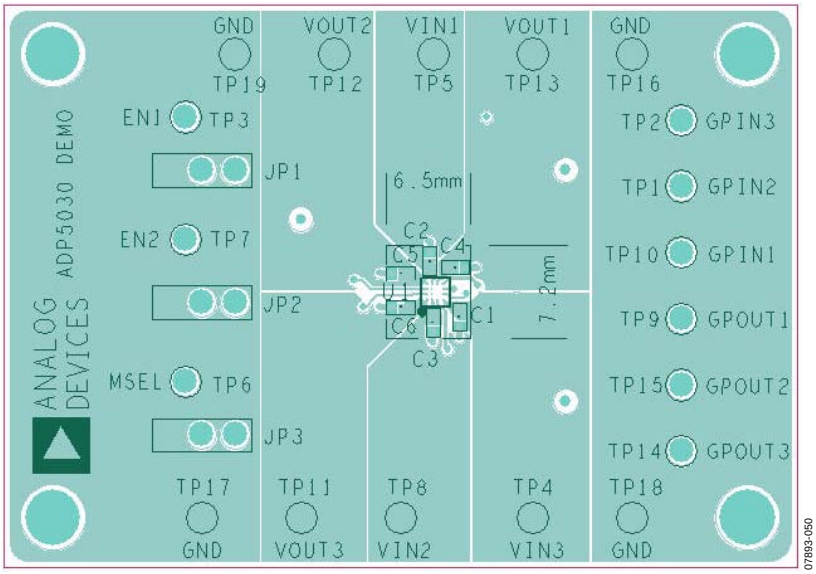

Figure 50. Example of PCB Layout, Top Side

OUTLINE DIMENSIONS

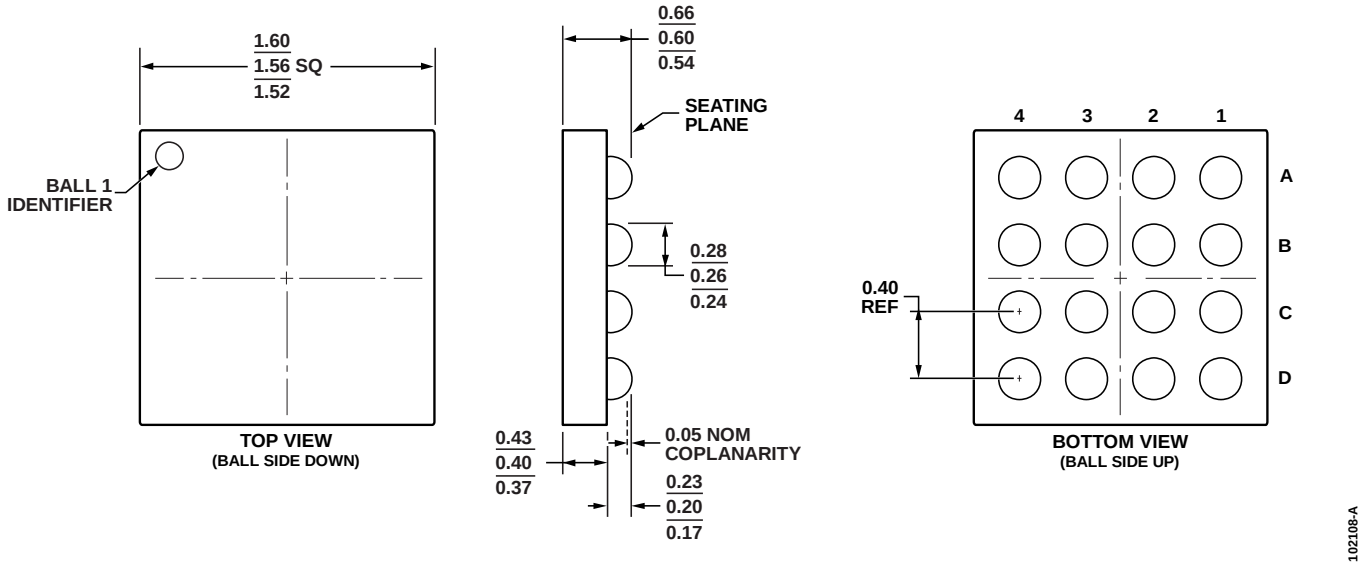

Figure 51. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-6)
Dimensions show in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltages (V)[1]	Package Description	Package Option	Branding
ADP5030ACBZ-1228R7[2]	−40°C to +125°C	1.2 V, 2.8 V	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-6	L9K

[1] For additional voltage options, contact a local sales or distribution representative.
[2] Z = RoHS Compliant Part.

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