# Charge Pump, 7-Channel Fun Lighting LED Driver

Data Sheet

# ADP8863

## FEATURES

- Automated blinking and funlight timing for each LED driver
- 16 programmable fade in and fade out times
  - 0.1 sec to 5.5 sec
  - Selectable linear, square, or cubic fade rates
- 7 independent and programmable LED drivers
  - 7 drivers capable of 30 mA (maximum)
  - 1 driver also capable of 60 mA (maximum)
- Programmable maximum current limit (128 levels)
- Separate and independent controls for backlight LEDs
- Backlight fade override
- Up to two built-in comparator inputs with programmable modes for ambient light sensing
- Charge pump with automatic gain selection of 1×, 1.5×, and 2× for maximum efficiency
- Standby mode for <1 µA current consumption
- I²C-compatible interface for all programming
- Dedicated reset pin and built-in power-on reset (POR)
- Short-circuit, overvoltage, and overtemperature protection
- Internal soft start to limit inrush currents
- Input-to-output isolation during faults or shutdown
- Operation down to $V_{IN}$ = 2.5 V with undervoltage lockout (UVLO) at $V_{IN}$ = 2.0 V
- Available in a small 20-ball, 2.15 mm × 2.36 mm × 0.6 mm WLCSP or a 20-lead, 4 mm × 4 mm × 0.75 mm LFCSP

## APPLICATIONS

- LED indication
- Funlight indicator lighting
- Keypad backlighting
- RGB LED color generation and mixing
- General backlighting of small format displays

## TYPICAL OPERATING CIRCUIT

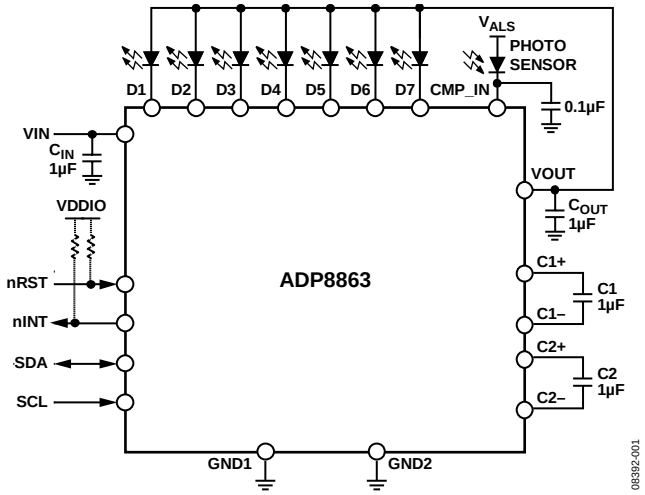


*Figure 1.*

## GENERAL DESCRIPTION

The ADP8863 combines a powerful charge pump driver with advanced autonomous LED lighting features. It allows as many as seven LEDs to be independently driven up to 30 mA (maximum). The seventh LED can also be driven to 60 mA (maximum). All LEDs are programmable for maximum current and fade in/fade out times via the I²C interface.

Additionally, automated blinking routines can be independently programmed and enabled for all seven LED channels. These LEDs can also be combined into groups to reduce the processor instructions.

This entire configuration is driven by a two-capacitor charge pump with gains of 1×, 1.5×, and 2×. The charge pump is capable of driving a maximum $I_{OUT}$ of 240 mA from a supply of 2.5 V to 5.5 V. The device includes a variety of safety features including short-circuit, overvoltage, and overtemperature protection. These features allow easy implementation of a safe and robust design. Additionally, input inrush currents are limited via an integrated soft start combined with controlled input-to-output isolation.

Rev. B
Document Feedback


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**Last Content Update: 11/08/2017**

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADP8863 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- ADP8863: Charge Pump, 7-Channel Fun Lighting LED Driver Data Sheet

**User Guides**

- UG-005: Software User Guide

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADP8860 Back-light LED Linux Driver

## DESIGN RESOURCES

- ADP8863 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADP8863 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

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## DOCUMENT FEEDBACK

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## REVISION HISTORY

**10/2017—Rev. A to Rev. B**

Changed CP-20-10 to CP-20-8 ... Throughout
Updated Outline Dimensions ... 48
Changes to Ordering Guide ... 49

**6/2010—Rev. 0 to Rev. A**

Changes to Features Section and General Description Section . 1
Changes to Thermal Resistance Section and Table 3 ... 5
Added Figure 4; Renumbered Sequentially ... 6
Changes to Table 4 ... 6
Updated Outline Dimensions ... 48
Changes to Ordering Guide ... 49

**4/2010—Revision 0: Initial Version**

# SPECIFICATIONS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nINT = open, nRST = 2.7 V, CMP_IN = 0 V, $V_{D1:D7}$ = 0.4 V, Capacitor C1 = 1 µF, Capacitor C2 = 1 µF, $C_{OUT}$ = 1 µF, typical values are at $T_A$ = 25°C and are not guaranteed, minimum and maximum limits are guaranteed from $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SUPPLY | | | | | | |
| Input Voltage | | | | | | |
| Operating Range | $V_{IN}$ | | 2.5 | | 5.5 | V |
| Start-Up Level | $V_{IN(START)}$ | $V_{IN}$ increasing | | 2.05 | 2.30 | V |
| Low Level | $V_{IN(STOP)}$ | $V_{IN}$ decreasing | 1.75 | 1.97 | | V |
| $V_{IN(START)}$ Hysteresis | $V_{IN(HYS)}$ | After startup | | 80 | | mV |
| UVLO Noise Filter | $t_{UVLO}$ | | | 10 | | µs |
| Quiescent Current | $I_Q$ | | | | | |
| Prior to $V_{IN(START)}$ | $I_{Q(START)}$ | $V_{IN} = V_{IN(START)} - 100$ mV | | 10 | | µA |
| During Standby | $I_{Q(STBY)}$ | $V_{IN}$ = 3.6 V, Bit nSTBY = 0, SCL = SDA = 0 V | | 0.3 | 1.0 | µA |
| After Startup and Switching | $I_{Q(ACTIVE)}$ | $V_{IN}$ = 3.6 V, Bit nSTBY = 1, $I_{OUT}$ = 0 mA, gain = 2× | | 4.5 | 7.2 | mA |
| OSCILLATOR | | | | | | |
| Switching Frequency | $f_{SW}$ | | 0.8 | 1 | 1.32 | MHz |
| Duty Cycle | D | | | 50 | | % |
| OUTPUT CURRENT CONTROL | | | | | | |
| Maximum Drive Current | $I_{D1:D7(MAX)}$ | $V_{D1:D7}$ = 0.4 V | | | | |
| D1 to D7 | | Bit SCR = 0 in the ISC7 register | | | | |
| $T_J$ = 25°C | | | 26.2 | 30 | 34.1 | mA |
| $T_J$ = −40°C to +85°C | | | 24.4 | | 34.1 | mA |
| D7 Only (60 mA Setting) | $I_{D7(60\ mA)}$ | $V_{D7}$ = 0.4 V, Bit SCR = 1 in the ISC7 register | | | | |
| $T_J$ = 25°C | | | 52.5 | 60 | 67 | mA |
| $T_J$ = −40°C to +85°C | | | 48.8 | | 67 | mA |
| LED Current Source Matching[1] | $I_{MATCH}$ | | | | | |
| All Current Sinks | $I_{MATCH7}$ | $V_{D1:D7}$ = 0.4 V | | 2.0 | | % |
| D2 to D7 Current Sinks | $I_{MATCH6}$ | $V_{D2:D7}$ = 0.4 V | | 1.5 | | % |
| Leakage Current on LED Pins | $I_{D1:D7(LKG)}$ | $V_{IN}$ = 5.5 V, $V_{D1:D7}$ = 2.5 V, Bit nSTBY = 1 | | | 0.5 | µA |
| Equivalent Output Resistance | $R_{OUT}$ | | | | | |
| Gain = 1× | | $V_{IN}$ = 3.6 V, $I_{OUT}$ = 100 mA | | 0.5 | | Ω |
| Gain = 1.5× | | $V_{IN}$ = 3.1 V, $I_{OUT}$ = 100 mA | | 3.0 | | Ω |
| Gain = 2× | | $V_{IN}$ = 2.5 V, $I_{OUT}$ = 100 mA | | 3.8 | | Ω |
| Regulated Output Voltage | $V_{OUT(REG)}$ | $V_{IN}$ = 3 V, gain = 2×, $I_{OUT}$ = 10 mA | 4.3 | 4.9 | 5.5 | V |
| AUTOMATIC GAIN SELECTION | | | | | | |
| Minimum Voltage | | | | | | |
| Gain Increases | $V_{HR(UP)}$ | Decrease $V_{D1:D7}$ until the gain switches up | 162 | 200 | 276 | mV |
| Minimum Current Sink Headroom Voltage | $V_{HR(MIN)}$ | $I_{DX} = I_{DX(MAX)} \times 95\%$ | | 180 | | mV |
| Gain Delay | $t_{GAIN}$ | The delay after gain has changed and before gain is allowed to change again | | 100 | | µs |
| AMBIENT LIGHT SENSING COMPARATORS | | | | | | |
| Ambient Light Sensor Current | $I_{ALS}$ | CMP_IN = $V_{D6}$ = 2.8 V, Bit CMP2_SEL = 1 | 0.70 | 1.08 | 1.33 | mA |
| DAC Bit Step | | | | | | |
| Threshold L2 Level | $I_{L2BIT}$ | $I_{L2BIT} = I_{ALS}/250$ | | 4.3 | | µA |
| Threshold L3 Level | $I_{L3BIT}$ | $I_{L3BIT} = I_{ALS}/2000$ | | 0.54 | | µA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FAULT PROTECTION | | | | | | |
| Start-Up Charging Current Source | $I_{SS}$ | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.8 × $V_{IN}$ | 2.5 | 3.75 | 5.5 | mA |
| Output Voltage Threshold | $V_{OUT}$ | | | | | |
| Exit Soft Start | $V_{OUT(START)}$ | $V_{OUT}$ rising | | 0.92 × $V_{IN}$ | | V |
| Short-Circuit Protection | $V_{OUT(SC)}$ | $V_{OUT}$ falling | | 0.55 × $V_{IN}$ | | V |
| Output Overvoltage Protection | $V_{OVP}$ | | | | | |
| Activation Level | | | | 5.8 | | V |
| OVP Recovery Hysteresis | $V_{OVP(HYS)}$ | | | 500 | | mV |
| Thermal Shutdown | | | | | | |
| Threshold | TSD | | | 150 | | °C |
| Hysteresis | $TSD_{(HYS)}$ | | | 20 | | °C |
| Isolation from Input to Output During Fault | $I_{OUTLKG}$ | $V_{IN}$ = 5.5 V, $V_{OUT}$ = 0 V, Bit nSTBY = 0 | | | 1.5 | µA |
| Time to Validate a Fault | $t_{FAULT}$ | | | 2 | | µs |
| I²C INTERFACE | | | | | | |
| Operating $V_{DDIO}$ Voltage | $V_{DDIO}$ | | | | 5.5 | V |
| Logic Low Input[2] | $V_{IL}$ | $V_{IN}$ = 3.6 V | | | 0.6 | V |
| Logic High Input[3] | $V_{IH}$ | $V_{IN}$ = 3.6 V | 1.30 | | | V |
| I²C TIMING SPECIFICATIONS | | Guaranteed by design | | | | |
| Delay from Reset Deassertion to I²C Access | $t_{RESET}$ | | | | 20 | µs |
| SCL Frequency | $f_{SCL}$ | | | | 400 | kHz |
| SCL High Time | $t_{HIGH}$ | | 0.6 | | | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | | | µs |
| Setup Time | | | | | | |
| Data | $t_{SU, DAT}$ | | 100 | | | ns |
| Repeated Start | $t_{SU, STA}$ | | 0.6 | | | µs |
| Stop Condition | $t_{SU, STO}$ | | 0.6 | | | µs |
| Hold Time | | | | | | |
| Data | $t_{HD, DAT}$ | | 0 | | 0.9 | µs |
| Start/Repeated Start | $t_{HD, STA}$ | | 0.6 | | | µs |
| Bus Free Time (Stop and Start Conditions) | $t_{BUF}$ | | 1.3 | | | µs |
| Rise Time (SCL and SDA) | $t_R$ | | 20 + 0.1 $C_B$ | | 300 | ns |
| Fall Time (SCL and SDA) | $t_F$ | | 20 + 0.1 $C_B$ | | 300 | ns |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |
| Capacitive Load per Bus Line | $C_B$ | | | | 400 | pF |

[1] Current source matching is calculated by dividing the difference between the maximum and minimum current from the sum of the maximum and minimum.
[2] $V_{IL}$ is a function of the input voltage. See Figure 16 in the Typical Performance Characteristics section for typical values over operating ranges.
[3] $V_{IH}$ is a function of the input voltage. See Figure 16 in the Typical Performance Characteristics section for typical values over operating ranges.

## I²C TIMING DIAGRAM

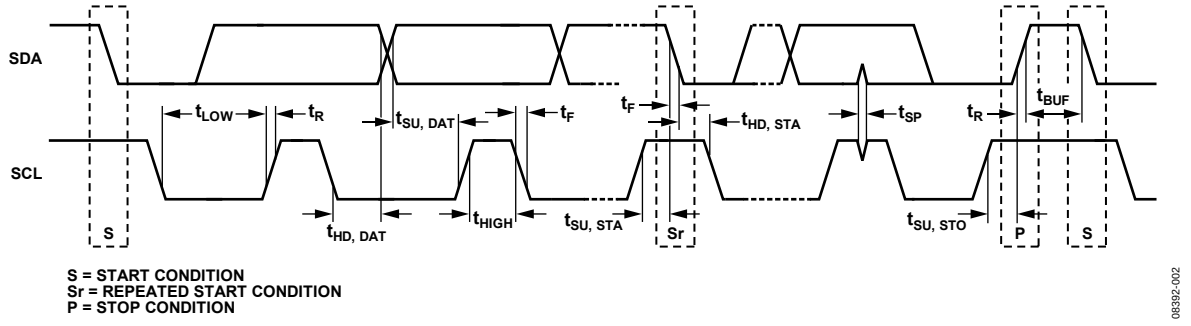


*Figure 2. I²C Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| VIN, VOUT | −0.3 V to +6 V |
| D1, D2, D3, D4, D5, D6, and D7 | −0.3 V to +6 V |
| CMP_IN | −0.3 V to +6 V |
| nINT, nRST, SCL, and SDA | −0.3 V to +6 V |
| Output Short-Circuit Duration | Indefinite |
| Operating Ambient Temperature Range | −40°C to +85°C[1] |
| Operating Junction Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Conditions | JEDEC J-STD-020 |
| ESD (Electrostatic Discharge) | |
| Human Body Model (HBM) | ±3 kV |
| Charged Device Model (CDM) | ±1.5 kV |

[1] The maximum operating junction temperature ($T_{J(MAX)}$) takes precedence over the maximum operating ambient temperature ($T_{A(MAX)}$). See the Maximum Temperature Ranges section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all voltages are referenced to ground.

## MAXIMUM TEMPERATURE RANGES

The maximum operating junction temperature ($T_{J(MAX)}$) takes precedence over the maximum operating ambient temperature ($T_{A(MAX)}$). Therefore, in situations where the ADP8863 is exposed to poor thermal resistance and high power dissipation ($P_D$), the maximum ambient temperature may need to be derated. In these cases, the maximum ambient temperature can be calculated with the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - (\theta_{JA} \times P_{D(MAX)})$$

## THERMAL RESISTANCE

$\theta_{JA}$ (junction to air) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The $\theta_{JA}$, $\theta_{JB}$ (junction to board), and $\theta_{JC}$ (junction to case) are determined according to JESD51-9 on a 4-layer printed circuit board (PCB) with natural convection cooling. For the LFCSP package, the exposed pad must be soldered to GND.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JB}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|---|
| WLCSP | 48 | 9 | N/A[1] | °C/W |
| LFCSP | 49.5 | N/A[1] | 5.3 | °C/W |

[1] N/A stands for not applicable.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

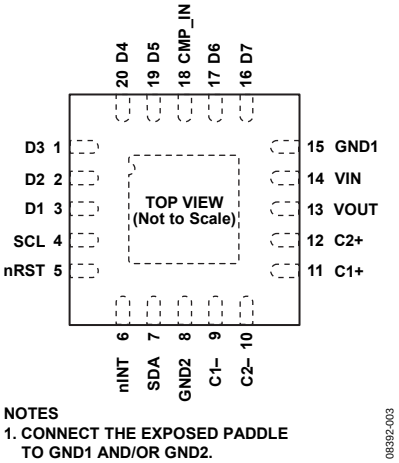


*Figure 3. LFCSP Pin Configuration*

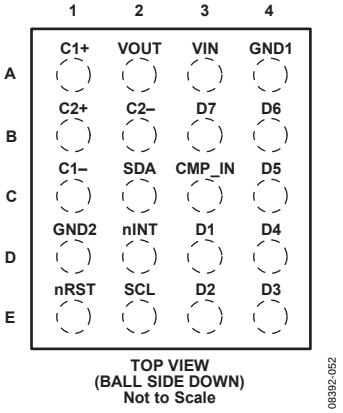


*Figure 4. WLCSP Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **LFCSP** | **WLCSP** | **Mnemonic** | **Description** |
| 14 | A3 | VIN | Input Voltage, 2.5 V to 5.5 V. |
| 3 | D3 | D1 | LED Sink 1. |
| 2 | E3 | D2 | LED Sink 2. |
| 1 | E4 | D3 | LED Sink 3. |
| 20 | D4 | D4 | LED Sink 4. |
| 19 | C4 | D5 | LED Sink 5. |
| 17 | B4 | D6 | LED Sink 6. This pin can also be selected as a comparator input for the second phototransistor. |
| 16 | B3 | D7 | LED Sink 7. |
| 18 | C3 | CMP_IN | Comparator Input for Phototransistor. When using this function, a capacitor (0.1 µF recommended) must be connected from this pin to ground. |
| 13 | A2 | VOUT | Charge Pump Output. |
| 11 | A1 | C1+ | Charge Pump C1+. |
| 9 | C1 | C1− | Charge Pump C1−. |
| 12 | B1 | C2+ | Charge Pump C2+. |
| 10 | B2 | C2− | Charge Pump C2−. |
| 15 | A4 | GND1 | Ground. Connect the exposed pad to GND1 and/or GND2. |
| 8 | D1 | GND2 | Ground. Connect the exposed pad to GND1 and/or GND2. |
| 6 | D2 | nINT | Processor Interrupt (Active Low). Requires an external pull-up resistor. If this pin is not used, it can be left floating. |
| 5 | E1 | nRST | Hardware Reset (Active Low). This pin resets the device to the default conditions. If not used, this pin must be tied above $V_{IH(MIN)}$. |
| 7 | C2 | SDA | $I^2C$ Serial Data. Requires an external pull-up resistor. |
| 4 | E2 | SCL | $I^2C$ Clock. Requires an external pull-up resistor. |
| 21 | NA | EPAD | Exposed Paddle. Connect the exposed paddle to GND1 and/or GND2. |

# TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6 V, SCL = 2.7 V, SDA = 2.7 V, nRST = 2.7 V, $V_{D1:D7}$ = 0.4 V, $C_{IN}$ = 1 µF, Capacitor C1 = 1 µF, Capacitor C2 = 1 µF, $C_{OUT}$ = 1 µF, $T_A$= 25°C, unless otherwise noted.

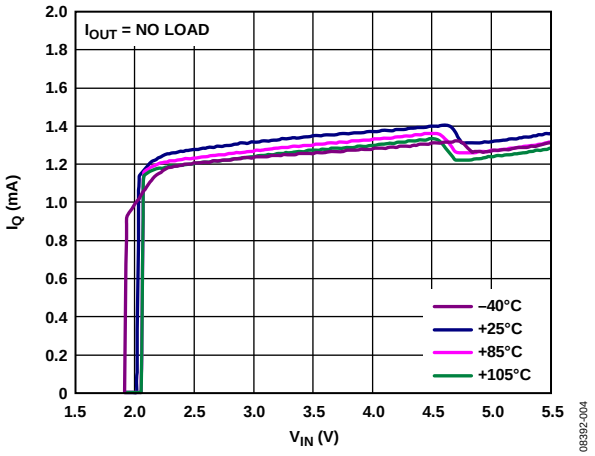


Figure 5. Typical Quiescent Current, G = 1×

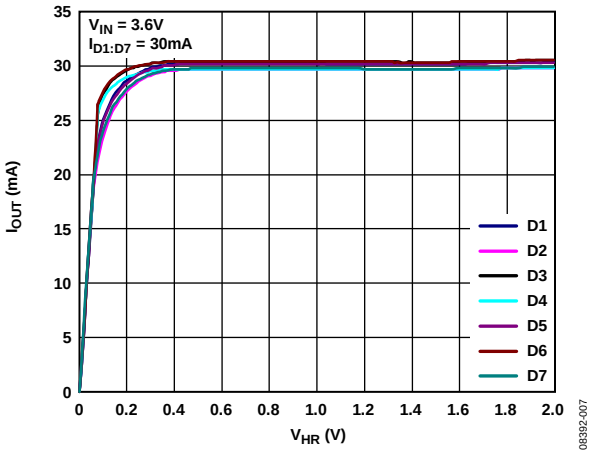


Figure 8. Typical Diode Current vs. Current Sink Headroom Voltage ($V_{HR}$)

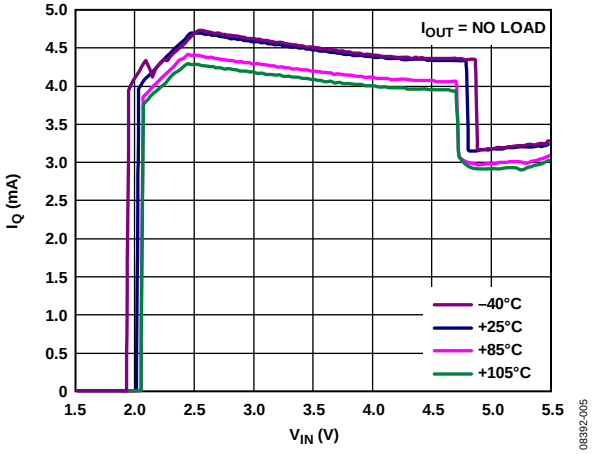


Figure 6. Typical Quiescent Current, G = 2×, $I_{Q(ACTIVE)}$

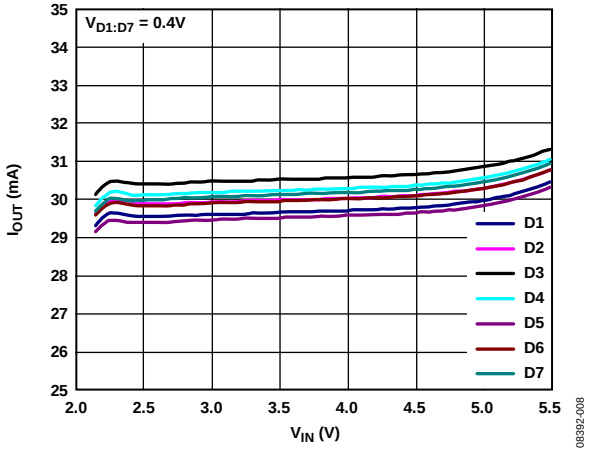


Figure 9. Typical Diode Matching vs. $V_{IN}$

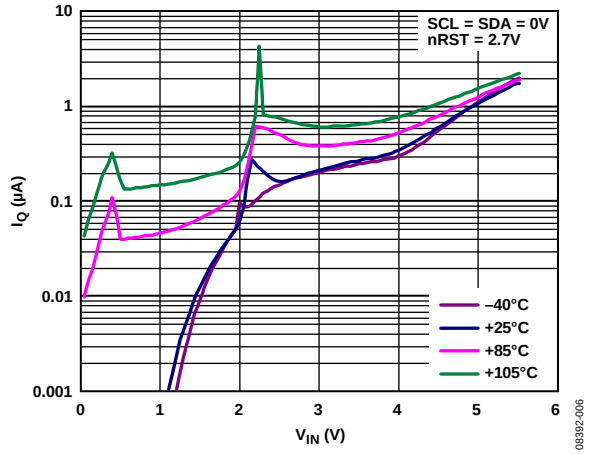


Figure 7. Typical Standby $I_Q$ vs. $V_{IN}$

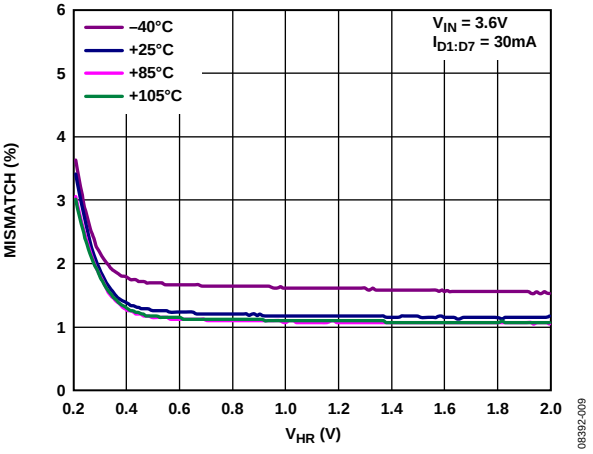


Figure 10. Typical Diode Matching vs. Current Sink Headroom Voltage ($V_{HR}$)

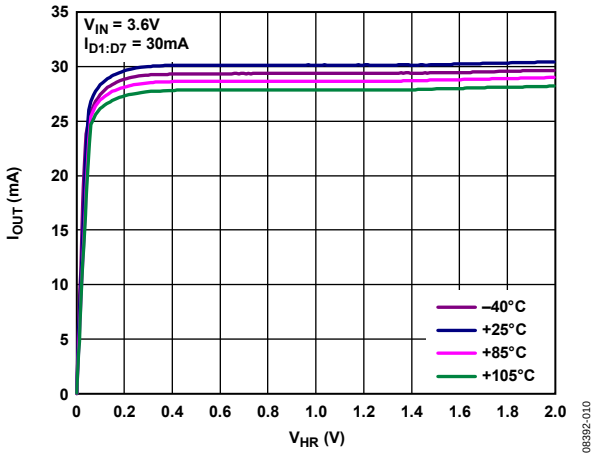


Figure 11. Typical Diode Current vs. Current Sink Headroom Voltage ($V_{HR}$)

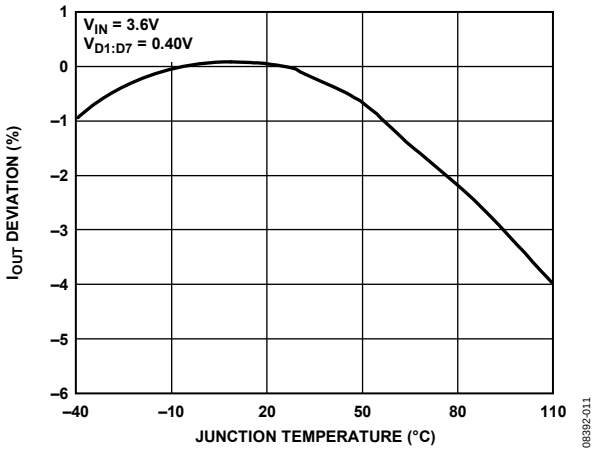


Figure 12. Typical Change In Diode Current vs. Temperature

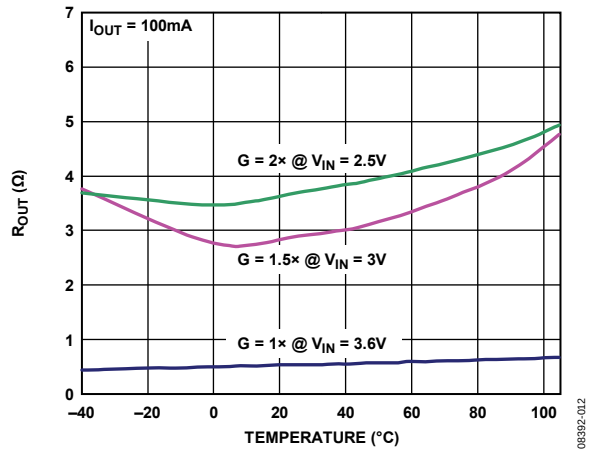


Figure 13. $R_{OUT}$ vs. Temperature

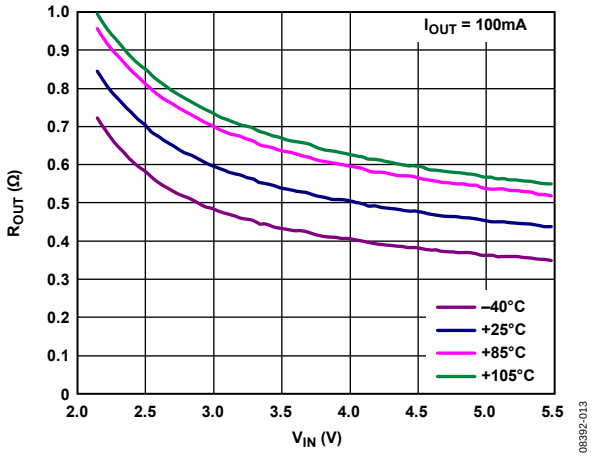


Figure 14. Typical $R_{OUT}$ ($G = 1\times$) vs. $V_{IN}$

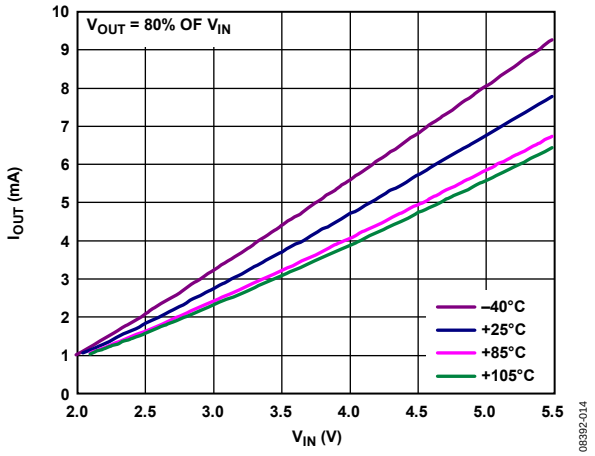


Figure 15. Typical Output Soft Start Current, $I_{SS}$

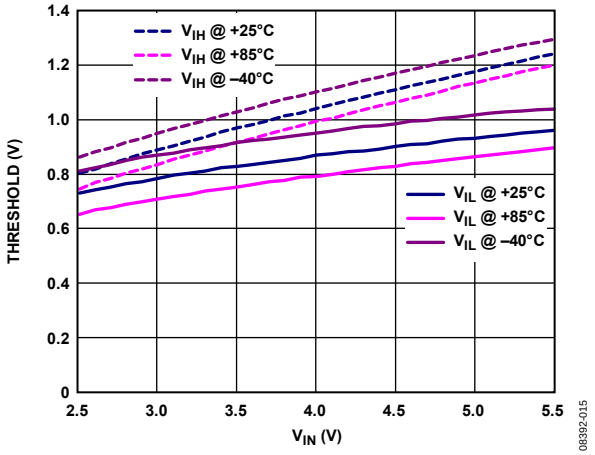


Figure 16. Typical $I^2C$ Thresholds, $V_{IH}$ and $V_{IL}$

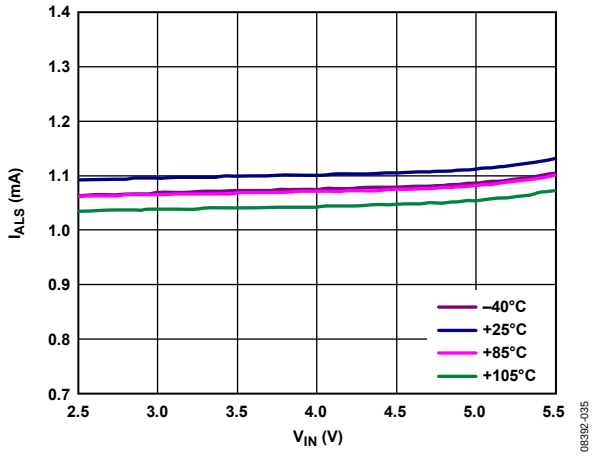


Figure 17. Typical ALS Current, $I_{ALS}$

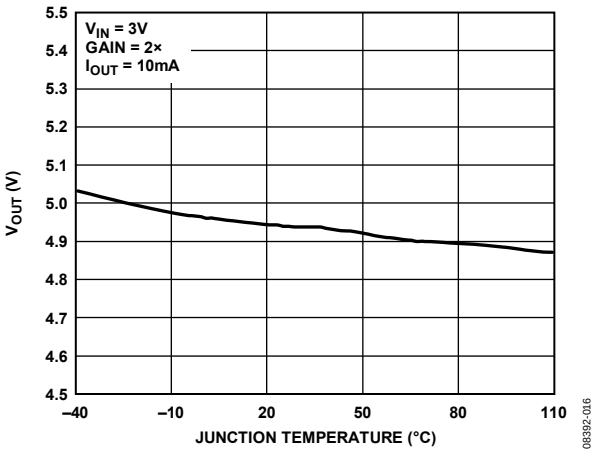


Figure 18. Typical Regulated Output Voltage ($V_{OUT(REG)}$)

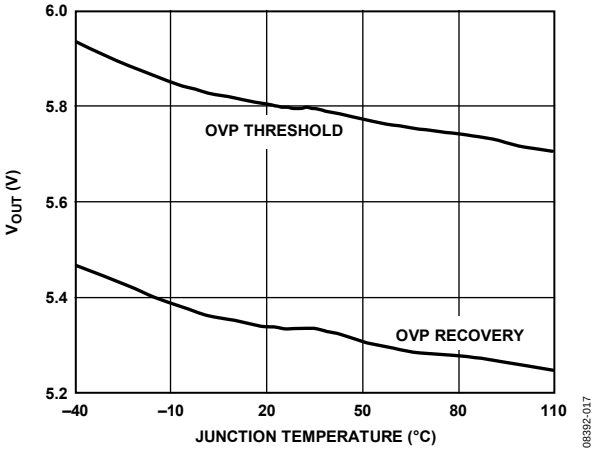


Figure 19. Typical Overvoltage Protection (OVP) Threshold

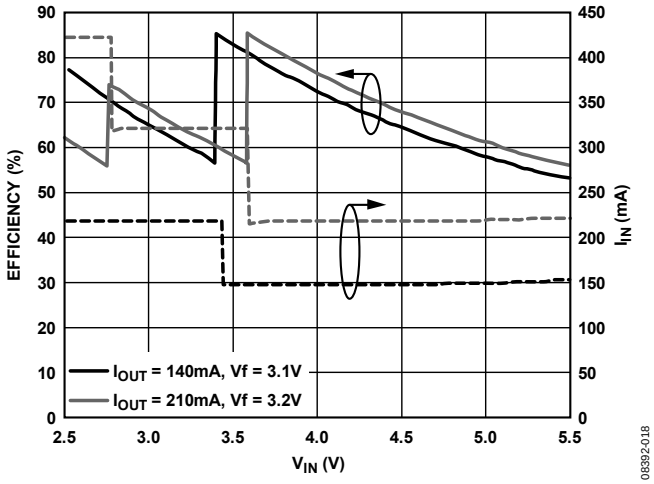


Figure 20. Typical Efficiency (Low Vf Diode)

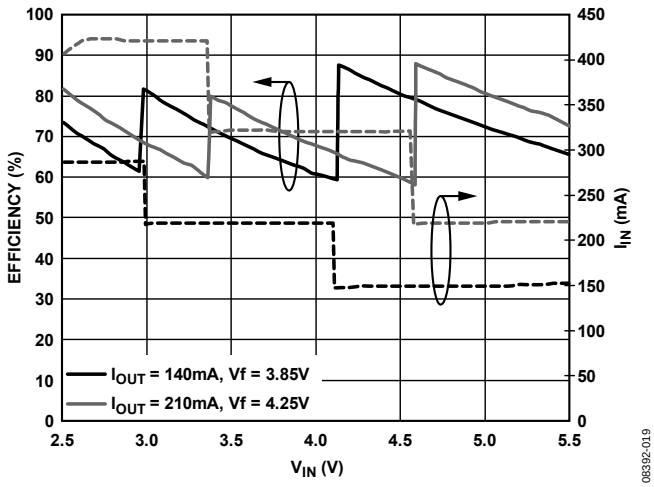


Figure 21. Typical Efficiency (High Vf Diode)

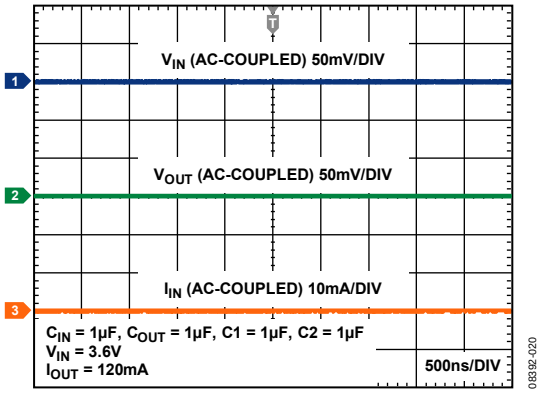


Figure 22. Typical Operating Waveforms, G = 1×

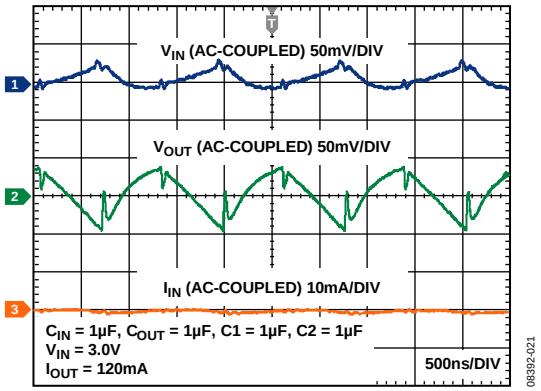


Figure 23. Typical Operating Waveforms, G = 1.5×

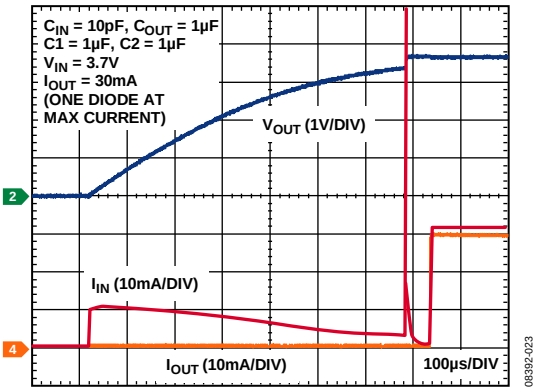


Figure 25. Typical Start-Up Waveform

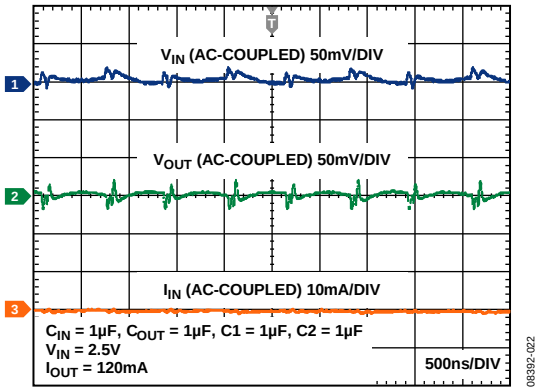


Figure 24. Typical Operating Waveforms, G = 2×

# THEORY OF OPERATION

The ADP8863 combines a powerful LED charge pump driver with independent control of up to seven LEDs. These LED drivers can sink up to 30 mA (typical) on six channels. The seventh LED can also be driven to 60 mA (typical). All LEDs can be individually programmed or combined into a group to operate backlight LEDs. A full set of safety features, including short-circuit, overvoltage, and overtemperature protection with input-to-output isolation, allows for a robust and safe design. The integrated soft start limits inrush currents at startup, restart attempts, and gain transitions.

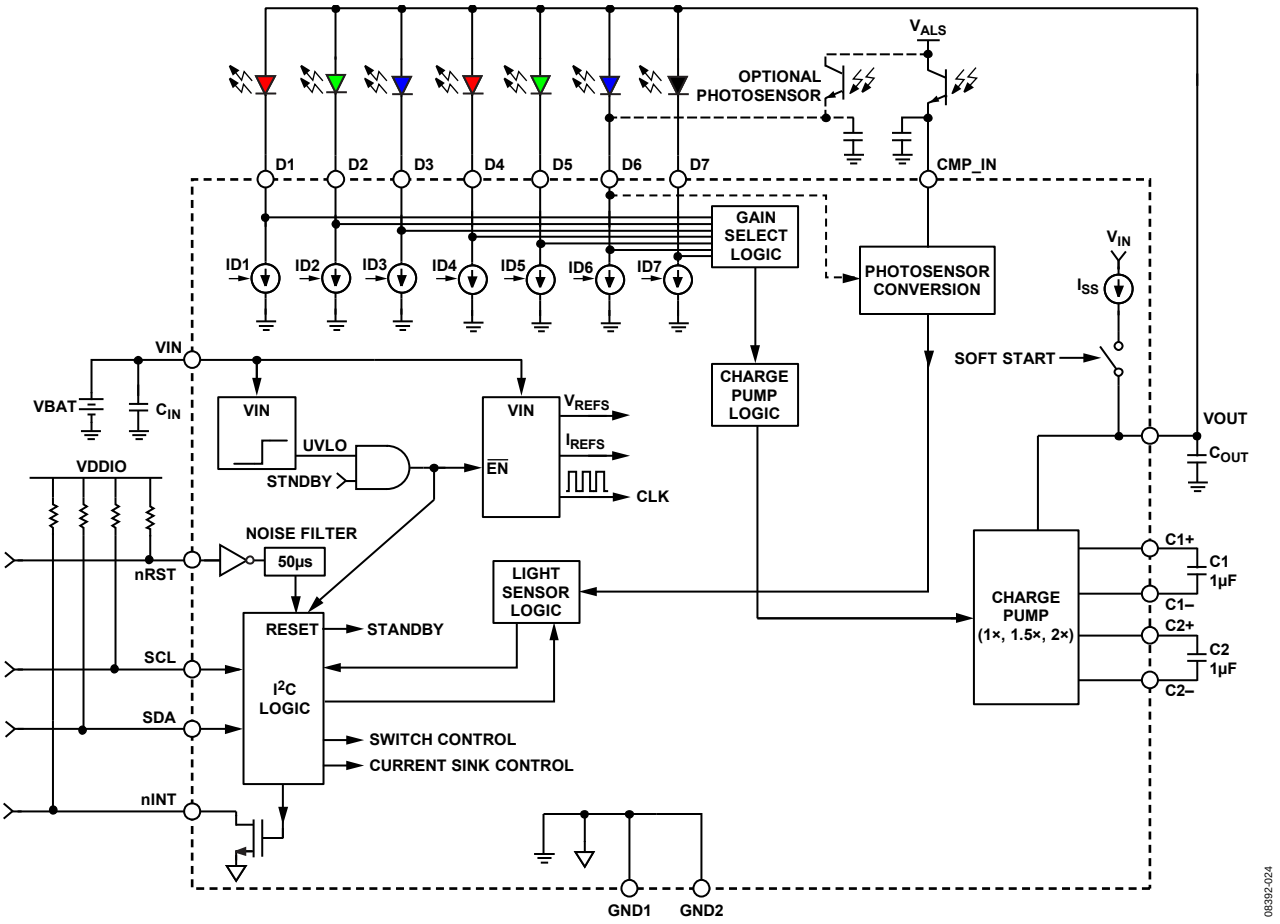


*Figure 26. Detailed Block Diagram*

## POWER STAGE

Because typical white LEDs require up to 4 V to drive them, some form of boosting is required over the typical variation in battery voltage. The ADP8863 accomplishes this with a high efficiency charge pump capable of producing a maximum $I_{OUT}$ of 240 mA over the entire input voltage range (2.5 V to 5.5 V). Charge pumps use the basic principle that a capacitor stores charge based on the voltage applied to it, as shown in the following equation:

$$Q = C \times V \quad (1)$$

By charging the capacitors in different configurations, the charge, and therefore the gain, can be optimized to deliver the voltage required to power the LEDs. Because a fixed charging and discharging combination must be used, only certain multiples of gain are available. The ADP8863 is capable of automatically optimizing the gain (G) from 1×, 1.5×, and 2×. These gains are accomplished with two capacitors (labeled C1 and C2 in Figure 26) and an internal switching network.

In G = 1× mode, the switches are configured to pass VIN directly to VOUT. In this mode, several switches are connected in parallel to minimize the resistive drop from input to output. In G = 1.5× and 2× modes, the switches alternatively charge from the battery and discharge into the output. For G = 1.5×, the capacitors are charged from $V_{IN}$ in series and are discharged to $V_{OUT}$ in parallel. For G = 2×, the capacitors are charged from $V_{IN}$ in parallel and are discharged to $V_{OUT}$ in parallel. In certain fault modes, the switches are opened and the output is physically isolated from the input.

### *Automatic Gain Selection*

Each LED that is driven requires a current source. The voltage on this current source must be greater than a minimum headroom voltage (200 mV typical) to maintain accurate current regulation. The gain is automatically selected based on the minimum voltage ($V_{DX}$) at all of the current sources. At startup, the device is placed into G = 1× mode and the output charges to $V_{IN}$. If any $V_{DX}$ level is less than the required headroom (200 mV), the gain is increased to the next step (G = 1.5×). A 100 µs delay is allowed for the output to stabilize prior to the next gain switching decision. If there remains insufficient current sink headroom, then the gain is increased again to 2×. Conversely, to optimize efficiency, it is not desirable for the output voltage to be too high. Therefore, the gain reduces when the headroom voltage is great enough. This point (labeled $V_{DMAX}$ in Figure 27) is internally calculated to ensure that the lower gain still results in ample headroom for all the current sinks. The entire cycle is illustrated in Figure 27.

Note that the gain selection criteria apply only to active current sources. If current sources have been deactivated through an $I^2C$ command (for example, only five LEDs are used), then the voltages on the deactivated current sources are ignored.

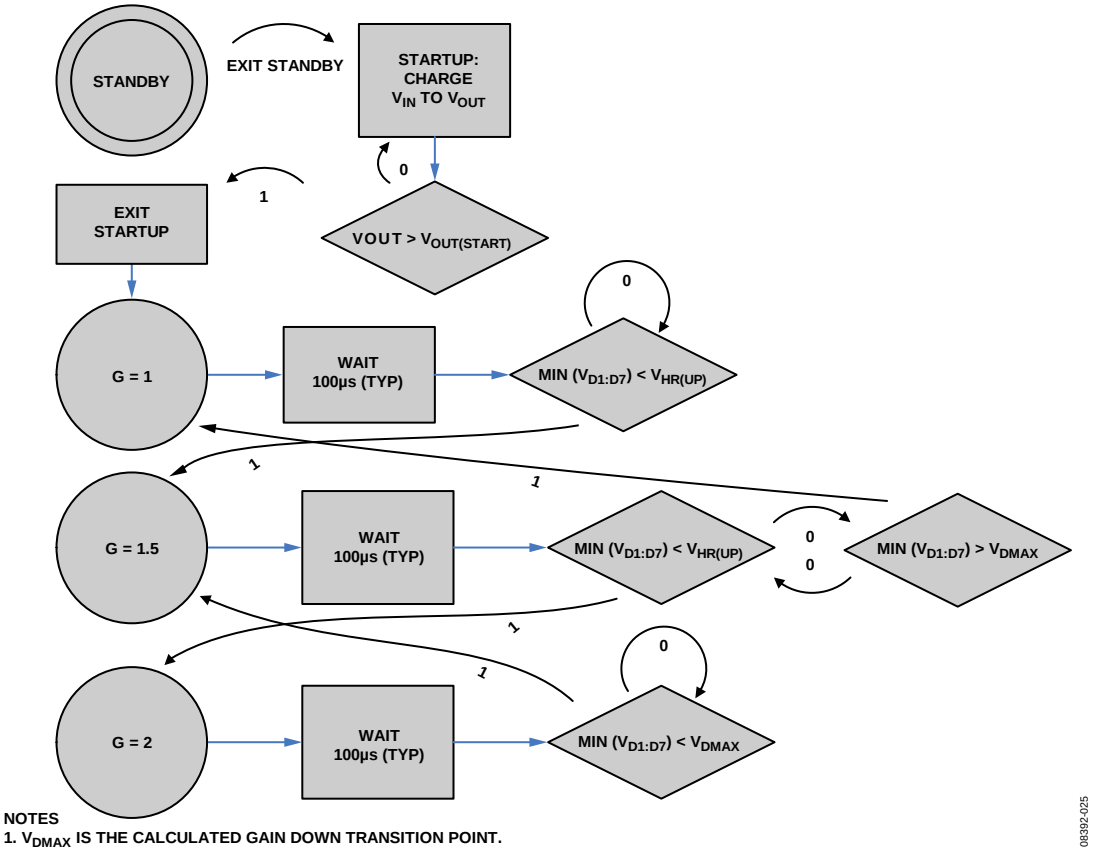


*Figure 27. State Diagram for Automatic Gain Selection*

### Soft Start Feature

At startup (either from UVLO activation or fault/standby recovery), the output is first charged by $I_{SS}$ (3.75 mA typical) until it reaches about 92% of $V_{IN}$. This soft start feature reduces the inrush current that is otherwise present when the output capacitance is initially charged to $V_{IN}$. When this point is reached, the controller enters G = 1× mode. If the output voltage is not sufficient, then the automatic gain selection determines the optimal point as defined in the Automatic Gain Selection section.

## OPERATING MODES

There are four different operating modes: active, standby, shutdown, and reset.

### Active Mode

In active mode, all circuits are powered up and in a fully operational state. This mode is entered when Bit nSTBY (in Register MDCR) is set to 1.

### Standby Mode

Standby mode disables all circuitry except for the I²C receivers. Current consumption is reduced to less than 1 µA. This mode is entered when the nSTBY bit is set to 0 or when the nRST pin is held low for more than 100 µs (maximum). When standby is exited, a soft start sequence is performed.

### Shutdown Mode

Shutdown mode disables all circuitry, including the I²C receivers. Shutdown occurs when $V_{IN}$ is below the undervoltage thresholds. When $V_{IN}$ rises above $V_{IN(START)}$ (2.05 V typical), all registers are reset and the part is placed into standby mode.

### Reset Mode

In reset mode, all registers are set to their default values and the part is placed into standby. There are two ways to reset the part: by power-on reset (POR) or using the nRST pin. POR is activated any time that the part exits shutdown mode. After a POR sequence is complete, the part automatically enters standby mode.

After startup, the part can be reset by pulling the nRST pin low. As long as the nRST pin is low, the part is held in a standby state, but no I²C commands are acknowledged (all registers are kept at their default values). After releasing the nRST pin, all registers remain at their default values, and the part remains in standby; however, the part does accept I²C commands.

The nRST pin has a 50 µs (typical) noise filter to prevent inadvertent activation of the reset function. The nRST pin must be held low for this entire time to activate reset.

The operating modes function according to the timing diagram in Figure 28.

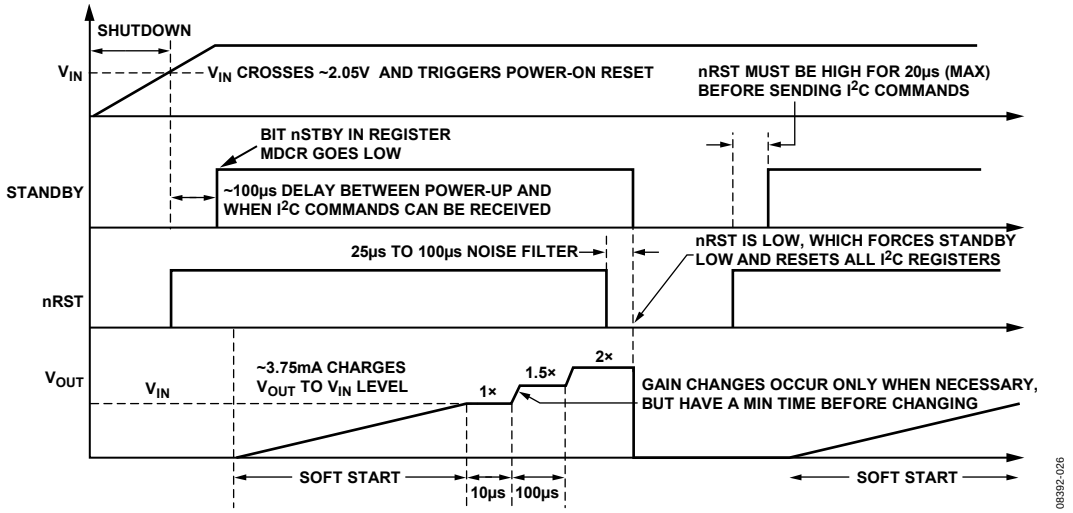


*Figure 28. Typical Timing Diagram*

## LED GROUPINGS

Each LED can respond individually or be grouped together into the backlight controls. By default, all LEDs are set to be part of the backlight. This is changed by setting Bits[6:0] in Register 0x05. LEDs that are set up as independent sinks can be enabled individually in Register 0x10. They can also all be enabled simultaneously via the SIS_EN bit in Register 0x01. Any LEDs configured for the backlight can only be enabled via the BL_EN bit in Register 0x01.

## LED CURRENT SETTINGS

Any of the LED outputs (Pin D1 to Pin D7) can be used to drive any color of LED at 0 mA to 30 mA, provided that the LED's Vf is less than 4.1 V. Additionally, the D7 sink can regulate up to 60 mA. The current settings are determined by a 7-bit code programmed by the user into Register 0x14 through Register 0x1A (for the independent sinks) and Register 0x09 to Register 0x0E (for the backlight sinks). The 7-bit resolution allows the user to set the LED to one of 128 different levels.

The ADP8863 can implement two distinct algorithms to achieve a linear or a nonlinear relationship between input code and diode output current. The law and SC_LAW bits in Register 0x04 and Register 0x0F, respectively, are used to change between these algorithms.

By default, the ADP8863 uses a linear algorithm (law and SC_LAW = 00), where the LED current increases linearly for a corresponding increase in input code. LED current (in milliamperes) is determined by the following equation:

$$LED\ Current\ (\text{mA}) = Code \times (Full\text{-}Scale\ Current/127) \quad (2)$$

where:
*Code* is the input code programmed by the user.
*Full-Scale Current* is the maximum sink current allowed per LED (typically 30 mA).

The ADP8863 can also implement a nonlinear (square approximation) relationship between input code and LED current. In this case (law and SC_LAW = 01, 10, or 11), the LED current (in milliamperes) is determined by the following equation:

$$LED\ Current\ (\text{mA}) = \left( Code \times \frac{\sqrt{Full - Scale\ Current}}{127} \right)^2 \quad (3)$$

Figure 29 shows the LED current level vs. input code for both the linear and square law algorithms.

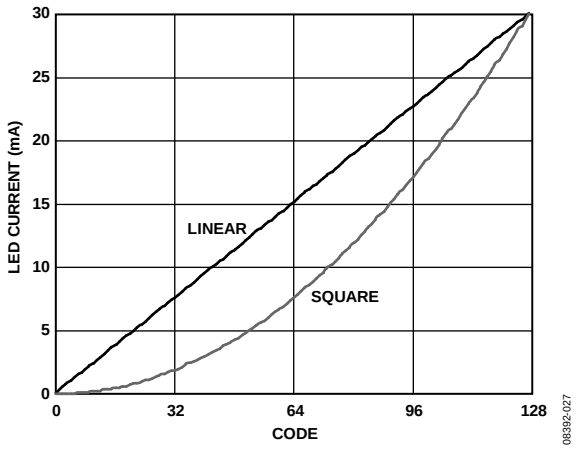


*Figure 29. LED Current vs. Input Code*

## AUTOMATED FADE IN AND FADE OUT

The LED drivers are easily configured for automated fade in and fade out. Sixteen fade in and fade out rates can be selected via the I²C interface. Fade in and fade out rates range from 0.0 sec to 5.5 sec (per full-scale current, either 30 mA or 60 mA). The backlight LEDs have separate fade in and fade out time controls from the independent sink LEDs.

**Table 5. Available Fade In and Fade Out Rates**

| Code | Fade Rate (in sec per Full-Scale Current) |
|---|---|
| 0000 | 0.0 (disabled) |
| 0001 | 0.3 |
| 0010 | 0.6 |
| 0011 | 0.9 |
| 0100 | 1.2 |
| 0101 | 1.5 |
| 0110 | 1.8 |
| 0111 | 2.1 |
| 1000 | 2.4 |
| 1001 | 2.7 |
| 1010 | 3.0 |
| 1011 | 3.5 |
| 1100 | 4.0 |
| 1101 | 4.5 |
| 1110 | 5.0 |
| 1111 | 5.5 |

The fade profile is based on the transfer law selected (linear, square, Cubic 10, or Cubic 11) and the delta between the actual current and the target current. Smaller changes in current reduce the fade time. For linear and square law fades, the fade time is given by

$$Fade\ Time = Fade\ Rate \times (Code/127) \quad (4)$$

where the *Fade Rate* is shown in Table 5.

The Cubic 10 and Cubic 11 laws also use the square law LED currents derived from Equation 3; however, the time between each step is varied to produce a steeper slope at higher currents and a shallower slope at lower currents (see Figure 30).

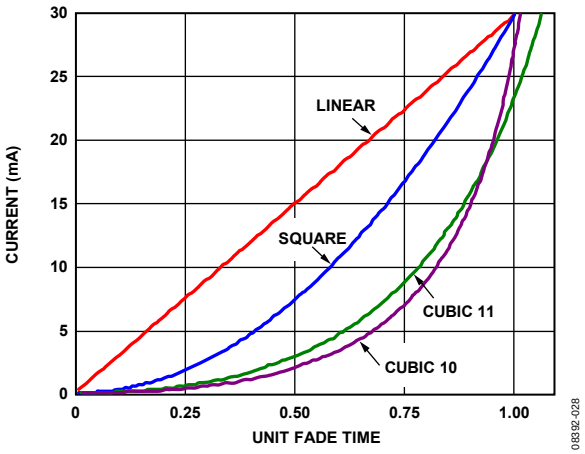


*Figure 30. Comparison of the Dimming Transfers Laws*

Each LED can be enabled independently and has its own current level, but all LEDs share the same fade in rates, fade out rates, and fade law.

## INDEPENDENT SINK CONTROL

Each of the seven LEDs can be configured (in Register 0x05) to operate as either part of the backlight or to operate as an independent sink current (ISC). Each ISC can be enabled independently and has its own current level. All ISCs share the same fade in rates, fade out rates, and fade law.

The ISCs have additional timers to facilitate blinking functions. A shared on timer (SCON) in conjunction with the off timer of each ISC (SC1OFF, SC2OFF, SC3OFF, SC4OFF, SC5OFF, SC6OFF, and SC7OFF) allows the LED current sinks to be configured in various blinking modes. The on timer can be set to one of four different settings: 0.2 sec, 0.6 sec, 0.8 sec, or 1.2 sec. The off timers have four different settings: disabled, 0.6 sec, 1.2 sec, and 1.8 sec. Blink mode is activated by setting the off timers to any setting other than disabled.

Program all fade, on, and off timers before enabling any of the LED current sinks. If ISCx is on during a blink cycle and SCx_EN is cleared, the LED turns off (or fades to off if fade out is enabled). If ISCx is off during a blink cycle and SCx_EN is cleared, it stays off.

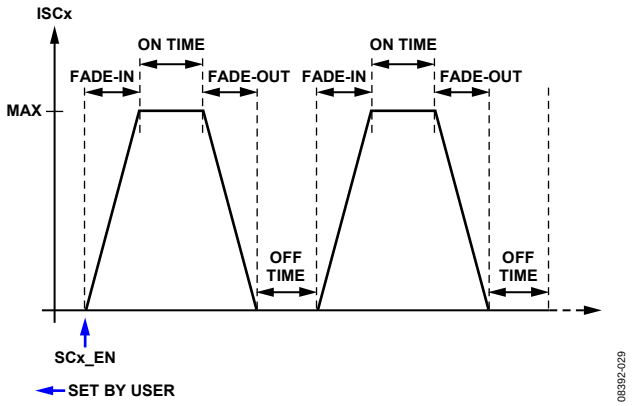


*Figure 31. Independent Sink Blink Mode with Fading*

## RGB COLOR GENERATION

The ADP8863 is easily programmed to generate any color with an RGB LED. To configure this feature, connect each LED in a standard RGB diode to a separate driver on the ADP8863. Because each channel can be programmed for a different current level, setting the currents for all three LEDs generates the desired color. To set the current levels, use a simple RGB color selector (see Figure 32).

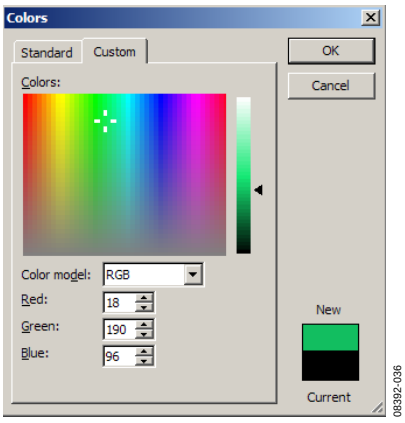


*Figure 32. Standard RGB Color Generator*

The example in Figure 32 shows a color of green, which is generated with a red content of 18 (out of 255), a green content of 190, and a blue content of 96. All numbers are out of a maximum of 255. Thus, the percentage of red is 7.1%, the percentage of green is 74.5%, and the percentage of blue is 37.6%. To generate the color with the ADP8863, scale this value to each of the current drivers.

## AUTOMATED RGB COLOR FADES

The ADP8863 is easily programmed to cycle through RGB generated colors. This can be either a repeating or a random pattern of one color fading into the other. To execute this cycle autonomously, set up the RGB LEDs as described in the RGB Color Generation section and program the on, off, fading times, and current intensities. Adjusting the fading time in particular can create any pattern from a fast, striking effect to a soothing slow color change.

## BACKLIGHT OPERATING LEVELS

Backlight brightness control operates at three distinct levels: daylight (L1), office (L2), and dark (L3). The BLV bits in Register 0x04 control the specific level at which the backlight operates. These bits can be changed manually or, if in automatic mode (CMP_AUTOEN is set high in Register 0x01), by the ambient light sensor (see the Ambient Light Sensing section).

By default, the backlight operates at daylight level (BLV = 00), where the maximum brightness is set using Register 0x09 (BLMX1). A daylight dim setting can also be set using Register 0x0A (BLDM1). When operating at office level (BLV = 01), the backlight maximum and dim brightness settings are set using Register 0x0B (BLMX2) and Register 0x0C (BLDM2). When operating at the dark level (BLV = 10), the backlight maximum and dim brightness settings are set using Register 0x0D (BLMX3) and Register 0x0E (BLDM3).

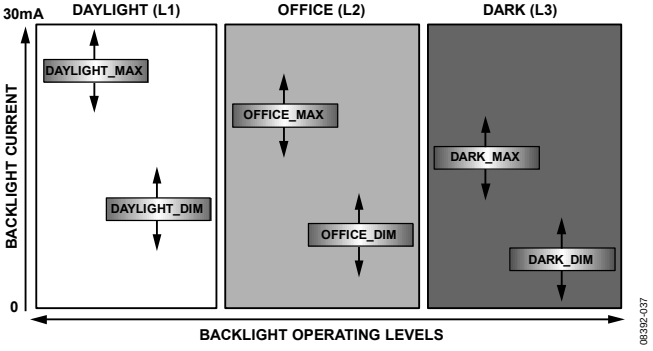


*Figure 33. Backlight Operating Levels*

## BACKLIGHT TURN ON/TURN OFF/DIM

With the device in active mode (nSTBY = 1), the backlight can be turned on using the BL_EN bit in Register 0x01. Before turning on the backlight, select the level (daylight (L1), office (L2), or dark (L3)) to operate in and ensure that maximum and dim settings are programmed for that level. The backlight turns on when BL_EN = 1. The backlight turns off when BL_EN = 0.

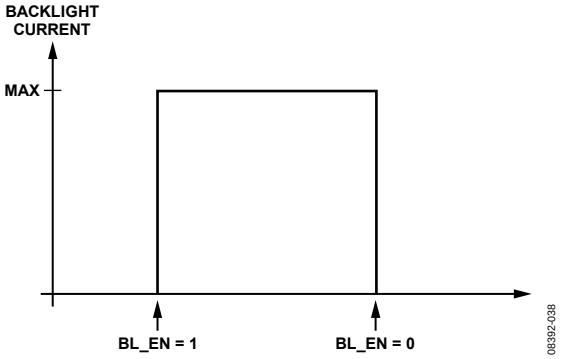


*Figure 34. Backlight Turn On/Turn Off*

While the backlight is on (BL_EN = 1), the user can change to the dim setting by programming DIM_EN = 1 in Register 0x01. If DIM_EN = 0, the backlight reverts to its maximum setting.

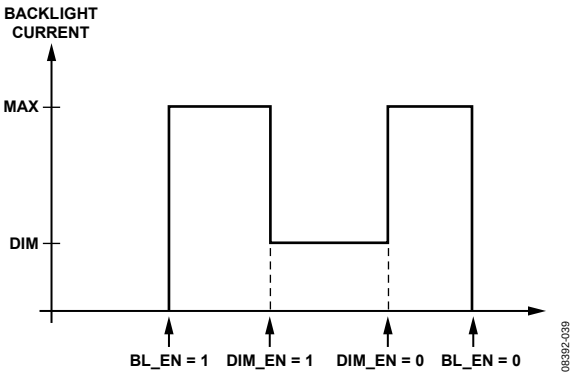


*Figure 35. Backlight Turn On/Dim/Turn Off*

The maximum and dim settings can be set from 0 mA to 30 mA; therefore, it is possible to program a dim setting that is greater than a maximum setting. For normal expected operation, ensure that the dim setting is programmed to be less than the maximum setting.

## AUTOMATIC DIM AND TURN OFF TIMERS

The user can program the backlight to dim automatically by using the DIMT bits in Register 0x07. The dim timer has 127 settings ranging from 1 sec to 127 sec. Program the dim timer (DIMT) before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the dim timer starts counting. When the dim timer expires, the internal state machine sets DIM_EN = 1, and the backlight enters its dim setting.

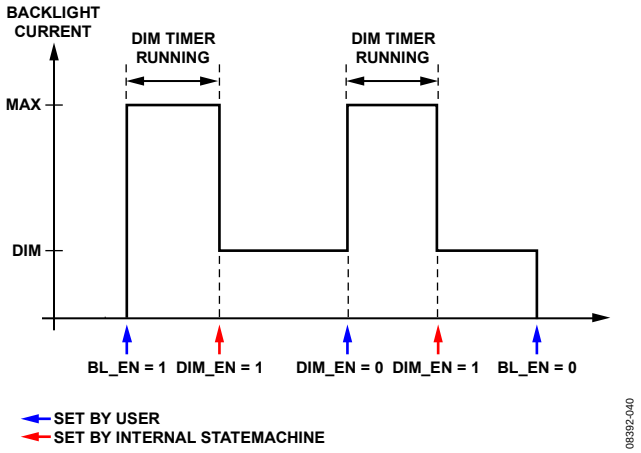


*Figure 36. Dim Timer*

If the user clears the DIM_EN bit, the backlight reverts to its maximum setting and the dim timer begins counting again. When the dim timer expires, the internal state machine again sets DIM_EN = 1, and the backlight enters its dim setting. The backlight can be turned off at any point during the dim timer countdown by clearing BL_EN.

The user can also program the backlight to turn off automatically by using the OFFT bits in Register 0x06. The off timer has 127 settings ranging from 1 sec to 127 sec. Program the off timer (OFFT) before turning on the backlight. If BL_EN = 1, the backlight turns on to its maximum setting and the off timer

starts counting. When the off timer expires, the internal state machine clears the BL_EN bit, and the backlight turns off.

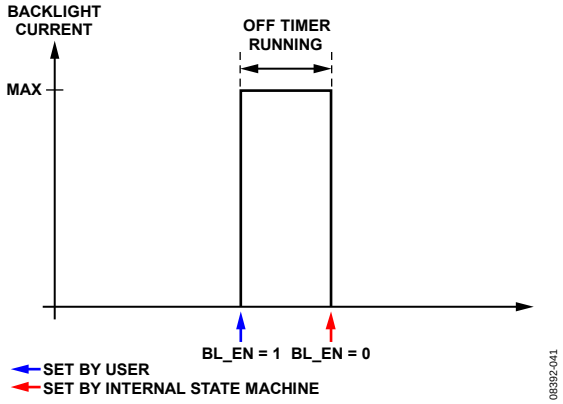


*Figure 37. Off Timer*

The backlight can be turned off at any point during the off timer countdown by clearing BL_EN.

The dim timer and off timer can be used together for sequential maximum-to-dim-to-off functionality. With both the dim and off timers programmed, and BL_EN asserted, the backlight turns on to its maximum setting, and when the dim timer expires, the backlight changes to its dim setting. When the off timer expires, the backlight turns off.

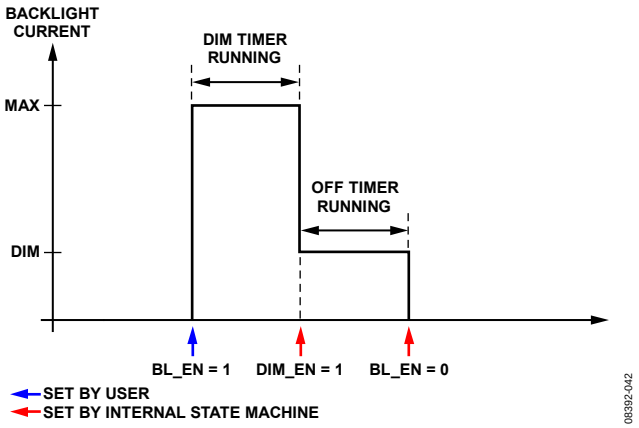


*Figure 38. Dim and Off Timers Used Together*

## FADE OVERRIDE

A fade override feature (FOVR in Register CFGR (0x04)) enables the host to override the preprogrammed fade in or fade out settings. If FOVR is set and the backlight is enabled in the middle of a fade out process, the backlight instantly (within approximately 100 ms) returns to its maximum setting. Alternatively, if the backlight is fading in, reasserting BL_EN overrides the programmed fade in time, and the backlight instantly goes to its final fade value. This is useful for situations in which a key is pressed during a fade sequence. However, if FOVR is cleared and the backlight is enabled in the middle of a fade process, the backlight gradually brightens from where it was interrupted (it does not go down to 0 and then comes back on).

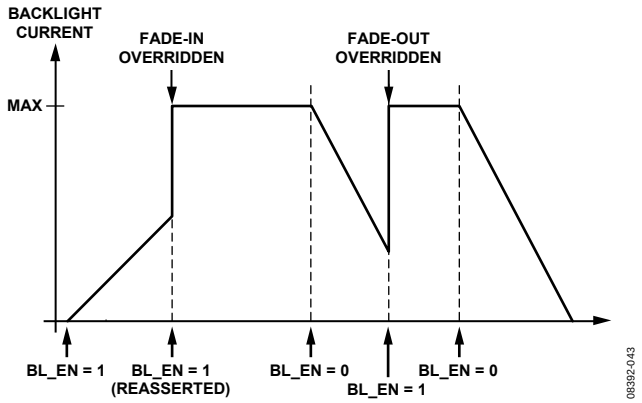


*Figure 39. Fade Override Function (FOVR Is High)*

## AMBIENT LIGHT SENSING

The ADP8863 integrates two ambient light sensing comparators. One of the ambient light sensing comparator pins (CMP_IN) is always available. The second pin (D6) has an ambient light sensor comparator (CMP_IN2) that can be activated rather than connecting an LED to D6. Activating the CMP_IN2 function of the pin is accomplished through the CMP2_SEL bit in Register CFGR. Therefore, when the CMP2_SEL bit is set to 0, Pin D6 is programmed as a current sink. When the CMP2_SEL bit is set to 1, Pin D6 becomes the input for a second phototransistor.

These comparators have two programmable trip points (L2 and L3) that select one of the three backlight operation modes (daylight, office, and dark) based on the ambient lighting conditions.

The L3 comparator controls the dark-to-office mode transition. The L2 comparator controls the office-to-daylight transition (see Figure 40). The currents for the different lighting modes are defined in the BLMXx and BLDMx registers (see the Backlight Operating Levels section).

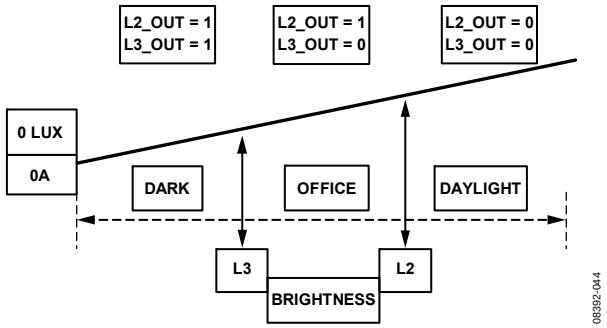


*Figure 40. Light Sensor Modes Based on the Detected Ambient Light Level*

Each light sensor comparator uses an external capacitor together with an internal reference current source to form an analog-to-digital converter (ADC) that samples the output of the external photosensor. The ADC result is fed into two programmable trip comparators. The ADC has an input range of 0 µA to 1080 µA (typical).

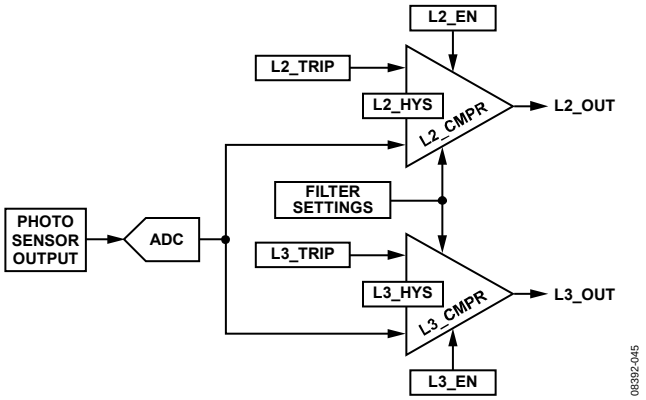


*Figure 41. Ambient Light Sensing and Trip Comparators*

The L2 comparator, L2_CMPR, detects when the photosensor output has dropped below the programmable L2_TRP point (Register 0x1D). If this event occurs, then the L2_OUT status signal is set. L2_CMPR contains programmable hysteresis, meaning that the photosensor output must rise above L2_TRP + L2_HYS before L2_OUT clears. L2_CMPR is enabled via the L2_EN bit. The L2_TRP and L2_HYS values of L2_CMPR can be set between 0 µA and 1080 µA (typical) in steps of 4.3 µA (typical).

The L3 comparator, L3_CMPR, detects when the photosensor output drops below the programmable L3_TRP point (Register 0x1F). If this event occurs, the L3_OUT status signal is set. L3_CMPR contains programmable hysteresis, meaning that the photosensor output must rise above L3_TRP + L3_HYS before L3_OUT clears. L3_CMPR is enabled via the L3_EN bit. The L3_TRP and L3_HYS values of L3_CMPR can be set between 0 µA and 137.7 µA (typical) in steps of 0.54 µA (typical).

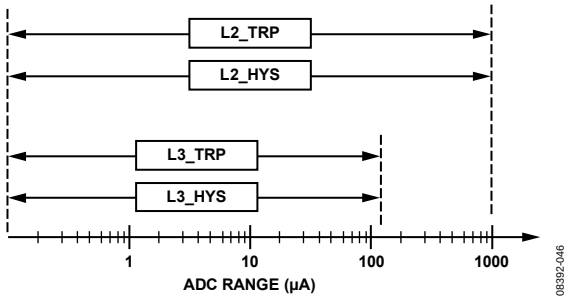


*Figure 42. Comparator Ranges*

Note that the full-scale value of the L2_TRP and L2_HYS registers is 250 (decimal). Therefore, if the value of L2_TRP + L2_HYS exceeds 250, the comparator output is unable to deassert. For example, if L2_TRP is set to 204 (80% of the full-scale value, or approximately 0.80 × 1080 µA = 864 µA), then L2_HYS must be set to less than 46 (250 − 204 = 46). If it is not, then L2_HYS + L2_TRP exceeds 250 and the L2_CMPR comparator is never allowed to go low.

When both phototransistors are enabled and programmed in automatic mode (through Bit CMP_AUTOEN in Register 0x01), the user application must determine which comparator outputs to use, by selecting Bit SEL_AB in Register 0x04 for automatic light sensing transitions. For example, the user software may select the comparator of the phototransistor that is exposed to higher light intensity to control the transition between the programmed backlight intensity levels.

The L2_CMPR and L3_CMPR comparators can be enabled independently of each other, or they can operate simultaneously. A single conversion from each ADC takes 80 ms (typical). When CMP_AUTOEN is set for automatic backlight adjustment (see the Automatic Backlight Adjustment section), the ADC and comparators run continuously. If the backlight is disabled and at least one independent sink is enabled, it is possible to use the light sensor comparators in a single-shot mode. A single-shot read of the photocomparators is performed by setting the FORCE_RD bit in Register 0x1B. After the single-shot measurement is completed, the internal state machine clears the FORCE_RD bit.

The interrupt flags (CMP_INT and CMP_INT2) can be used to notify the system when either L2 or L3 changes state. See the Interrupts section for more information.

## AUTOMATIC BACKLIGHT ADJUSTMENT

The ambient light sensor comparators can automatically transition the backlight between one of its three operating levels. To enable this mode, set the CMP_AUTOEN bit in Register 0x01.

When $I^2C$ selection is enabled, the internal state machine takes control of the BLV bits and changes them based on the L2_OUT and L3_OUT status bits. When L2_OUT is set high, it indicates that the ambient light conditions have dropped below the L2_TRP point and that the backlight should move to its office (L2) level. When L3_OUT is set high, it indicates that ambient light conditions have dropped below the L3_TRP point and that the backlight should move to its dark (L3) level. Table 6 shows the relationship between backlight operation and the ambient light sensor comparator outputs.

The L3_OUT status bit has greater priority; therefore, if L3_OUT is set, the backlight operates at L3 (dark) even if L2_OUT is also set.

Filter times from 80 ms to 10 sec can be programmed for the comparators (Register 0x1B and Register 0x1C) before they change state.

**Table 6. Comparator Output Truth Table**

| CMP_AUTOEN | L3_OUT | L2_OUT | Backlight Operation |
|---|---|---|---|
| 0 | X[1] | X[1] | BLV can be manually set by the user |
| 1 | 0 | 0 | BLV = 00, backlight operates at L1 (daylight) |
| 1 | 0 | 1 | BLV = 01, backlight operates at L2 (office) |
| 1 | 1 | X[1] | BLV = 10, backlight operates at L3 (dark) |

[1] X is the don't care bit.

## USING THE ADP8863 TO DRIVE ADDITIONAL LEDS

In some situations, it may be desirable to drive more than seven LEDs. This can be done in one of two ways: paralleling LEDs using ballast resistors, or using the ADP8863 to power additional LED drivers.

### *Ballast Resistors*

In the first method, multiple LEDs can be attached to any one LED driver with the use of ballast resistors.

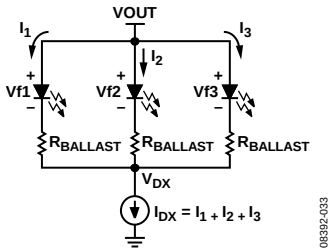


*Figure 43. Ballast Resistor Arrangement*

Ballast resistors attempt to compensate for the forward voltage (Vf) mismatch inherent in any parallel combination of LEDs. The choice of a ballasting resistor is a trade-off between the efficiency and the current matching of the LEDs in parallel. Smaller ballast resistors give better efficiency. Larger ballast resistors gives better current matching, because the resistor balances out the current differences for a voltage drop. The relationship is summarized with the following:

$$R_{BALLAST} \approx \frac{\Delta Vf}{\Delta I} \quad (5)$$

where:
$\Delta Vf$ is the difference between the maximum Vf and the minimum Vf of the LEDs in parallel.
$\Delta I$ is the difference between the parallel LED currents.

The addition of the ballast resistor brings the effective Vf of the LED to

$$Vf(eff) = Vf(LED) + I_{LED} \times R_{BALLAST} \quad (6)$$

The $I_{LED} \times R_{BALLAST}$ term forces the charge pump to work a little harder for this additional voltage drop. Furthermore, for guaranteed operation with the ADP8863, the total Vf(eff) should never exceed $V_{OUT(REG)} - V_{HR(UP)}$ (see Table 1).

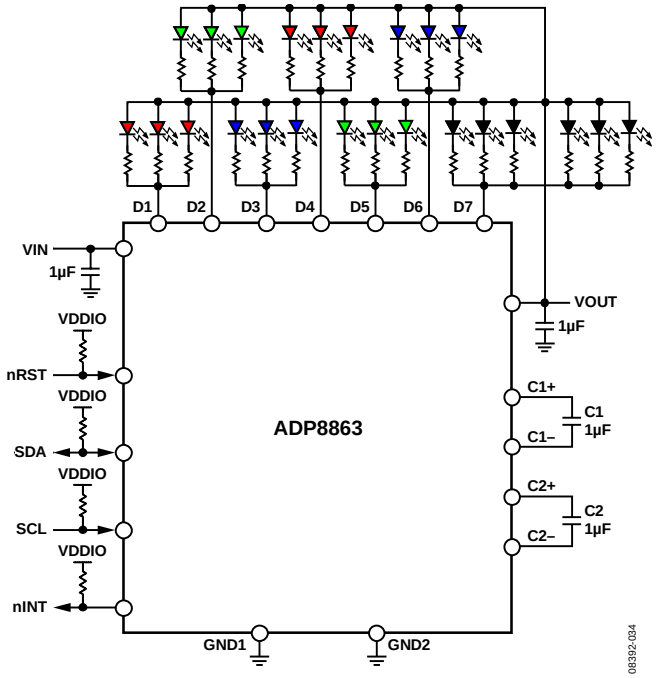


*Figure 44. Powering Additional LEDs with Ballast Resistors*

### *Adding Additional Parallel Sinks*

The ballast resistor's compromises of efficiency and matching are not suitable for many applications. Therefore, another option is to use the ADP8863 charge pump to power additional current sinks. First, the charge pump must be optimized for this option by setting the GDWN_DIS bit in Register 0x01, which prevents the charge pump from switching back down in gain, and thus stabilizes it against the unknown loads that the additional current sinks present.

To use the sinks, turn the ADP8863 charge pump on before activating the additional sinks. If the additional sinks are activated first, the ADP8863 soft start may not complete.

The ADP8863 can be set up with an ADP8860 or ADP8861. An example using the ADP8861 is shown in Figure 45.

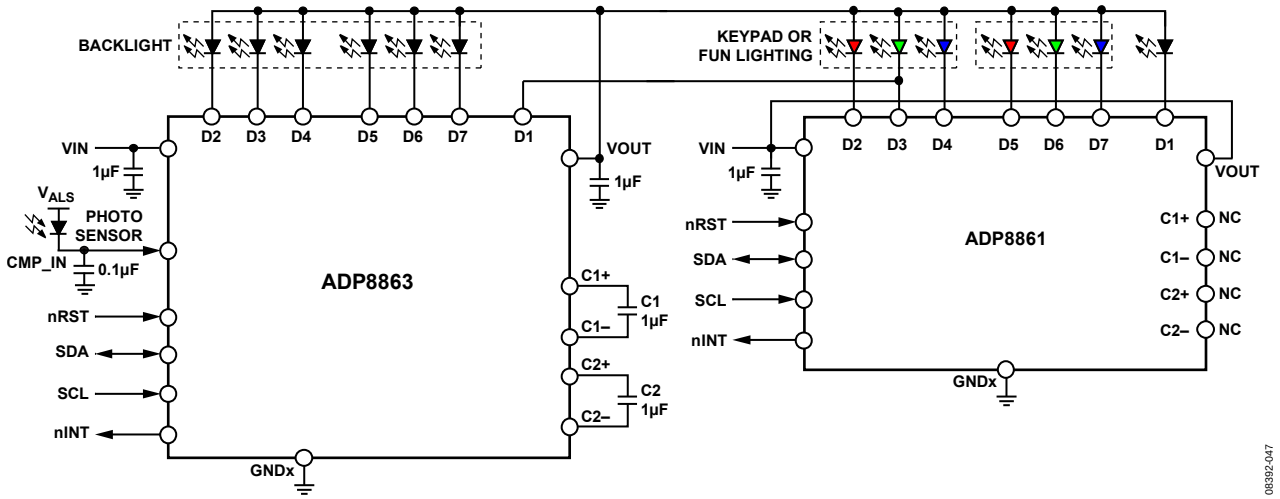


*Figure 45. Connecting the ADP8863 to an ADP8861 to Power More LEDs*

## OPERATING LEDS FROM ALTERNATIVE SUPPLIES

For some applications, it is advantageous to operate the LEDs from a voltage source other than the ADP8863 charge pump output. For example, it may be possible to operate a red LED over the entire battery voltage range without any charge pump boosting. For a charge pump,

$$I_{IN} = Gain \times I_{OUT} \quad (7)$$

Therefore, operating the red LEDs directly from the battery removes output current of the red LEDs from the charge pump draw. This in turn reduces the total input current by (Gain − 1) × $I_{OUT(red)}$.

However, care must be taken when selecting LEDs to operate from a different voltage input. Specifically, the voltage source must at least be able to support the maximum forward voltage (Vf) of the LED plus the maximum $V_{HR(UP)}$ (276 mV, given in Table 1). Additionally, operating an LED from an independent voltage source may interfere with the ADP8863's gain selection algorithm. This algorithm selects the optimal gain for the charge pump based on all seven diodes. By operating one or more of the diodes from another supply, the algorithm may not switch the gain back down to a lower state until the LEDs are disabled or the part enters standby.

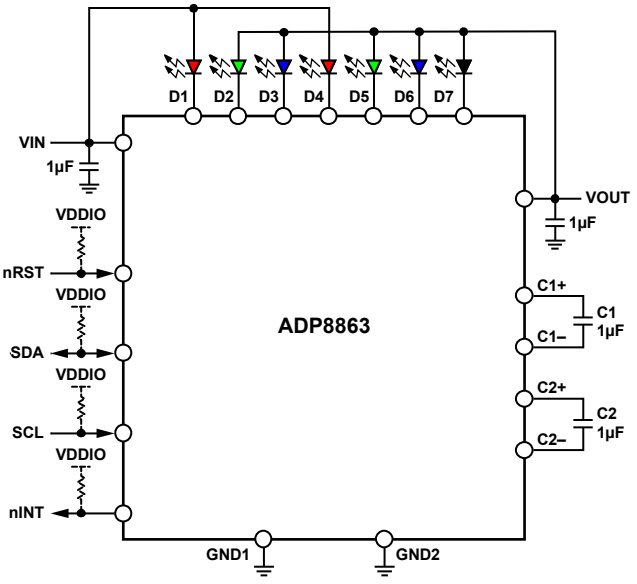


*Figure 46. Alternate Schematic for Low Vf LEDs*

## SHORT-CIRCUIT PROTECTION MODE

The ADP8863 can protect against short circuits on the output (VOUT). Short-circuit protection (SCP) is activated at the point when VOUT < 55% of $V_{IN}$. Note that SCP sensing is disabled during both startup and restart attempts (fault recovery). SCP sensing is reenabled 4 ms (typical) after activation. During a short-circuit fault, the device enters a low current consumption state and an interrupt flag is set. The device can be restarted at any time after receiving a short-circuit fault by rewriting nSTBY = 1. It then repeats another complete soft start sequence. Note that the value of the output capacitance ($C_{OUT}$) should be small enough to allow VOUT to reach approximately 55% (typical) of $V_{IN}$ within the 4 ms (typical) time. If $C_{OUT}$ is too large, the device inadvertently enters short-circuit protection.

## OVERVOLTAGE PROTECTION

Overvoltage protection (OVP) is implemented on the output. There are two types of overvoltage events: normal (no fault) and abnormal (from a fault or sudden load change).

### *Normal Overvoltage*

In a normal (no fault) overvoltage, the output voltage approaches $V_{OUT(REG)}$ (4.9 V typical) during normal operation. This is not caused by a fault or load change, but is simply a consequence of the input voltage times the gain reaching the same level as the clamped output voltage ($V_{OUT(REG)}$). To prevent this type of overvoltage, the ADP8863 detects when the output voltage rises to $V_{OUT(REG)}$. It then increases the effective $R_{OUT}$ of the gain stage to reduce the voltage that is delivered. This effectively regulates $V_{OUT}$ to $V_{OUT(REG)}$; however, there is a limit to the effect that this system can have on regulating $V_{OUT}$. It is designed only for normal operation and it is not intended to protect against faults or sudden load changes. When the output voltage is regulated to $V_{OUT(REG)}$, no interrupt is set and the operation is transparent to the LEDs and the overall application.

### *Abnormal Overvoltage*

Because of the open-loop behavior of the charge pump as well as how the gain transitions are computed, a sudden load change or fault can abnormally force $V_{OUT}$ beyond 6 V. This causes an abnormal overvoltage situation. If the event happens slowly enough, the system first tries to regulate the output to 4.9 V as in a normal overvoltage scenario. However, if this is not sufficient, or if the event happens too quickly, the ADP8863 enters overvoltage protection (OVP) mode when $V_{OUT}$ exceeds the OVP threshold (typically 5.8 V). In OVP mode, only the charge pump is disabled to prevent $V_{OUT}$ from rising too high. The current sources and all other device functionality remain intact. When the output voltage falls by about 500 mV (to 5.3 V typical), the charge pump resumes operation. If the fault or load event recurs, the process may repeat. An interrupt flag is set at each OVP instance.

## THERMAL SHUTDOWN/OVERTEMPERATURE PROTECTION

If the die temperature of the ADP8863 rises above a safe limit (150°C typical), the controllers enter thermal shutdown (TSD) protection mode. In this mode, most of the internal functions shut down, the part enters standby, and the TSD_INT interrupt (Register 0x02) is set. When the die temperature decreases below ~130°C, the part can be restarted. To restart the part, remove it from standby. No interrupt is generated when the die temperature falls below 130°C. However, if the software clears the pending TSD_INT interrupt and the temperature remains above 130°C, another interrupt is generated.

The complete state machine for these faults (SCP, OVP, and TSD) is shown in Figure 47.

## INTERRUPTS

There are five interrupt sources available on the ADP8863 in Register 0x02.

- Main light sensor comparator: The CMP_INT interrupt sets every time the main light sensor comparator detects a threshold (L2 or L3) transition (rising or falling condition).
- Sensor Comparator 2: The CMP2_INT interrupt works the same way as CMP_INT, except that the sensing input derives from the second light sensor. The programmable thresh-olds are the same as for the main light sensor comparator.
- Overvoltage protection: OVP_INT is generated when the output voltage exceeds 5.8 V (typical).
- Thermal shutdown circuit: an interrupt (TSD_INT) is generated when entering overtemperature protection.
- Short-circuit detection: SHORT_INT is generated when the device enters short-circuit protection mode.

The interrupt (if any) that appears on the nINT pin is determined by the bits mapped in Register INTR_EN (0x03). To clear an interrupt, write a 1 to the interrupt in the MDCR2 register (0x02) or reset the part. Reading the interrupt, or writing a 0, has no effect.

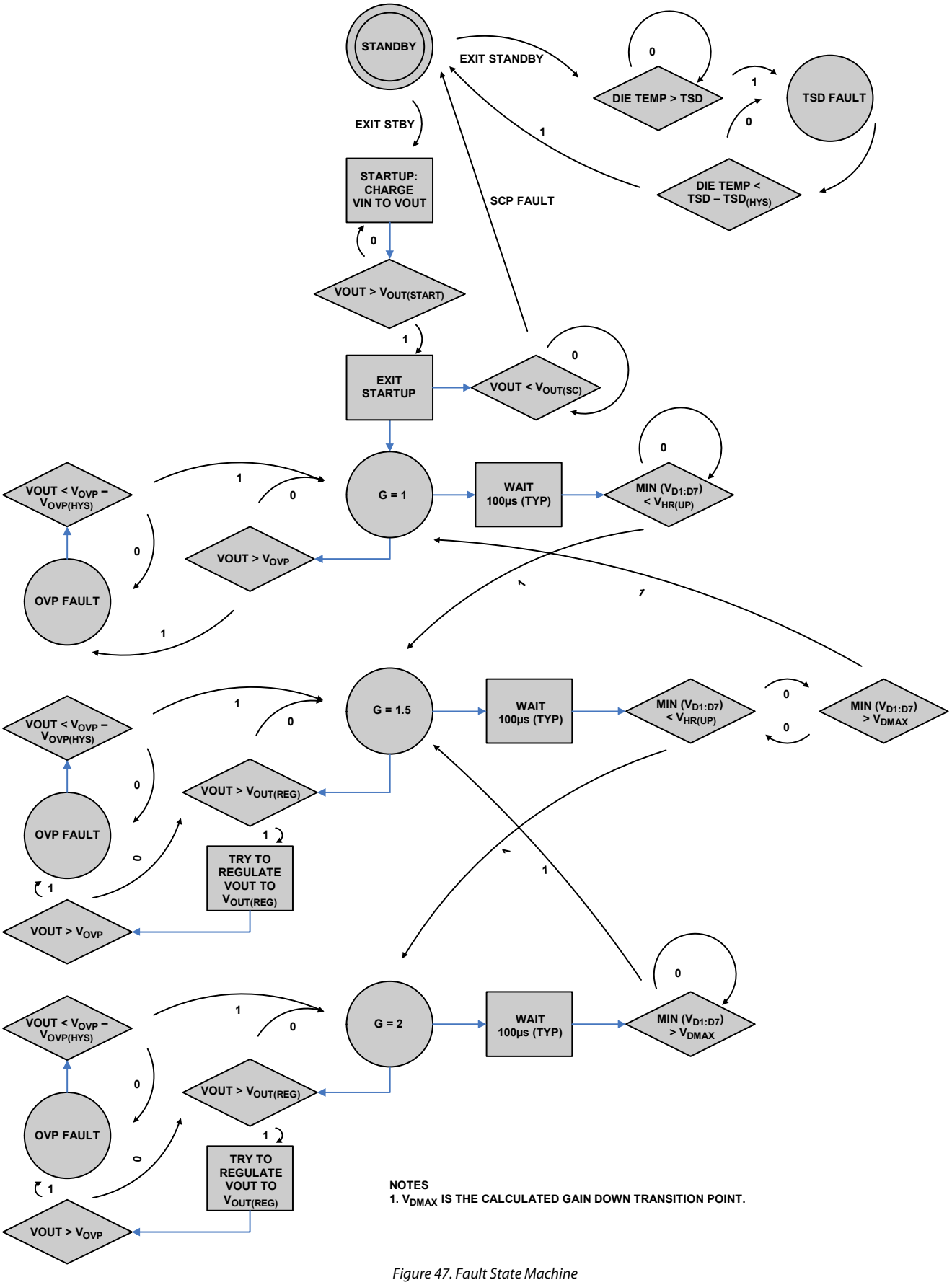


*Figure 47. Fault State Machine*

# APPLICATIONS INFORMATION

The ADP8863 allows the charge pump to operate efficiently with a minimum of external components. Specifically, the user must select an input capacitor ($C_{IN}$), output capacitor ($C_{OUT}$), and two charge pump fly capacitors (C1 and C2). $C_{IN}$ should be 1 µF or greater. The value must be high enough to produce a stable input voltage signal at the minimum input voltage and maximum output load. A 1 µF capacitor for $C_{OUT}$ is recommended. Larger values are permissible, but care must be exercised to ensure that VOUT charges above 55% (typical) of $V_{IN}$ within 4 ms (typical). See the Short-Circuit Protection Mode section for more details.

For best practice, it is recommended that the two charge pump fly capacitors be 1 µF; larger values are not recommended, and smaller values may reduce the ability of the charge pump to deliver maximum current. For optimal efficiency, the charge pump fly capacitors should have low equivalent series resistance (ESR). Low ESR X5R or X7R capacitors are recommended for all four components. The use of fly capacitors sized 0402 and smaller is allowed, but the GDWN_DIS bit in Register 0x01 must be set. Minimum voltage ratings should adhere to the guidelines in Table 7.

**Table 7. Capacitor Stress in Each Charge Pump Gain State**

| Capacitor | Gain = 1× | Gain = 1.5× | Gain = 2× |
|---|---|---|---|
| $C_{IN}$ | $V_{IN}$ | $V_{IN}$ | $V_{IN}$ |
| $C_{OUT}$ | $V_{IN}$ | $V_{IN} \times 1.5$ (max of 5.5 V) | $V_{IN} \times 2.0$ (max of 5.5 V) |
| C1 | None | $V_{IN}/2$ | $V_{IN}$ |
| C2 | None | $V_{IN}/2$ | $V_{IN}$ |

If one or both ambient light sensor comparator inputs (CMP_IN and D6) are used, a small capacitor (0.1 µF is recommended) must be connected from the input to ground.

Any color LED can be used if the Vf (forward voltage) is less than 4.1 V. However, using lower Vf LEDs reduces the input power consumption by allowing the charge pump to operate at lower gain states.

The equivalent circuit model for a charge pump is shown in Figure 48.

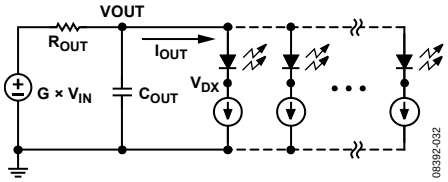


*Figure 48. Charge Pump Equivalent Circuit Model*

The input voltage is multiplied by the gain (G) and delivered to the output through an effective resistance ($R_{OUT}$). The output current flows through $R_{OUT}$ and produces an IR drop to yield

$$V_{OUT} = G \times V_{IN} - I_{OUT} \times R_{OUT}(G) \quad (8)$$

The $R_{OUT}$ term is a combination of the $R_{DSON}$ resistance for the switches used in the charge pump and a small resistance that accounts for the effective dynamic charge pump resistance. The $R_{OUT}$ level changes based upon the gain (the configuration of the switches). Typical $R_{OUT}$ values are given in Table 1, Figure 13, and Figure 14. $V_{OUT}$ is also equal to the largest Vf of the LEDs used plus the voltage drop across the regulating current source. This gives

$$V_{OUT} = Vf_{(MAX)} + V_{DX} \quad (9)$$

Combining Equation 8 and Equation 9 gives

$$V_{IN} = (Vf_{(MAX)} + V_{DX} + I_{OUT} \times R_{OUT}(G))/G \quad (10)$$

Equation 10 is useful for calculating approximate bounds for the charge pump design.

### *Determining the Transition Point of the Charge Pump*

Consider the following design example, where:

$Vf_{(MAX)}$ = 3.7 V
$I_{OUT}$ = 140 mA (7 LEDs at 20 mA each)
$R_{OUT}(G = 1.5\times)$ = 3 Ω (obtained from Figure 13)

At the point of a gain transition, $V_{DX} = V_{HR(UP)}$. Table 1 gives the typical value of $V_{HR(UP)}$ as 0.2 V. Therefore, the input voltage level when the gain transitions from 1.5× to 2× is

$$V_{IN} = (3.7\text{ V} + 0.2\text{ V} + 140\text{ mA} \times 3\ \Omega)/1.5 = 2.88\text{ V}$$

## LAYOUT GUIDELINES

Note the following layout guidelines:

- For optimal noise immunity, place the $C_{IN}$ and $C_{OUT}$ capacitors as close as possible to their respective pins. These capacitors should share a short ground trace. If the LEDs are a significant distance from the VOUT pin, another capacitor on VOUT, placed closer to the LEDs, is advisable.
- For optimal efficiency, place the charge pump fly capacitors (C1 and C2) as close to the part as possible.
- The ADP8863 does not distinguish between power ground and analog ground. Therefore, both ground pins can be connected directly together. It is recommended that these ground pins be connected at the ground for the input and output capacitors.
- The LFCSP package requires the exposed pad to be soldered at the board to the GND1 and/or GND2 pin(s).
- Unused diode pins (Pin D1 to Pin D7) can be connected to ground or to VOUT, or remain floating. However, the unused diode current sinks must be disabled by setting them as independent sinks in Register 0x05 and then disabling them in Register 0x10. If they are not disabled, the charge pump efficiency may suffer.
- If the CMP_IN phototransistor input is not used, it can be connected to ground or remain floating.
- If the interrupt pin (nINT) is not used, connect it to ground or leave it floating. Never connect it to a voltage supply, except through a ≥1 kΩ series resistor.
- The ADP8863 has an integrated noise filter on the nRST pin. Under normal conditions, it is not necessary to filter the reset line. However, if the part is exposed to an unusually noisy signal, it is beneficial to add a small RC filter or bypass capacitor on this pin. If the nRST pin is not used, it must be pulled well above the $V_{IH(MIN)}$ level (see Table 1). Do not allow the nRST pin to float.

# I²C PROGRAMMING AND DIGITAL CONTROL

The ADP8863 provides full software programmability to facilitate its adoption in various product architectures. The I²C address is 0101011x (x = 0 during write, x = 1 during read). Therefore, the write address is 0x56 and the read address is 0x57.

Note the following general behavior of registers:

- All registers are set to their default values during reset or after a UVLO event.
- All registers are read/write unless otherwise specified.
- Unused bits are read as zero.

Table 8 to Table 84 provide register and bit descriptions. The reset value for all bits in the bit map tables is all 0s, except in Table 10 (see Table 10 for its unique reset value). Wherever the acronym N/A appears in the tables, it means not applicable.

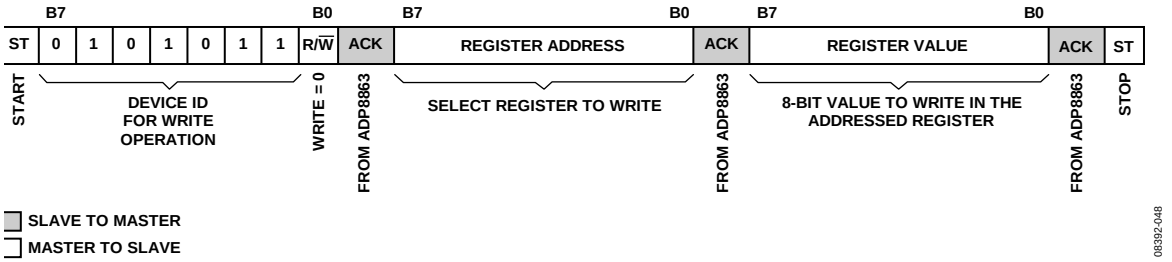


*Figure 49. I²C Write Sequence*

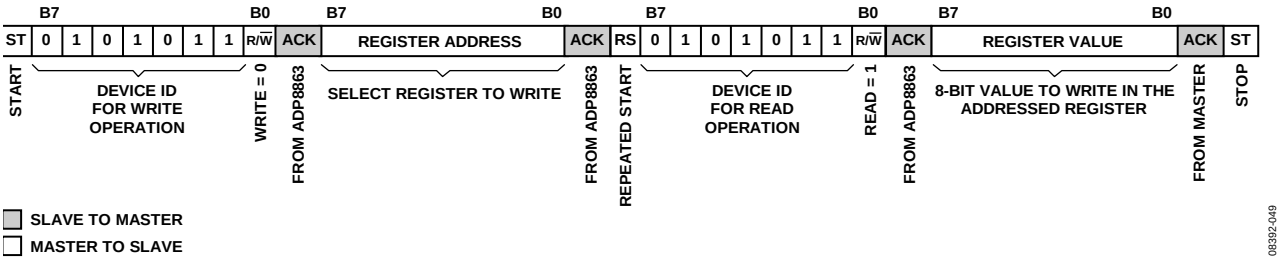


*Figure 50. I²C Read Sequence*

**Table 8. Register Set Definitions**

| Address (Hex) | Register Name | Description |
|---|---|---|
| 0x00 | MFDVID | Manufacturer and device ID |
| 0x01 | MDCR | Device mode and status |
| 0x02 | MDCR2 | Device mode and Status Register 2 |
| 0x03 | INTR_EN | Interrupts enable |
| 0x04 | CFGR | Configuration register |
| 0x05 | BLSEN | Sink enable, backlight or independent |
| 0x06 | BLOFF | Backlight off timeout |
| 0x07 | BLDIM | Backlight dim timeout |
| 0x08 | BLFR | Backlight fade in and fade out rates |
| 0x09 | BLMX1 | Backlight (brightness Level 1—daylight) maximum current |
| 0x0A | BLDM1 | Backlight (brightness Level 1—daylight) dim current |
| 0x0B | BLMX2 | Backlight (brightness Level 2—office) maximum current |
| 0x0C | BLDM2 | Backlight (brightness Level 2—office) dim current |
| 0x0D | BLMX3 | Backlight (brightness Level 3—dark) maximum current |
| 0x0E | BLDM3 | Backlight (brightness Level 3—dark) dim current |
| 0x0F | ISCFR | Independent sink current fade control register |
| 0x10 | ISCC | Independent sink current control register |
| 0x11 | ISCT1 | Independent sink current timer register, LED[7:5] |
| 0x12 | ISCT2 | Independent sink current timer register, LED[4:1] |
| 0x13 | ISCF | Independent sink current fade register |
| 0x14 | ISC7 | Independent sink current, LED7 |
| 0x15 | ISC6 | Independent sink current, LED6 |
| 0x16 | ISC5 | Independent sink current, LED5 |
| 0x17 | ISC4 | Independent sink current, LED4 |
| 0x18 | ISC3 | Independent sink current, LED3 |
| 0x19 | ISC2 | Independent sink current, LED2 |
| 0x1A | ISC1 | Independent sink current, LED1 |
| 0x1B | CCFG | Comparator configuration |
| 0x1C | CCFG2 | Second comparator configuration |
| 0x1D | L2_TRP | L2 comparator reference |
| 0x1E | L2_HYS | L2 hysteresis |
| 0x1F | L3_TRP | L3 comparator reference |
| 0x20 | L3_HYS | L3 hysteresis |
| 0x21 | PH1LEVL | First phototransistor ambient light level—low byte register |
| 0x22 | PH1LEVH | First phototransistor ambient light level—high byte register |
| 0x23 | PH2LEVL | Second phototransistor ambient light level—low byte register |
| 0x24 | PH2LEVH | Second phototransistor ambient light level—high byte register |

**Table 9. Register Map**

| Addr (Hex) | Reg. Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | MFDVID | Manufacturer ID | | | | Device ID | | | |
| 0x01 | MDCR | Reserved | INT_CFG | nSTBY | DIM_EN | GDWN_DIS | SIS_EN | CMP_AUTOEN | BL_EN |
| 0x02 | MDCR2 | Reserved | | | SHORT_INT | TSD_INT | OVP_INT | CMP2_INT | CMP_INT |
| 0x03 | INTR_EN | Reserved | | | SHORT_IEN | TSD_IEN | OVP_IEN | CMP2_IEN | CMP_IEN |
| 0x04 | CFGR | Reserved | SEL_AB | CMP2_SEL | BLV | | Law | | FOVR |
| 0x05 | BLSEN | Reserved | D7EN | D6EN | D5EN | D4EN | D3EN | D2EN | D1EN |
| 0x06 | BLOFF | Reserved | OFFT | | | | | | |
| 0x07 | BLDIM | Reserved | DIMT | | | | | | |
| 0x08 | BLFR | BL_FO | | | | BL_FI | | | |
| 0x09 | BLMX1 | Reserved | BL1_MC | | | | | | |
| 0x0A | BLDM1 | Reserved | BL1_DC | | | | | | |
| 0x0B | BLMX2 | Reserved | BL2_MC | | | | | | |
| 0x0C | BLDM2 | Reserved | BL2_DC | | | | | | |
| 0x0D | BLMX3 | Reserved | BL3_MC | | | | | | |
| 0x0E | BLDM3 | Reserved | BL3_DC | | | | | | |
| 0x0F | ISCFR | Reserved | | | | | | SC_LAW | |
| 0x10 | ISCC | Reserved | SC7_EN | SC6_EN | SC5_EN | SC4_EN | SC3_EN | SC2_EN | SC1_EN |
| 0x11 | ISCT1 | SCON | | SC7OFF | | SC6OFF | | SC5OFF | |
| 0x12 | ISCT2 | SC4OFF | | SC3OFF | | SC2OFF | | SC1OFF | |
| 0x13 | ISCF | SCFO | | | | SCFI | | | |
| 0x14 | ISC7 | SCR | SCD7 | | | | | | |
| 0x15 | ISC6 | Reserved | SCD6 | | | | | | |
| 0x16 | ISC5 | Reserved | SCD5 | | | | | | |
| 0x17 | ISC4 | Reserved | SCD4 | | | | | | |
| 0x18 | ISC3 | Reserved | SCD3 | | | | | | |
| 0x19 | ISC2 | Reserved | SCD2 | | | | | | |
| 0x1A | ISC1 | Reserved | SCD1 | | | | | | |
| 0x1B | CCFG | FILT | | | FORCE_RD | L3_OUT | L2_OUT | L3_EN | L2_EN |
| 0x1C | CCFG2 | FILT2 | | | FORCE_RD2 | L3_OUT2 | L2_OUT2 | L3_EN2 | L2_EN2 |
| 0x1D | L2_TRP | L2_TRP | | | | | | | |
| 0x1E | L2_HYS | L2_HYS | | | | | | | |
| 0x1F | L3_TRP | L3_TRP | | | | | | | |
| 0x20 | L3_HYS | L3_HYS | | | | | | | |
| 0x21 | PH1LEVL | PH1LEV_LOW | | | | | | | |
| 0x22 | PH1LEVH | Reserved | | | PH1LEV_HIGH | | | | |
| 0x23 | PH2LEVL | PH2LEV_LOW | | | | | | | |
| 0x24 | PH2LEVH | Reserved | | | PH2LEV_HIGH | | | | |

### *Manufacturer and Device ID (MFDVID)—Register 0x00*

This is a read-only register.

**Table 10. MFDVID Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Manufacturer ID | | | | Device ID | | | |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

### *Mode Control Register (MDCR)—Register 0x01*

**Table 11. MDCR Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | INT_CFG | nSTBY | DIM_EN | GDWN_DIS | SIS_EN | CMP_AUTOEN | BL_EN |

**Table 12. Bit Descriptions for the MDCR Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved. |
| INT_CFG | 6 | Interrupt configuration.<br>1 = processor interrupt deasserts for 50 µs and reasserts with pending events.<br>0 = processor interrupt remains asserted if the host tries to clear the interrupt while there is a pending event. |
| nSTBY | 5 | 1 = device is in active mode.<br>0 = device is in standby mode; only the $I^2C$ interface is enabled. |
| DIM_EN | 4 | DIM_EN is set by the hardware after a dim timeout. The user may also force the backlight into dim mode by asserting this bit. Dim mode can only be entered if BL_EN is also enabled.<br>1 = backlight is operating at the dim current level (BL_EN must also be asserted).<br>0 = backlight is not in dim mode. |
| GDWN_DIS | 3 | Gain down disable bit. Setting this bit does not allow the charge pump to switch to lower gains.<br>1 = the charge pump does not switch down in gain until all LEDs are off. The charge pump switches up in gain as needed. This feature is useful if the ADP8863 charge pump is used to drive an external load. This feature must be used when utilizing small fly capacitors (0402 or smaller).<br>0 = the charge pump automatically switches up and down in gain. This provides optimal efficiency, but is not suitable for driving loads that are not connected through the ADP8863 diode drivers. Additionally, the charge pump fly capacitors should be low ESR and sized 0603 or greater. |
| SIS_EN | 2 | Synchronous independent sinks enable.<br>1 = enables all LED current sinks designated as independent sinks. All of the ISC enable bits must be cleared; if any of the SCx_EN bits in Register 0x10 are set, this bit has no effect.<br>0 = disables all sinks designated as independent sinks. All of the ISC enable bits must be cleared; if any of the SCx_EN bits in Register 0x10 are set, this bit has no effect. |
| CMP_AUTOEN | 1 | 1 = backlight automatically responds to the comparator outputs (L2_OUT and L3_OUT). L2_EN and/or L3_EN must be set for this to function. BLV values in Register 0x04 are overridden.<br>0 = backlight does not respond automatically to comparator level changes. The user can manually select backlight operating levels using Bit BLV in Register 0x04. |
| BL_EN | 0 | 1 = backlight is enabled (nSTBY must also be asserted).<br>0 = backlight is disabled. |

### *Mode Control Register 2 (MDCR2)—Register 0x02*

**Table 13. MDCR2 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | SHORT_INT | TSD_INT | OVP_INT | CMP2_INT | CMP_INT |

**Table 14. Bit Descriptions for the MDCR2 Register**

| Bit Name | Bit No. | Description[1] |
|---|---|---|
| N/A | [7:5] | Reserved. |
| SHORT_INT | 4 | Short-circuit error interrupt.<br>1 = a short-circuit or overload condition on VOUT has been detected.<br>0 = no short-circuit or overload condition has been detected. |
| TSD_INT | 3 | Thermal shutdown interrupt.<br>1 = the device temperature has exceeded 150°C (typical).<br>0 = no overtemperature condition has been detected. |
| OVP_INT | 2 | Overvoltage interrupt.<br>1 = VOUT has exceeded $V_{OVP}$.<br>0 = VOUT has not exceeded $V_{OVP}$. |
| CMP2_INT | 1 | 1 = the second ALS comparator (CMP_IN2) has changed state.<br>0 = the second sensor comparator has not been triggered. |
| CMP_INT | 0 | 1 = main ALS comparator (CMP_IN) has changed state.<br>0 = the main sensor comparator has not been triggered. |

[1] Interrupt bits are cleared by writing a 1 to the flag; writing a 0 or reading the flag has no effect.

### *Interrupt Enable (INTR_EN)—Register 0x03*

**Table 15. INTR_EN Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | SHORT_IEN | TSD_IEN | OVP_IEN | CMP2_IEN | CMP_IEN |

**Table 16. Bit Descriptions for the INTR_EN Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | [7:5] | Reserved. |
| SHORT_IEN | 4 | Short-circuit interrupt is enabled. When the SHORT_INT status bit is set after an error condition, an interrupt is raised to the host if the SHORT_IEN flag is enabled.<br>1 = the short-circuit interrupt is enabled.<br>0 = the short-circuit interrupt is disabled (the SHORT_INT flag continues to assert). |
| TSD_IEN | 3 | Thermal shutdown interrupt is enabled. When the TSD_INT status bit is set after an error condition, an interrupt is raised to the host if the TSD_IEN flag is enabled.<br>1 = the thermal shutdown interrupt is enabled.<br>0 = the thermal shutdown interrupt is disabled (the TSD_INT flag continues to assert). |
| OVP_IEN | 2 | Overvoltage interrupt enabled. When the OVP_INT status bit is set after an error condition, an interrupt is raised to the host if the OVP_IEN flag is enabled.<br>1 = the overvoltage interrupt is enabled.<br>0 = the overvoltage interrupt is disabled (the OVP_INT flag continues to assert). |
| CMP2_IEN | 1 | When the CMP2_INT status bit is set after an enabled comparator trips, an interrupt is raised if the CMP2_IEN flag is enabled.<br>1 = the second phototransistor comparator interrupt is enabled.<br>0 = the second phototransistor comparator interrupt is disabled (the CMP2_INT flag continues to assert). |
| CMP_IEN | 0 | When the CMP_INT status bit is set after an enabled comparator trips, an interrupt is raised if the CMP_IEN flag is enabled.<br>1 = the main comparator interrupt is enabled.<br>0 = the main comparator interrupt is disabled (the CMP_INT flag continues to assert). |

## BACKLIGHT REGISTER DESCRIPTIONS

### *Configuration Register (CFGR)—Register 0x04*

**Table 17. CFGR Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SEL_AB | CMP2_SEL | BLV | | Law | | FOVR |

**Table 18. Bit Descriptions for the CFGR Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved. |
| SEL_AB | 6 | 1 = selects the second phototransistor (CMP_IN2) to control the backlight.<br>0 = selects the main phototransistor (CMP_IN) to control the backlight. |
| CMP2_SEL | 5 | 1 = the second phototransistor is enabled; the current sink on D6 is disabled.<br>0 = the second phototransistor is disabled. |
| BLV | [4:3] | Brightness level. This field indicates the brightness level at which the device is operating. The software may force the backlight to operate at one of the three brightness levels. Setting CMP_AUTOEN high (Register 0x01) sets these values automatically and overwrites any previously written values.<br>00 = Level 1 (daylight).<br>01 = Level 2 (office).<br>10 = Level 3 (dark).<br>11 = off (backlight set to 0 mA). |
| Law | [2:1] | Backlight transfer law.<br>00 = linear law DAC, linear time steps.<br>01 = square law DAC, linear time steps.<br>10 = square law DAC, nonlinear time steps (Cubic 10).<br>11 = square law DAC, nonlinear time steps (Cubic 11). |
| FOVR | 0 | Backlight fade override.<br>1 = the backlight fade override is enabled.<br>0 = the backlight fade override is disabled. |

### *Backlight Sink Enable (BLSEN)—Register 0x05*

**Table 19. BLSEN Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | D7EN | D6EN | D5EN | D4EN | D3EN | D2EN | D1EN |

**Table 20. Bit Descriptions for the BLSEN Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved |
| D7EN | 6 | Diode 7 backlight sink enable<br>1 = selects LED7 as an independent sink<br>0 = connects LED7 sink to backlight enable (BL_EN) |
| D6EN | 5 | Diode 6 backlight sink enable<br>1 = selects LED6 as an independent sink<br>0 = connects LED6 sink to backlight enable (BL_EN) |
| D5EN | 4 | Diode 5 backlight sink enable<br>1 = selects LED5 as an independent sink<br>0 = connects LED5 sink to backlight enable (BL_EN) |
| D4EN | 3 | Diode 4 backlight sink enable<br>1 = selects LED4 as an independent sink<br>0 = connects LED4 sink to backlight enable (BL_EN) |
| D3EN | 2 | Diode 3 backlight sink enable<br>1 = selects LED3 as an independent sink<br>0 = connects LED3 sink to backlight enable (BL_EN) |

| Bit Name | Bit No. | Description |
|---|---|---|
| D2EN | 1 | Diode 2 backlight sink enable<br>1 = selects LED2 as an independent sink<br>0 = connects LED2 sink to backlight enable (BL_EN) |
| D1EN | 0 | Diode 1 backlight sink enable<br>1 = selects LED1 as an independent sink<br>0 = connects LED1 sink to backlight enable (BL_EN) |

### *Backlight Off Timeout (BLOFF)—Register 0x06*

**Table 21. BLOFF Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | OFFT | | | | | | |

**Table 22. Bit Descriptions for the BLOFF Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved. |
| OFFT | [6:0] | Backlight off timeout. After the off timeout (OFFT) period, the backlight turns off. If the dim timeout (DIMT) is enabled, the off timeout starts after the dim timeout.<br>0000000 = timeout disabled<br>0000001 = 1 sec<br>0000010 = 2 sec<br>0000011 = 3 sec<br>…<br>1111111 = 127 sec |

### *Backlight Dim Timeout (BLDIM)—Register 0x07*

**Table 23. BLDIM Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | DIMT | | | | | | |

**Table 24. Bit Descriptions for the BLDIM Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved. |
| DIMT | [6:0] | Backlight dim timeout. After the dim timeout (DIMT) period, the backlight is set to the dim current value. The dim timeout starts after the backlight reaches the maximum current.<br>0000000 = timeout disabled<br>0000001 = 1 sec<br>0000010 = 2 sec<br>0000011 = 3 sec<br>…<br>1111111 = 127 sec |

### *Backlight Fade (BLFR)—Register 0x08*

**Table 25. BLFR Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| BL_FO | | | | BL_FI | | | |

**Table 26. Bit Descriptions for the BLFR Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| BL_FO | [7:4] | Backlight fade out rate. If fade out is disabled (BL_FO = 0000), the backlight changes instantly (within 100 ms). If the fade out rate is set, the backlight fades from its current value to the dim or the off value. The times listed for BL_FO are for a full-scale fade out (30 mA to 0 mA). Fades between closer current values reduce the fade time. See the Automated Fade In and Fade Out Section for more information.<br>0000 = 0.1 sec (fade out disabled)[1]<br>0001 = 0.3 sec<br>0010 = 0.6 sec<br>0011 = 0.9 sec<br>0100 = 1.2 sec<br>0101 = 1.5 sec<br>0110 = 1.8 sec<br>0111 = 2.1 sec<br>1000 = 2.4 sec<br>1001 = 2.7 sec<br>1010 = 3.0 sec<br>1011 = 3.5 sec<br>1100 = 4.0 sec<br>1101 = 4.5 sec<br>1110 = 5.0 sec<br>1111 = 5.5 sec |
| BL_FI | [3:0] | Backlight fade in rate. If fade in is disabled (BL_FI = 0000), the backlight changes instantly (within 100 ms). If the fade in rate is set, the backlight fades from its current value to its maximum value when the backlight is turned on. The times listed for BL_FI are for a full-scale fade in (0 mA to 30 mA). Fades between closer current values reduce the fade time. See the Automated Fade In and Fade Out Section for more information.<br>0000 = 0.1 sec (fade in disabled)[1]<br>0001 = 0.3 sec<br>0010 = 0.6 sec<br>0011 = 0.9 sec<br>…<br>1111 = 5.5 sec |

[1] When fade in and fade out are disabled, the backlight does not instantly fade, but instead, fades rapidly within about 100 ms.

### *Backlight Level 1 (Daylight) Maximum Current Register (BLMX1)—Register 0x09*

**Table 27. BLMX1 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | BL1_MC | | | | | | |

**Table 28. Bit Descriptions for the BLMX1 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| BL1_MC | [6:0] | Backlight Level 1 (daylight) maximum current. The backlight maximum current can be set according to the linear or square law function (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

**Table 29. Linear and Square Law Currents Per DAC Code (SCR = 0)**

| DAC Code | Linear Law (mA) | Square Law (mA)[1] | DAC Code | Linear Law (mA) | Square Law (mA)[1] |
|---|---|---|---|---|---|
| 0x00 | 0 | 0.000 | 0x22 | 8.031 | 2.150 |
| 0x01 | 0.236 | 0.002 | 0x23 | 8.268 | 2.279 |
| 0x02 | 0.472 | 0.007 | 0x24 | 8.504 | 2.411 |
| 0x03 | 0.709 | 0.017 | 0x25 | 8.740 | 2.546 |
| 0x04 | 0.945 | 0.030 | 0x26 | 8.976 | 2.686 |
| 0x05 | 1.181 | 0.047 | 0x27 | 9.213 | 2.829 |
| 0x06 | 1.417 | 0.067 | 0x28 | 9.449 | 2.976 |
| 0x07 | 1.654 | 0.091 | 0x29 | 9.685 | 3.127 |
| 0x08 | 1.890 | 0.119 | 0x2A | 9.921 | 3.281 |
| 0x09 | 2.126 | 0.151 | 0x2B | 10.157 | 3.439 |
| 0x0A | 2.362 | 0.186 | 0x2C | 10.394 | 3.601 |
| 0x0B | 2.598 | 0.225 | 0x2D | 10.630 | 3.767 |
| 0x0C | 2.835 | 0.268 | 0x2E | 10.866 | 3.936 |
| 0x0D | 3.071 | 0.314 | 0x2F | 11.102 | 4.109 |
| 0x0E | 3.307 | 0.365 | 0x30 | 11.339 | 4.285 |
| 0x0F | 3.543 | 0.419 | 0x31 | 11.575 | 4.466 |
| 0x10 | 3.780 | 0.476 | 0x32 | 11.811 | 4.650 |
| 0x11 | 4.016 | 0.538 | 0x33 | 12.047 | 4.838 |
| 0x12 | 4.252 | 0.603 | 0x34 | 12.283 | 5.029 |
| 0x13 | 4.488 | 0.671 | 0x35 | 12.520 | 5.225 |
| 0x14 | 4.724 | 0.744 | 0x36 | 12.756 | 5.424 |
| 0x15 | 4.961 | 0.820 | 0x37 | 12.992 | 5.627 |
| 0x16 | 5.197 | 0.900 | 0x38 | 13.228 | 5.833 |
| 0x17 | 5.433 | 0.984 | 0x39 | 13.465 | 6.043 |
| 0x18 | 5.669 | 1.071 | 0x3A | 13.701 | 6.257 |
| 0x19 | 5.906 | 1.163 | 0x3B | 13.937 | 6.475 |
| 0x1A | 6.142 | 1.257 | 0x3C | 14.173 | 6.696 |
| 0x1B | 6.378 | 1.356 | 0x3D | 14.409 | 6.921 |
| 0x1C | 6.614 | 1.458 | 0x3E | 14.646 | 7.150 |
| 0x1D | 6.850 | 1.564 | 0x3F | 14.882 | 7.382 |
| 0x1E | 7.087 | 1.674 | 0x40 | 15.118 | 7.619 |
| 0x1F | 7.323 | 1.787 | 0x41 | 15.354 | 7.859 |
| 0x20 | 7.559 | 1.905 | 0x42 | 15.591 | 8.102 |
| 0x21 | 7.795 | 2.026 | 0x43 | 15.827 | 8.350 |

| DAC Code | Linear Law (mA) | Square Law (mA)[1] |
|---|---|---|
| 0x44 | 16.063 | 8.601 |
| 0x45 | 16.299 | 8.855 |
| 0x46 | 16.535 | 9.114 |
| 0x47 | 16.772 | 9.376 |
| 0x48 | 17.008 | 9.642 |
| 0x49 | 17.244 | 9.912 |
| 0x4A | 17.480 | 10.185 |
| 0x4B | 17.717 | 10.463 |
| 0x4C | 17.953 | 10.743 |
| 0x4D | 18.189 | 11.028 |
| 0x4E | 18.425 | 11.316 |
| 0x4F | 18.661 | 11.608 |
| 0x50 | 18.898 | 11.904 |
| 0x51 | 19.134 | 12.203 |
| 0x52 | 19.370 | 12.507 |
| 0x53 | 19.606 | 12.814 |
| 0x54 | 19.842 | 13.124 |
| 0x55 | 20.079 | 13.439 |
| 0x56 | 20.315 | 13.757 |
| 0x57 | 20.551 | 14.078 |
| 0x58 | 20.787 | 14.404 |
| 0x59 | 21.024 | 14.733 |
| 0x5A | 21.260 | 15.066 |
| 0x5B | 21.496 | 15.403 |
| 0x5C | 21.732 | 15.743 |
| 0x5D | 21.968 | 16.087 |
| 0x5E | 22.205 | 16.435 |
| 0x5F | 22.441 | 16.787 |
| 0x60 | 22.677 | 17.142 |
| 0x61 | 22.913 | 17.501 |
| 0x62 | 23.150 | 17.863 |
| 0x63 | 23.386 | 18.230 |
| 0x64 | 23.622 | 18.600 |
| 0x65 | 23.858 | 18.974 |
| 0x66 | 24.094 | 19.351 |
| 0x67 | 24.331 | 19.733 |
| 0x68 | 24.567 | 20.118 |
| 0x69 | 24.803 | 20.507 |
| 0x6A | 25.039 | 20.899 |
| 0x6B | 25.276 | 21.295 |
| 0x6C | 25.512 | 21.695 |
| 0x6D | 25.748 | 22.099 |
| 0x6E | 25.984 | 22.506 |
| 0x6F | 26.220 | 22.917 |
| 0x70 | 26.457 | 23.332 |
| 0x71 | 26.693 | 23.750 |
| 0x72 | 26.929 | 24.173 |
| 0x73 | 27.165 | 24.599 |
| 0x74 | 27.402 | 25.028 |
| 0x75 | 27.638 | 25.462 |
| 0x76 | 27.874 | 25.899 |
| 0x77 | 28.110 | 26.340 |
| 0x78 | 28.346 | 26.784 |
| 0x79 | 28.583 | 27.232 |
| 0x7A | 28.819 | 27.684 |
| 0x7B | 29.055 | 28.140 |
| 0x7C | 29.291 | 28.599 |
| 0x7D | 29.528 | 29.063 |
| 0x7E | 29.764 | 29.529 |
| 0x7F | 30.000 | 30.000 |

[1] Cubic 10 and Cubic 11 laws use the square law DAC setting but vary the time step per DAC code (see the Automated Fade In and Fade Out section).

### *Backlight Level 1 (Daylight) Dim Current Register (BLDM1)—Register 0x0A*

**Table 30. BLDM1 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | BL1_DC | | | | | | |

**Table 31. Bit Descriptions for the BLDM1 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| BL1_DC | [6:0] | Backlight Level 1 (daylight) dim current. The backlight is set to the dim current value after a dim timeout or if the DIM_EN flag is set by the user (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Backlight Level 2 (Office) Maximum Current Register (BLMX2)—Register 0x0B*

**Table 32. BLMX2 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | BL2_MC | | | | | | |

**Table 33. Bit Descriptions for the BLMX2 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| BL2_MC | [6:0] | Backlight Level 2 (office) maximum current (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Backlight Level 2 (Office) Dim Current Register (BLDM2)—Register 0x0C*

**Table 34. BLDM2 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | BL2_DC | | | | | | |

**Table 35. Bit Descriptions for the BLDM2 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| BL2_DC | [6:0] | Backlight Level 2 (office) dim current. See Table 29 for a complete list of values. The backlight is set to the dim current value after a dim timeout or if the DIM_EN flag is set by the user. | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Backlight Level 3 (Dark) Maximum Current Register (BLMX3)—Register 0x0D*

**Table 36. BLMX3 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | BL3_MC | | | | | | |

**Table 37. Bit Descriptions for the BLMX3 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| BL3_MC | [6:0] | Backlight Level 3 (dark) maximum current. See Table 29 for a complete list of values. | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Backlight Level 3 (Dark) Dim Current Register (BLDM3)—Register 0x0E*

**Table 38. BLDM3 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | BL3_DC | | | | | | |

**Table 39. Bit Descriptions for the BLDM3 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| BL3_DC | [6:0] | Backlight Level 3 (dark) dim current. See Table 29 for a complete list of values. The backlight is set to the dim current value after a dim timeout or if the DIM_EN flag is set by the user. | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

## INDEPENDENT SINK REGISTER DESCRIPTIONS

### *Independent Sink Current Fade Control Register (ISCFR)—Register 0x0F*

**Table 40. ISCFR Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | SC_LAW | |

**Table 41. Bit Descriptions for the ISCFR Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | [7:2] | Reserved |
| SC_LAW | [1:0] | Independent sink current fade transfer law<br>00 = linear law DAC, linear time steps<br>01 = square law DAC, linear time steps<br>10 = square law DAC, nonlinear time steps (Cubic 10)<br>11 = square law DAC, nonlinear time steps (Cubic 11) |

### *Independent Sink Current Control (ISCC)—Register 0x10*

**Table 42. ISCC Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SC7_EN | SC6_EN | SC5_EN | SC4_EN | SC3_EN | SC2_EN | SC1_EN |

**Table 43. Bit Descriptions for the ISCC Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | 7 | Reserved |
| SC7_EN | 6 | This enable acts upon LED7<br>1 = SC7 is turned on<br>0 = SC7 is turned off |
| SC6_EN | 5 | This enable acts upon LED6<br>1 = SC6 is turned on<br>0 = SC6 is turned off |
| SC5_EN | 4 | This enable acts upon LED5<br>1 = SC5 is turned on<br>0 = SC5 is turned off |

| Bit Name | Bit No. | Description |
|---|---|---|
| SC4_EN | 3 | This enable acts upon LED4.<br>1 = SC4 is turned on.<br>0 = SC4 is turned off. |
| SC3_EN | 2 | This enable acts upon LED3.<br>1 = SC3 is turned on.<br>0 = SC3 is turned off. |
| SC2_EN | 1 | This enable acts upon LED2.<br>1 = SC2 is turned on.<br>0 = SC2 is turned off. |
| SC1_EN | 0 | This enable acts upon LED1.<br>1 = SC1 is turned on.<br>0 = SC1 is turned off. |

### *Independent Sink Current Time (ISCT1)—Register 0x11*

**Table 44. ISCT1 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| SCON | | SC7OFF | | SC6OFF | | SC5OFF | |

**Table 45. Bit Descriptions for the ISCT1 Register**

| Bit Name | Bit No. | Description[1, 2] |
|---|---|---|
| SCON | [7:6] | SC on time. If the SCxOFF time is not disabled and the independent current sink is enabled (Register 0x10), the LED(s) remains on for the time selected (per the following list) and then turns off.<br>00 = 0.2 sec<br>01 = 0.6 sec<br>10 = 0.8 sec<br>11 = 1.2 sec |
| SC7OFF | [5:4] | SC7 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |
| SC6OFF | [3:2] | SC6 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |
| SC5OFF | [1:0] | SC5 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |

[1] An independent sink remains on continuously when SCx_EN = 1 and SCxOFF = 00 (disabled).
[2] To enable multiple independent sinks, set the appropriate SCx_EN bits. To create equivalent blinking and fading sequences, enable all independent sinks in one write cycle to cause a preprogrammed sequence to start simultaneously.

### *Independent Sink Current Time (ISCT2)—Register 0x12*

**Table 46. ISCT2 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| SC4OFF | | SC3OFF | | SC2OFF | | SC1OFF | |

**Table 47. Bit Descriptions for the ISCT2 Register**

| Bit Name | Bit No. | Description[1, 2] |
|---|---|---|
| SC4OFF | [7:6] | SC4 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |
| SC3OFF | [5:4] | SC3 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |
| SC2OFF | [3:2] | SC2 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |
| SC1OFF | [1:0] | SC1 off time. When the SC off time is disabled, the ISC remains on while enabled. When the SC off time is set to any other value, the ISC turns off for the off time (per the following listed times) and then turns on according to the SCON setting.<br>00 = off time disabled<br>01 = 0.6 sec<br>10 = 1.2 sec<br>11 = 1.8 sec |

[1] An independent sink remains on continuously when SCx_EN = 1 and SCxOFF = 00 (disabled).
[2] To enable multiple independent sinks, set the appropriate SCx_EN bits. To create equivalent blinking and fading sequences, enable all independent sinks in one write cycle. This causes a preprogrammed sequence to start simultaneously.

### *Independent Sink Current Fade (ISCF)—Register 0x13*

**Table 48. ISCF Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| SCFO | | | | SCFI | | | |

**Table 49. Bit Descriptions for the ISCF Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| SCFO | [7:4] | Sink current fade out rate. The times listed here are for a full-scale fade out (30 mA to 0 mA). Fades between closer current values reduce the fade time. See the Automated Fade In and Fade Out section for more information.<br>0000 = disabled<br>0001 = 0.30 sec<br>0010 = 0.60 sec<br>0011 = 0.90 sec<br>0100 = 1.2 sec<br>0101 = 1.5 sec<br>0110 = 1.8 sec<br>0111 = 2.1 sec<br>1000 = 2.4 sec<br>1001 = 2.7 sec<br>1010 = 3.0 sec<br>1011 = 3.5 sec<br>1100 = 4.0 sec<br>1101 = 4.5 sec<br>1110 = 5.0 sec<br>1111 = 5.5 sec |
| SCFI | [3:0] | Sink current fade in rate. The times listed here are for a full-scale fade in (0 mA to 30 mA). Fades between closer current values reduce the fade time. See the Automated Fade In and Fade Out section for more information.<br>0000 = disabled<br>0001 = 0.30 sec<br>0010 = 0.60 sec<br>0011 = 0.90 sec<br>0100 = 1.2 sec<br>0101 = 1.5 sec<br>0110 = 1.8 sec<br>0111 = 2.1 sec<br>1000 = 2.4 sec<br>1001 = 2.7 sec<br>1010 = 3.0 sec<br>1011 = 3.5 sec<br>1100 = 4.0 sec<br>1101 = 4.5 sec<br>1110 = 5.0 sec<br>1111 = 5.5 sec |

### *Sink Current Register LED7 (ISC7)—Register 0x14*

**Table 50. ISC7 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| SCR | SCD7 | | | | | | |

**Table 51. Bit Descriptions for the ISC7 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| SCR | 7 | 1 = Sink Current 1.<br>0 = Sink Current 0. | | |
| SCD7 | [6:0] | For Sink Current 0, use the following DAC code schedule (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0.000 | 0 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |
| | | For Sink Current 1, use the following DAC code schedule (see Table 52 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0.000 | 0 |
| | | 0000001 | 0.472 | 0.004 |
| | | 0000010 | 0.945 | 0.014 |
| | | 0000011 | 1.42 | 0.034 |
| | | … | … | … |
| | | 1111111 | 60 | 60 |

**Table 52. Linear and Square Law Currents for LED7 (SCR = 1)**

| DAC Code | Linear Law (mA) | Square Law (mA)[1] | DAC Code | Linear Law (mA) | Square Law (mA)[1] |
|---|---|---|---|---|---|
| 0x00 | 0.000 | 0 | 0x18 | 11.34 | 2.142 |
| 0x01 | 0.472 | 0.004 | 0x19 | 11.81 | 2.326 |
| 0x02 | 0.945 | 0.014 | 0x1A | 12.28 | 2.514 |
| 0x03 | 1.42 | 0.034 | 0x1B | 12.76 | 2.712 |
| 0x04 | 1.89 | 0.06 | 0x1C | 13.23 | 2.916 |
| 0x05 | 2.36 | 0.094 | 0x1D | 13.70 | 3.128 |
| 0x06 | 2.83 | 0.134 | 0x1E | 14.17 | 3.348 |
| 0x07 | 3.31 | 0.182 | 0x1F | 14.65 | 3.574 |
| 0x08 | 3.78 | 0.238 | 0x20 | 15.12 | 3.81 |
| 0x09 | 4.25 | 0.302 | 0x21 | 15.59 | 4.052 |
| 0x0A | 4.72 | 0.372 | 0x22 | 16.06 | 4.3 |
| 0x0B | 5.20 | 0.45 | 0x23 | 16.54 | 4.558 |
| 0x0C | 5.67 | 0.536 | 0x24 | 17.01 | 4.822 |
| 0x0D | 6.14 | 0.628 | 0x25 | 17.48 | 5.092 |
| 0x0E | 6.61 | 0.73 | 0x26 | 17.95 | 5.372 |
| 0x0F | 7.09 | 0.838 | 0x27 | 18.43 | 5.658 |
| 0x10 | 7.56 | 0.952 | 0x28 | 18.90 | 5.952 |
| 0x11 | 8.03 | 1.076 | 0x29 | 19.37 | 6.254 |
| 0x12 | 8.50 | 1.206 | 0x2A | 19.84 | 6.562 |
| 0x13 | 8.98 | 1.342 | 0x2B | 20.31 | 6.878 |
| 0x14 | 9.45 | 1.488 | 0x2C | 20.79 | 7.202 |
| 0x15 | 9.92 | 1.64 | 0x2D | 21.26 | 7.534 |
| 0x16 | 10.39 | 1.8 | 0x2E | 21.73 | 7.872 |
| 0x17 | 10.87 | 1.968 | 0x2F | 22.20 | 8.218 |

| DAC Code | Linear Law (mA) | Square Law (mA)[1] |
|---|---|---|
| 0x30 | 22.68 | 8.57 |
| 0x31 | 23.15 | 8.932 |
| 0x32 | 23.62 | 9.3 |
| 0x33 | 24.09 | 9.676 |
| 0x34 | 24.57 | 10.058 |
| 0x35 | 25.04 | 10.45 |
| 0x36 | 25.51 | 10.848 |
| 0x37 | 25.98 | 11.254 |
| 0x38 | 26.46 | 11.666 |
| 0x39 | 26.93 | 12.086 |
| 0x3A | 27.40 | 12.514 |
| 0x3B | 27.87 | 12.95 |
| 0x3C | 28.35 | 13.392 |
| 0x3D | 28.82 | 13.842 |
| 0x3E | 29.29 | 14.3 |
| 0x3F | 29.76 | 14.764 |
| 0x40 | 30.24 | 15.238 |
| 0x41 | 30.71 | 15.718 |
| 0x42 | 31.18 | 16.204 |
| 0x43 | 31.65 | 16.7 |
| 0x44 | 32.13 | 17.202 |
| 0x45 | 32.60 | 17.71 |
| 0x46 | 33.07 | 18.228 |
| 0x47 | 33.54 | 18.752 |
| 0x48 | 34.02 | 19.284 |
| 0x49 | 34.49 | 19.824 |
| 0x4A | 34.96 | 20.37 |
| 0x4B | 35.43 | 20.926 |
| 0x4C | 35.91 | 21.486 |
| 0x4D | 36.38 | 22.056 |
| 0x4E | 36.85 | 22.632 |
| 0x4F | 37.32 | 23.216 |
| 0x50 | 37.80 | 23.808 |
| 0x51 | 38.27 | 24.406 |
| 0x52 | 38.74 | 25.014 |
| 0x53 | 39.21 | 25.628 |
| 0x54 | 39.69 | 26.248 |
| 0x55 | 40.16 | 26.878 |
| 0x56 | 40.63 | 27.514 |
| 0x57 | 41.10 | 28.156 |
| 0x58 | 41.57 | 28.808 |
| 0x59 | 42.05 | 29.466 |
| 0x5A | 42.52 | 30.132 |
| 0x5B | 42.99 | 30.806 |
| 0x5C | 43.46 | 31.486 |
| 0x5D | 43.94 | 32.174 |
| 0x5E | 44.41 | 32.87 |
| 0x5F | 44.88 | 33.574 |
| 0x60 | 45.35 | 34.284 |
| 0x61 | 45.83 | 35.002 |
| 0x62 | 46.30 | 35.726 |
| 0x63 | 46.77 | 36.46 |
| 0x64 | 47.24 | 37.2 |
| 0x65 | 47.72 | 37.948 |
| 0x66 | 48.19 | 38.702 |
| 0x67 | 48.66 | 39.466 |
| 0x68 | 49.13 | 40.236 |
| 0x69 | 49.61 | 41.014 |
| 0x6A | 50.08 | 41.798 |
| 0x6B | 50.55 | 42.59 |
| 0x6C | 51.02 | 43.39 |
| 0x6D | 51.50 | 44.198 |
| 0x6E | 51.97 | 45.012 |
| 0x6F | 52.44 | 45.834 |
| 0x70 | 52.91 | 46.664 |
| 0x71 | 53.39 | 47.5 |
| 0x72 | 53.86 | 48.346 |
| 0x73 | 54.33 | 49.198 |
| 0x74 | 54.80 | 50.056 |
| 0x75 | 55.28 | 50.924 |
| 0x76 | 55.75 | 51.798 |
| 0x77 | 56.22 | 52.68 |
| 0x78 | 56.69 | 53.568 |
| 0x79 | 57.17 | 54.464 |
| 0x7A | 57.64 | 55.368 |
| 0x7B | 58.11 | 56.28 |
| 0x7C | 58.58 | 57.198 |
| 0x7D | 59.06 | 58.126 |
| 0x7E | 59.53 | 59.058 |
| 0x7F | 60 | 60 |

[1] Cubic 10 and Cubic 11 laws use the square law DAC setting but vary the time step per DAC code (see the Automated Fade In and Fade Out section).

### *Sink Current Register LED6 (ISC6)—Register 0x15*

**Table 53. ISC6 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SCD6 | | | | | | |

**Table 54. Bit Descriptions for the ISC6 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| SCD6 | [6:0] | Sink current. Use the following DAC code schedule (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Sink Current Register LED5 (ISC5)—Register 0x16*

**Table 55. ISC5 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SCD5 | | | | | | |

**Table 56. Bit Descriptions for the ISC5 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| SCD5 | [6:0] | Sink current. Use the following DAC code schedule (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Sink Current Register LED4 (ISC4)—Register 0x17*

**Table 57. ISC4 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SCD4 | | | | | | |

**Table 58. Bit Descriptions for the ISC4 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| SCD4 | [6:0] | Sink current. Use the following DAC code schedule (see Table 29 for a complete list of values): | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Sink Current Register LED3 (ISC3)—Register 0x18*

**Table 59. ISC3 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SCD3 | | | | | | |

**Table 60. Bit Descriptions for the ISC3 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| SCD3 | [6:0] | Sink current. Use the following DAC code schedule (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Sink Current Register LED2 (ISC2)—Register 0x19*

**Table 61. ISC2 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SCD2 | | | | | | |

**Table 62. Bit Descriptions for the ISC2 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| SCD2 | [6:0] | Sink current. Use the following DAC code schedule (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

### *Sink Current Register LED1 (ISC1)—Register 0x1A*

**Table 63. ISC1 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | SCD1 | | | | | | |

**Table 64. Bit Descriptions for the ISC1 Register**

| Bit Name | Bit No. | Description | | |
|---|---|---|---|---|
| N/A | 7 | Reserved. | | |
| SCD1 | [6:0] | Sink current. Use the following DAC code schedule (see Table 29 for a complete list of values). | | |
| | | **DAC** | **Linear Law (mA)** | **Square Law (mA)** |
| | | 0000000 | 0 | 0.000 |
| | | 0000001 | 0.236 | 0.002 |
| | | 0000010 | 0.472 | 0.007 |
| | | 0000011 | 0.709 | 0.017 |
| | | … | … | … |
| | | 1111111 | 30 | 30 |

## COMPARATOR REGISTER DESCRIPTIONS

### *Comparator Configuration (CCFG)—Register 0x1B*

**Table 65. CCFG Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| FILT | | | FORCE_RD | L3_OUT | L2_OUT | L3_EN | L2_EN |

**Table 66. Bit Descriptions for the CCFG Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| FILT | [7:5] | Filter setting for the CMP_IN light sensor.<br>000 = 80 ms<br>001 = 160 ms<br>010 = 320 ms<br>011 = 640 ms<br>100 = 1280 ms<br>101 = 2560 ms<br>110 = 5120 ms<br>111 = 10,240 ms |
| FORCE_RD | 4 | Force a read of the CMP_IN light sensor while independent sinks are running, but the backlight is not. Reset by chip after the conversion is complete and L2_OUT and L3_OUT are valid. Ignored if the backlight is enabled. |
| L3_OUT | 3 | This bit is the output of the L3 comparator. |
| L2_OUT | 2 | This bit is the output of the L2 comparator. |
| L3_EN | 1 | 1 = the L3 comparator is enabled for the CMP_IN comparator.<br>0 = the L3 comparator is disabled for the CMP_IN comparator. |
| L2_EN | 0 | Note that the L3 comparator has priority over the L2 comparator.<br>1 = the L2 comparator is enabled for the CMP_IN comparator.<br>0 = the L2 comparator is disabled for the CMP_IN comparator. |

### *Second Comparator Configuration (CCFG2)—Register 0x1C*

**Table 67. CCFG2 Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| FILT2 | | | FORCE_RD2 | L3_OUT2 | L2_OUT2 | L3_EN2 | L2_EN2 |

**Table 68. Bit Descriptions for the CCFG2 Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| FILT2 | [7:5] | Filter setting for the CMP_IN2 light sensor.<br>000 = 80 ms<br>001 = 160 ms<br>010 = 320 ms<br>011 = 640 ms<br>100 = 1280 ms<br>101 = 2560 ms<br>110 = 5120 ms<br>111= 10,240 ms |
| FORCE_RD2 | 4 | Force a read of the CMP_IN2 light sensor while independent sinks are running, but the backlight is not. Reset by chip after the conversion is complete and L2_OUT and L3_OUT are valid. Ignored if backlight is enabled. |
| L3_OUT2 | 3 | This bit is the output of the L3 comparator for the second light sensor. |
| L2_OUT2 | 2 | This bit is the output of the L2 comparator for the second light sensor. |
| L3_EN2 | 1 | 1 = the L3 comparator is enabled for the CMP_IN2 comparator.<br>0 = the L3 comparator is disabled for the CMP_IN2 comparator. |
| L2_EN2 | 0 | Note that the L3 comparator has priority over the L2 comparator.<br>1 = the L2 comparator is enabled for the CMP_IN2 comparator.<br>0 = the L2 comparator is disabled for the CMP_IN2 comparator. |

### *Comparator Level 2 Threshold (L2_TRP)—Register 0x1D*

**Table 69. L2_TRP Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| L2_TRP | | | | | | | |

**Table 70. Bit Descriptions for the L2_TRP Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| L2_TRP | [7:0] | Comparator Level 2 threshold. If the comparator input is below L2_TRP, the comparator trips and the backlight enters Level 2 (office) mode. The following lists the code settings for the photosensor current:<br>00000000 = 0 µA<br>00000001 = 4.3 µA<br>00000010 = 8.6 µA<br>00000011 = 12.9 µA<br>…<br>11111010 = 1080 µA<br>…<br>11111111 = 1106 µA<br>Although codes above 1111010 (250 decimal) are possible, they should not be used. Furthermore, the maximum value of L2_TRP + L2_HYS must not exceed 11111010 (250). |

### *Comparator Level 2 Hysteresis (L2_HYS)—Register 0x1E*

**Table 71. L2_HYS Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| L2_HYS | | | | | | | |

**Table 72. Bit Descriptions for the L2_HYS Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| L2_HYS | [7:0] | Comparator Level 2 hysteresis. If the comparator input is above L2_TRP + L2_HYS, the comparator trips and the backlight enters Level 1 (daylight) mode. The following lists the code settings for the photosensor current hysteresis:<br>00000000 = 0 µA<br>00000001 = 4.3 µA<br>00000010 = 8.6 µA<br>00000011 = 12.9 µA<br>…<br>11111010 = 1080 µA<br>…<br>11111111 = 1106 µA<br><br>Although codes above 11111010 (250 decimal) are possible, they should not be used. Furthermore, the maximum value of L2_TRP + L2_HYS must not exceed 11111010 (250). |

### *Comparator Level 3 Threshold (L3_TRP)—Register 0x1F*

**Table 73. L3_TRP Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| L3_TRP | | | | | | | |

**Table 74. Bit Descriptions for the L3_TRP Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| L3_TRP | 7:0 | Comparator Level 3 threshold. If the comparator input is below L3_TRP, the comparator trips and the backlight enters Level 3 (dark) mode. The following lists the code settings for photosensor current:<br>00000000 = 0 µA<br>00000001 = 0.54 µA<br>00000010 = 1.08 µA<br>00000011 = 1.62 µA<br>…<br>11111111 = 137.7 µA |

### *Comparator Level 3 Hysteresis (L3_HYS)—Register 0x20*

**Table 75. L3_HYS Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| L3_HYS | | | | | | | |

**Table 76. Bit Descriptions for the L3_HYS Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| L3_HYS | [7:0] | Comparator Level 3 hysteresis. If the comparator input is above L3_TRP + L3_HYS, the comparator trips and the backlight enters Level 2 (office) mode. The following lists the code settings for photosensor current hysteresis:<br>00000000 = 0 µA<br>00000001 = 0.54 µA<br>00000010 = 1.08 µA<br>00000011 = 1.62 µA<br>…<br>11111111 = 137.7 µA |

### *First Phototransistor Register: Low Byte (PH1LEVL)—Register 0x21*

**Table 77. PH1LEVL Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| PH1LEV_LOW | | | | | | | |

**Table 78. Bit Descriptions for the PH1LEVL Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| PH1LEV_LOW | [7:0] | Lower eight bits of the 13-bit conversion value for the first light sensor (Bit 7 to Bit 0). The value is updated every 80 ms (when the light sensor is enabled). This is a read-only register. |

### *First Phototransistor Register: High Byte (PH1LEVH)—Register 0x22*

**Table 79. PH1LEVH Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | PH1LEV_HIGH | | | | |

**Table 80. Bit Descriptions for the PH1LEVH Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | [7:5] | Reserved. |
| PH1LEV_HIGH | [4:0] | Upper five bits of the 13-bit conversion value for the first light sensor (Bit 12 to Bit 8). The value is updated every 80 ms (when the light sensor is enabled). This is a read-only register. |

### *Second Phototransistor Register: Low Byte (PH2LEVL)—Register 0x23*

**Table 81. PH2LEVL Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| PH2LEV_LOW | | | | | | | |

**Table 82. Bit Descriptions for the PH2LEVL Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| PH2LEV_LOW | [7:0] | Lower eight bits of the 13-bit conversion value for the second light sensor (Bit 7 to Bit 0). The value is updated every 80 ms (when the light sensor is enabled). This is a read-only register. |

### *Second Phototransistor Register: High Byte (PH2LEVH)—Register 0x24*

**Table 83. PH2LEVH Bit Map**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | PH2LEV_HIGH | | | | |

**Table 84. Bit Descriptions for the PH2LEVH Register**

| Bit Name | Bit No. | Description |
|---|---|---|
| N/A | [7:5] | Reserved |
| PH2LEV_HIGH | [4:0] | Upper five bits of the 13-bit conversion value for the second light sensor (Bit 12 to Bit 8). The value is updated every 80 ms (when the light sensor is enabled). This is a read-only register. |

# OUTLINE DIMENSIONS

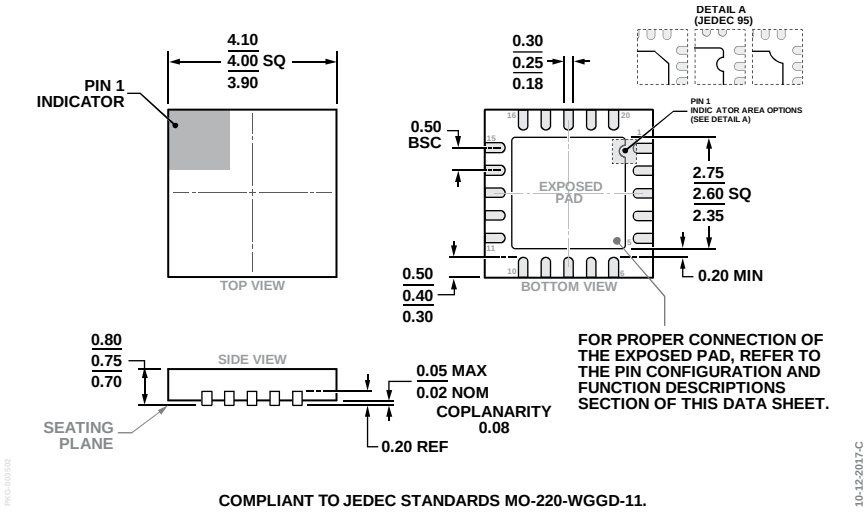


*Figure 51. 20-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-20-8)*
*Dimensions shown in millimeters*

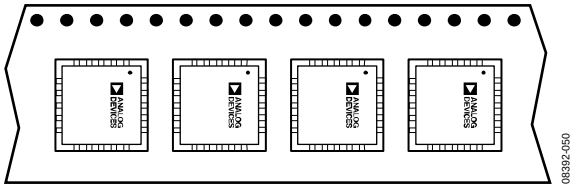


*Figure 52. Tape and Reel Orientation for LFCSP Units*

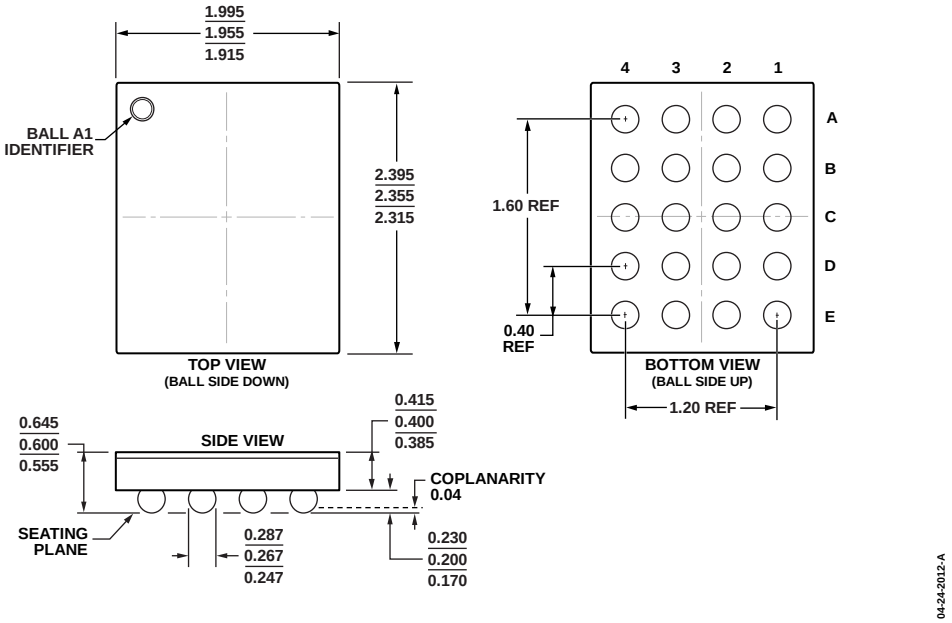


*Figure 53. 20-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-20-6)*
*Dimensions shown in millimeters*

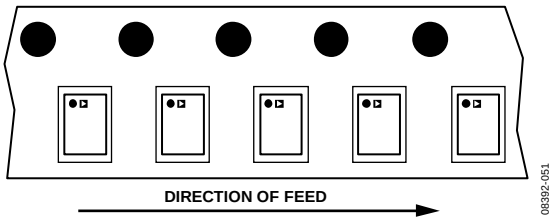


*Figure 54. Tape and Reel Orientation for WLCSP Units*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADP8863ACPZ-R7 | −40°C to +85°C | 20-Lead LFCSP, 7″ Tape and Reel | CP-20-8 |
| ADP8863ACBZ-R7 | −40°C to +85°C | 20-Ball WLCSP, 7″ Tape and Reel | CB-20-6 |

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).