ANALOG DEVICES

HMC1049LP5E

v01.1213

RoHS ✓ EARTH FRIENDLY

GaAs pHEMT MMIC LOW NOISE AMPLIFIER, 0.3 - 20 GHz

Typical Applications

The HMC1049LP5E is ideal for:

- Test Instrumentation
- High Linearity Microwave Radios
- VSAT & SATCOM
- Military & Space

Features

Noise Figure: 1.8 dB

P1dB Output Power: +14.5 dBm

Psat Output Power: +17.5 dBm

High Gain: 15 dB

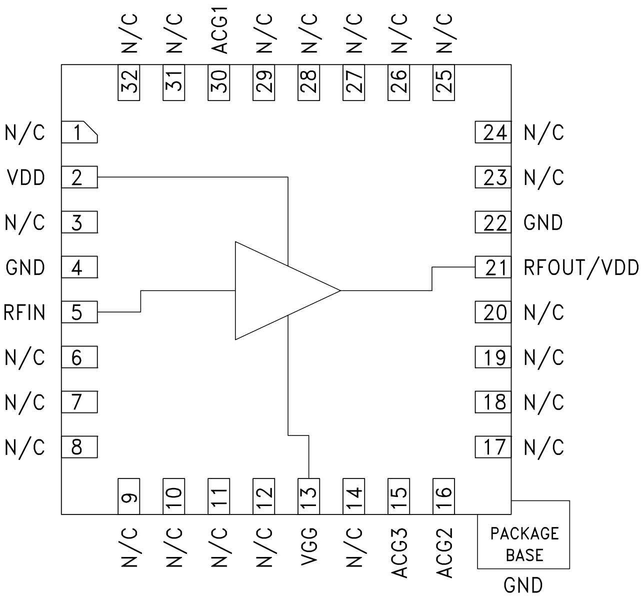
Output IP3: +29 dBm

Supply Voltage: Vdd = +7V @ 70 mA

50 Ohm Matched Input/Output

32 Lead 5x5 mm SMT Package: 25mm^2

Functional Diagram



General Description

The HMC1049LP5E is a GaAs MMIC Low Noise Amplifier which operates between 0.3 and 20 GHz. This LNA provides 15 dB of small signal gain, 1.8 dB noise figure, and output IP3 of 29 dBm, while requiring only 70 mA from a +7 V supply. The P1dB output power of 14.5 dBm enables the LNA to function as a LO driver for balanced, I/Q or image reject mixers. Vdd can be applied to pin 2 or pin 21. Pin 21 will require a bias tee. The HMC1049LP5E amplifier I/Os are internally matched to 50 Ohms and the device is supplied in a compact, leadless QFN 5x5 mm surface mount package.

Electrical Specifications, T_A = +25° C, Vdd = +7V, Idd = 70 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		0.3 - 1			1 - 14			14 - 20		GHz
Gain	13.5	16.5		12	15		10	13		dB
Gain Variation Over Temperature		0.006			0.019			0.017		dB/°C
Noise Figure		2.5	3.5		1.8	2.5		2.7	4.0	dB
Input Return Loss		15			13			14		dB
Output Return Loss		8			15			13		dB
Output Power for 1 dB Compression (P1dB)		15			14.5			13		dBm
Saturated Output Power (Psat)		18			17.5			16		dBm
Output Third Order Intercept (IP3) [2]		31			29			26		dBm
Total Supply Current		70			70			70		mA

[1] Adjust Vgg between -2 to 0V to achieve Idd = 70 mA typical.
[2] Measurement taken at Pout / tone = +8 dBm.

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Application Support: Phone: 1-800-ANALOG-D*

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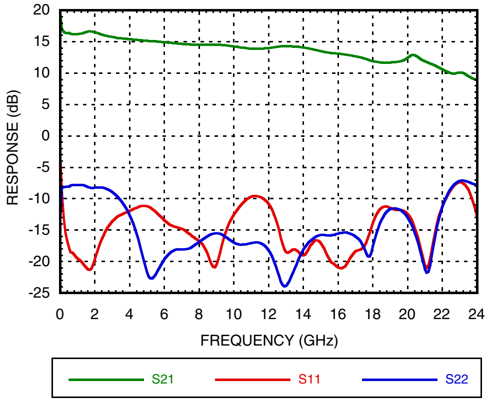
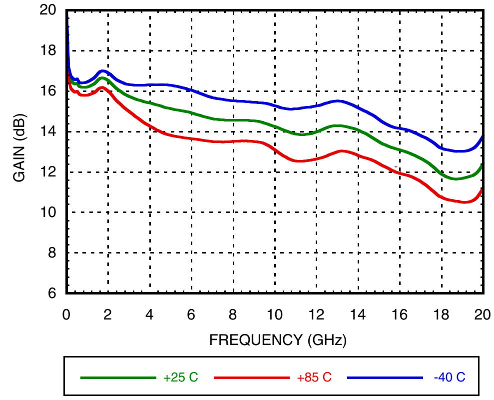
Data taken with Vdd applied to pin 2.

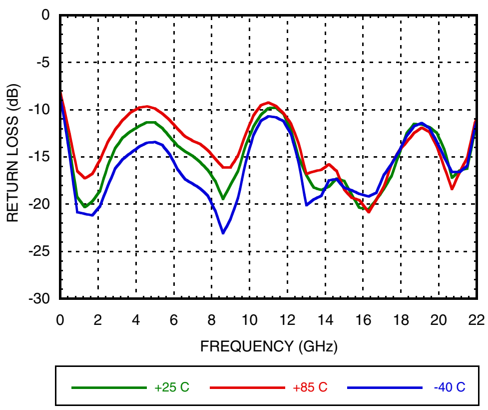
Broadband Gain & Return Loss



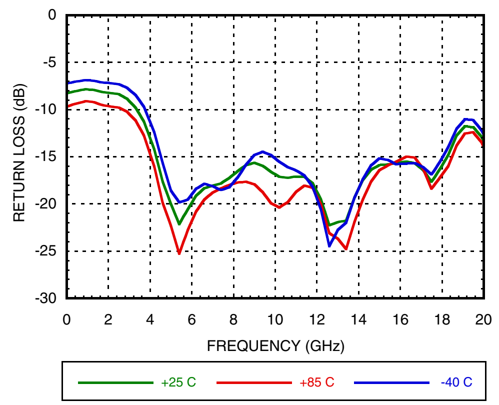
Gain vs. Temperature



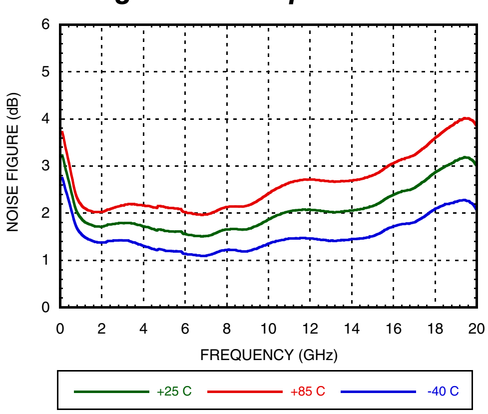
Input Return Loss vs. Temperature



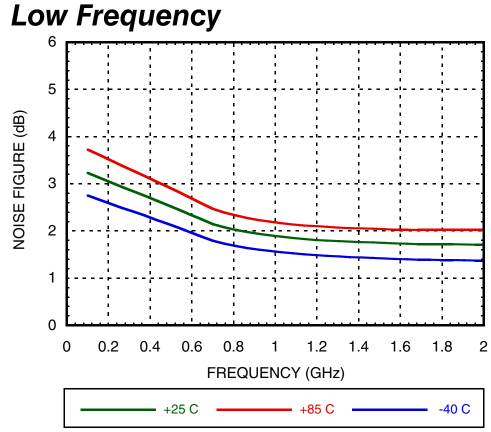
Output Return Loss vs. Temperature



Noise Figure vs. Temperature



Noise Figure vs. Temperature, Low Frequency



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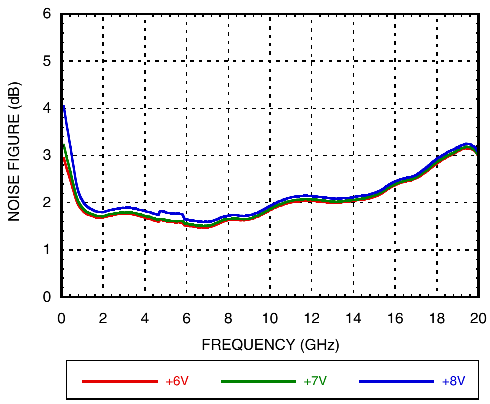
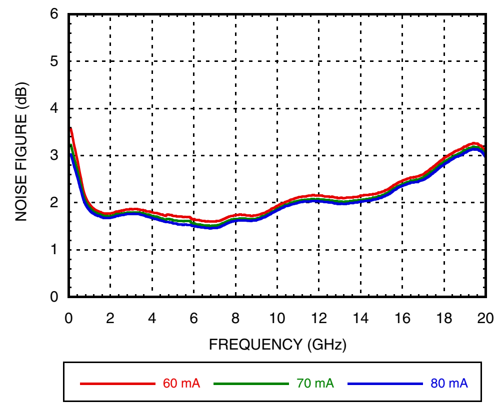
Data taken with Vdd applied to pin 2.

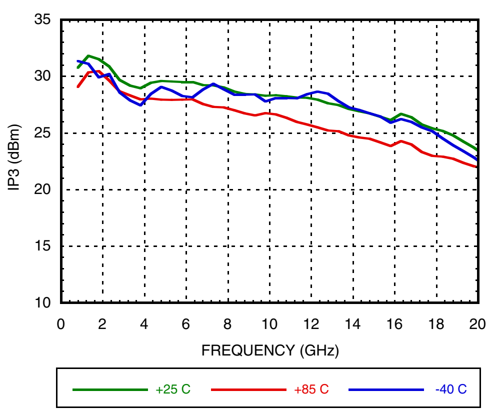
Noise Figure vs. Vdd



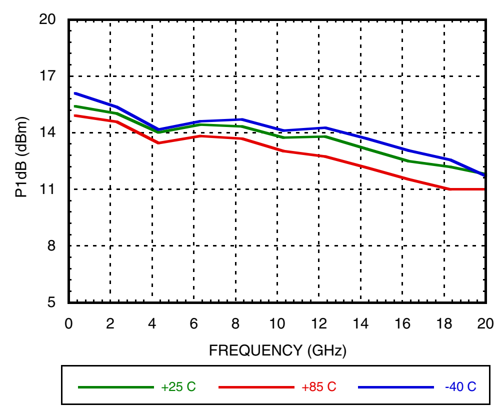
Noise Figure vs. Idd



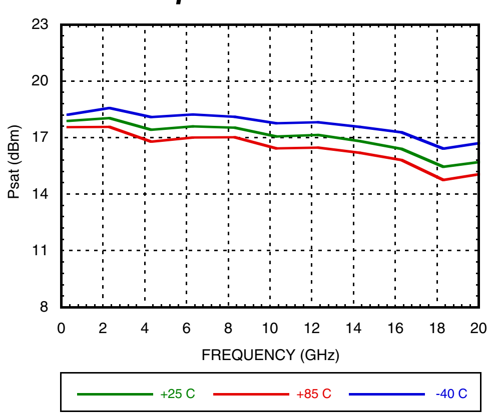
Output IP3 vs. Temperature



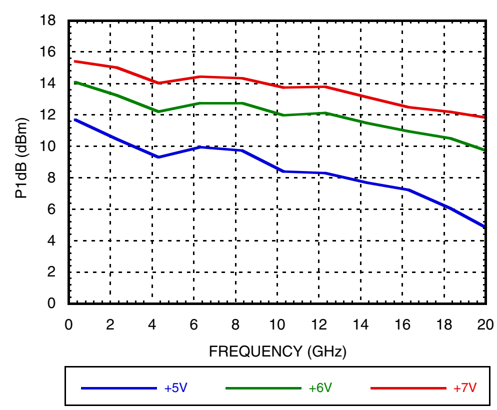
P1dB vs. Temperature



Psat vs. Temperature



P1dB vs. Vdd



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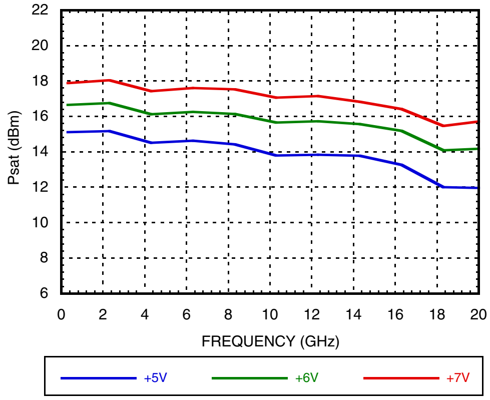
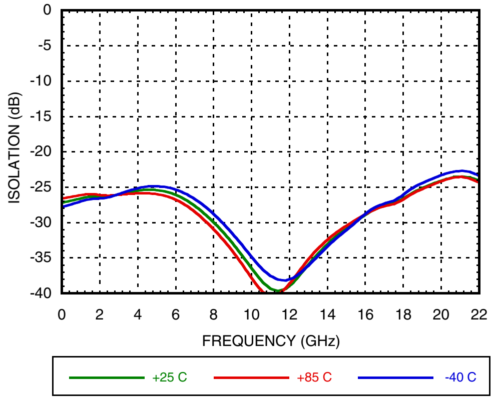
Data taken with Vdd applied to pin 2.

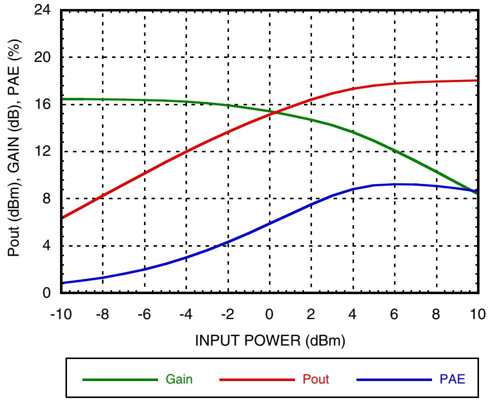
Psat vs. Vdd



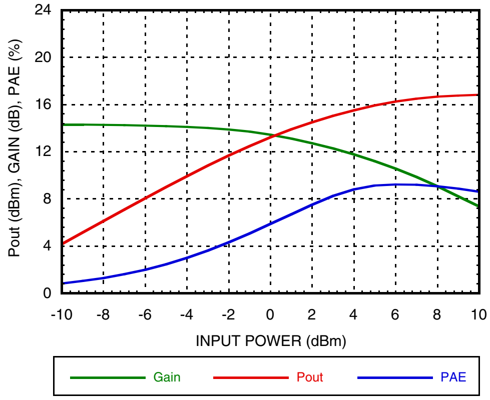
Reverse Isolation vs. Temperature



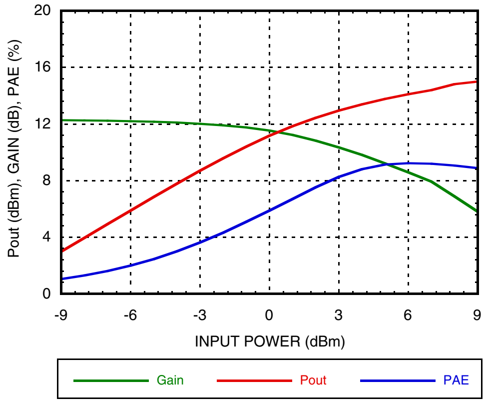
Power Compression @ 2 GHz



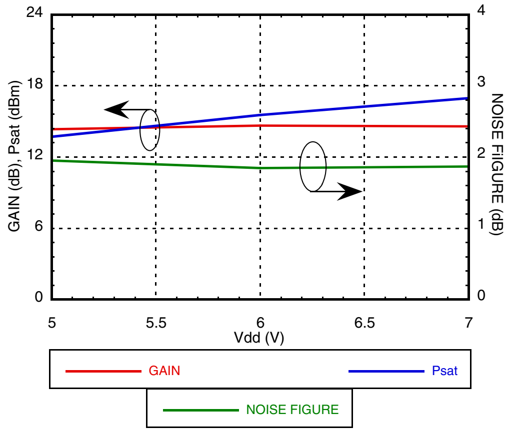
Power Compression @ 10 GHz



Power Compression @ 18 GHz

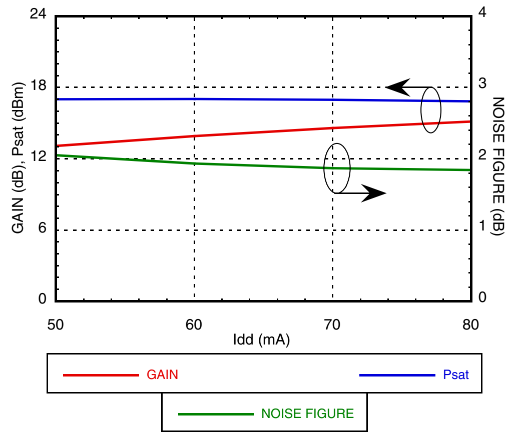


Noise Figure, Gain & Power vs. Supply Voltage @ 12 GHz



Data taken with Vdd applied to pin 2.

Noise Figure, Gain & Power vs. Supply Current @ 12 GHz



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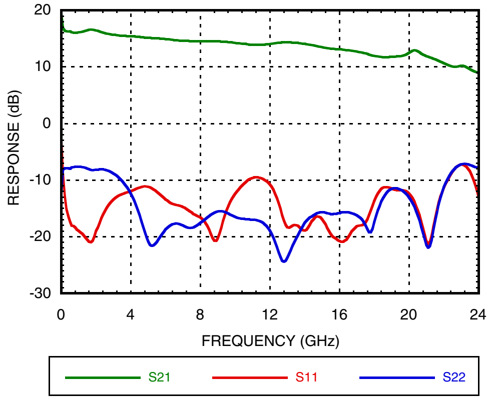
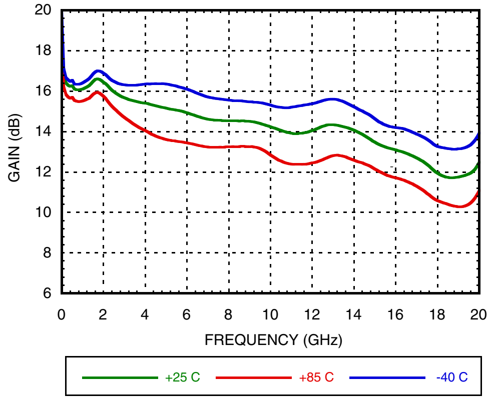
Data taken with Vdd applied to bias tee at pin 21.

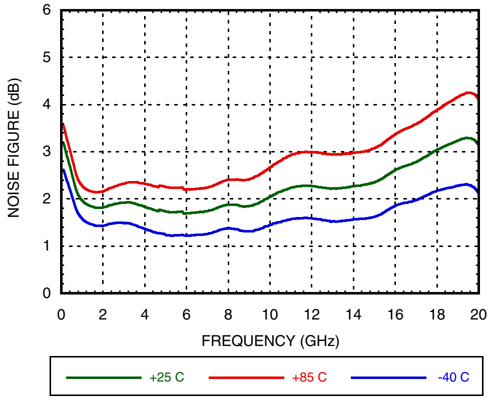
Broadband Gain & Return Loss [1]



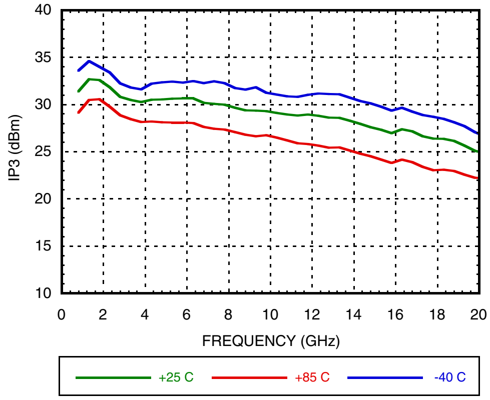
Gain vs. Temperature [1]



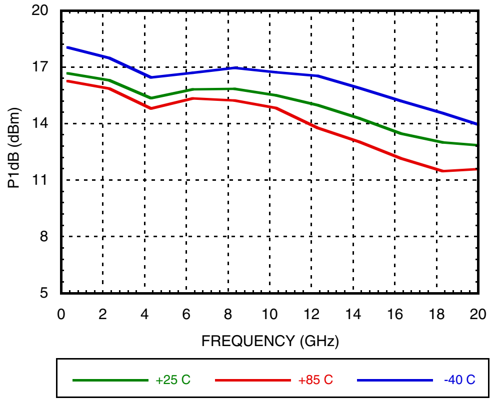
Noise Figure vs. Temperature [1]



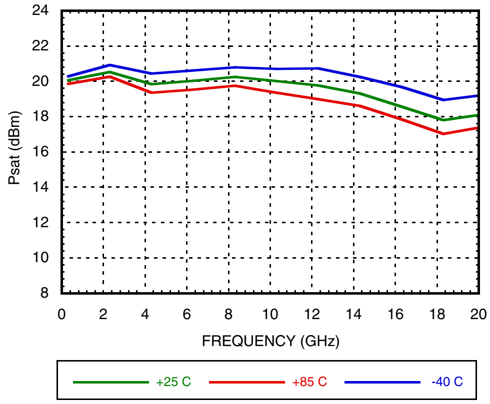
Output IP3 vs. Temperature [1]



P1dB vs. Temperature [1]



Psat vs. Temperature [1]



[1] Vdd= +4V, supply to bias tee.

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Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+10V
Drain Bias Voltage (RF out / Vdd)	+7V
RF Input Power	+18 dBm
Gate Bias Voltage, Vgg1	-2V to +0.2V
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 37.1 mW/°C above 85 °C)	3.34 W
Thermal Resistance (Channel to die bottom)	26.9 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

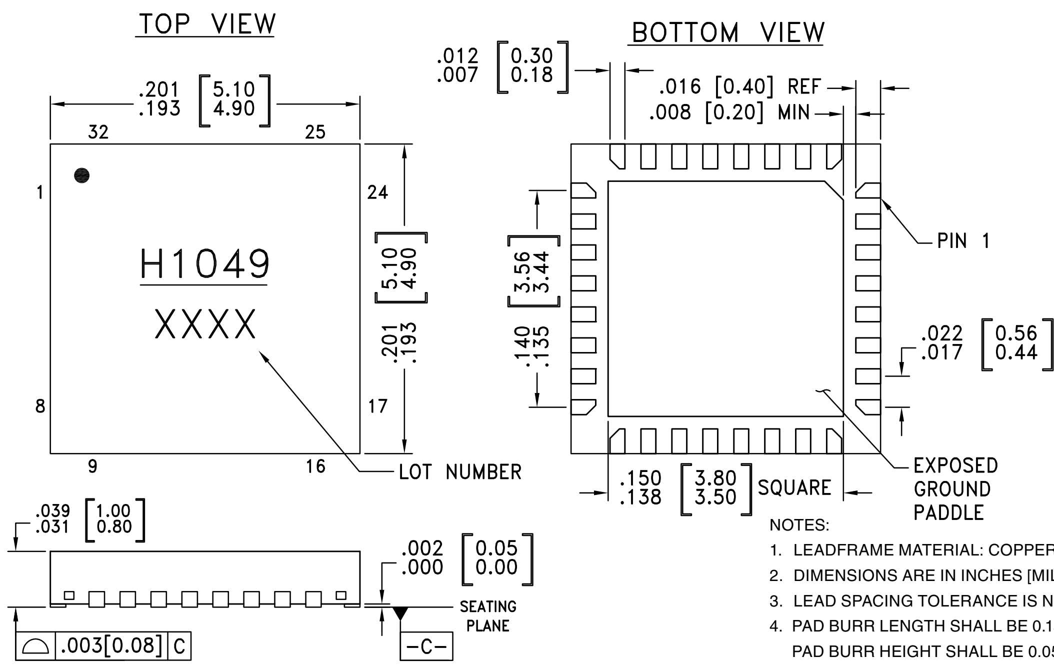
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+5	70
+6	70
+7	70

Adjust Vgg1 to achieve Idd = 70 mA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC1049LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1049 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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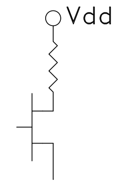
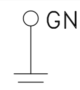
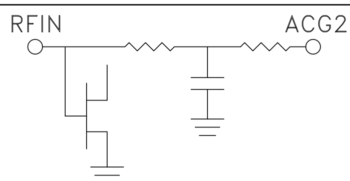
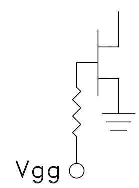
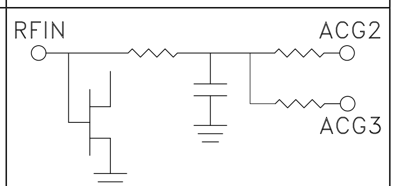
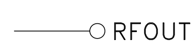
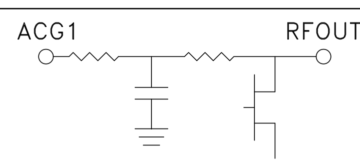
Pin Descriptions

Pad Number	Function	Description	Interface Schematic
1, 3, 6-12, 14, 17-20, 23-29, 31, 32	N/C	No connection required. The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2	Vdd	Power supply voltage for the amplifier. External bypass capacitors 100 pF, and 0.01 uF are required.	
4, 22	GND	These pins and the exposed ground paddle must be connected to RF/DC ground.	
5	RFIN	This pin is DC coupled and matched to 50 Ohms.	
13	Vgg	Gate control for amplifier. External bypass capacitors 100 pF, 0.01uF, and 4.7 uF are required. Adjust voltage to achieve typical Idd.	
15, 16	ACG3, ACG2	Low frequency termination. External bypass capacitors 100 pF are required.	
21	RFOUT/Vdd	This pin is DC coupled and matched to 50 Ohms.	
30	ACG1	Low frequency termination. External bypass capacitor 100 pF required.	

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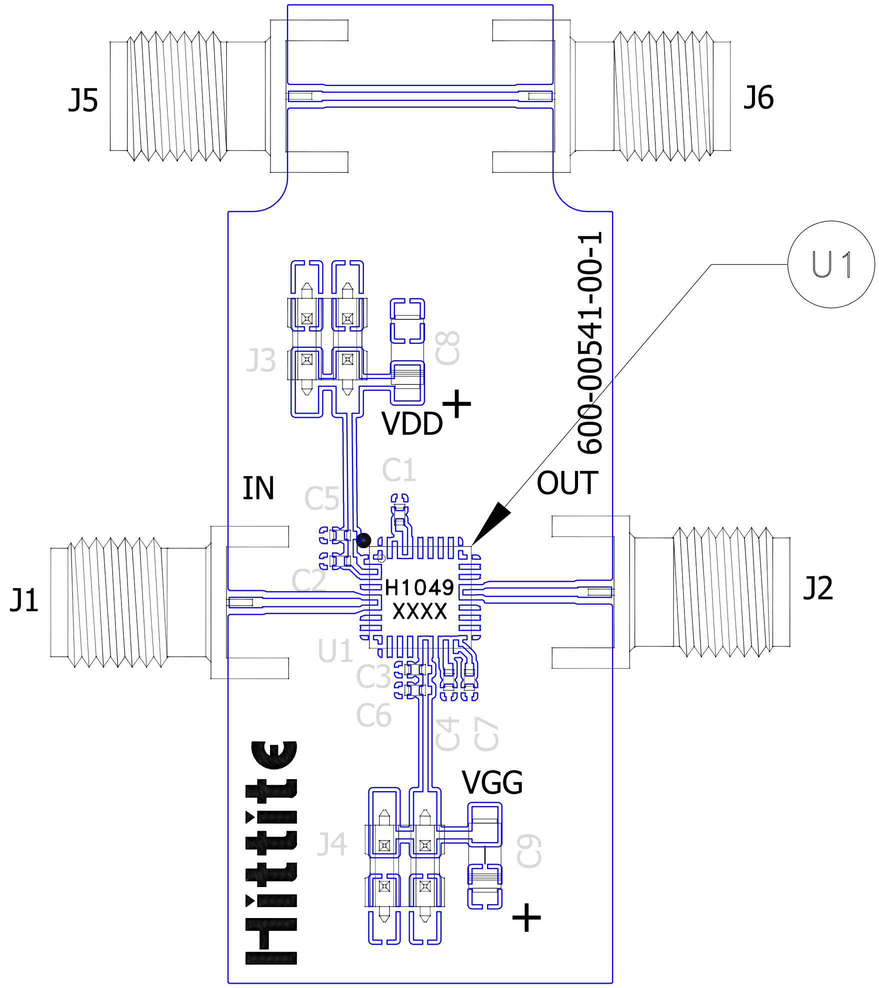
Evaluation PCB



List of Materials for Evaluation PCB EV1HMC1049LP5 [1]

Item	Description
J1, J2, J5, J6	PCB Mount SMA RF Connector.
J3, J4	DC Pins.
C1 - C4	100 pF Capacitor, 0402 Pkg.
C5 - C7	10000 pF Capacitor, 0402 Pkg.
C8 - C9	4.7 uF Capacitor, Tantalum.
U1	HMC1049LP5E.
PCB [1]	600-00541-00-1 Evaluation PCB.

[1] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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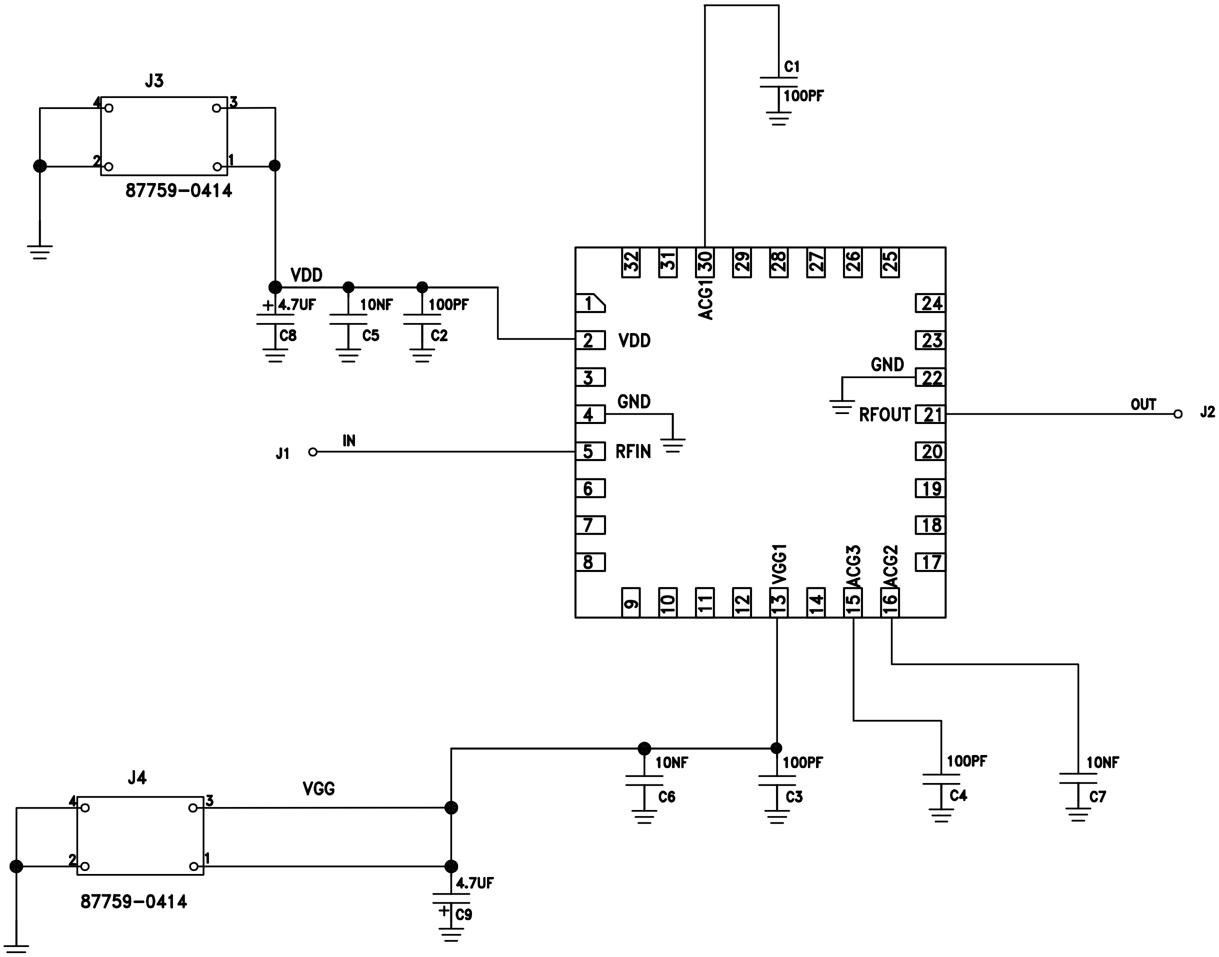
Evaluation PCB Schematic



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