# HMC544 / 544E

v00.0206

## GaAs MMIC T/R SWITCH, DC - 4 GHz

### Typical Applications

The HMC544 / HMC544E is ideal for:

- Cellular/PCS/3G Infrastructure
- Basestations & Repeaters
- WLAN, WiMAX and WiBro
- Microwave and Fixed Wireless Radios

### Features

Very Low Insertion Loss: 0.2 dB @ 1.0 GHz

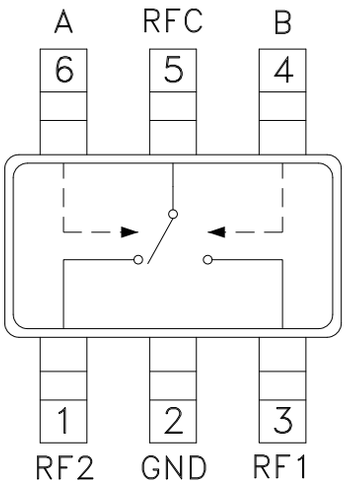
High Input P1dB: +39 dBm

High Input IP3: +55 dBm

Positive Control: 0/+3V to 0/+5V

Compact SOT26 SMT Package

### Functional Diagram




### General Description

The HMC544 & HMC544E are low cost SPDT switches in 6-lead SOT26 packages for use in transmit-receive applications which require very low insertion loss at medium power levels. These devices can control signals from DC to 4.0 GHz and are especially suited for 450, 900, 1900, 2300, and 2700 MHz applications with <0.5 dB insertion loss. This GaAs PHEMT design provides exceptional linearity performance of +36 dBm 1dB compression point and +55 dBm third order intercept at +3 volt bias. RF1 and RF2 are reflective opens when "Off". On-chip circuitry allows positive control operation at very low DC current.

### Electrical Specifications, $T_A$ = +25° C, Vctl = 0/+3 Vdc, 50 Ohm System

| Parameter | Frequency | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Insertion Loss | DC - 1.0 GHz<br>DC - 2.5 GHz<br>DC - 3.0 GHz<br>DC - 4.0 GHz | | 0.25<br>0.4<br>0.5<br>0.7 | 0.5<br>0.7<br>0.8<br>1.0 | dB<br>dB<br>dB<br>dB |
| Isolation | DC - 1.0 GHz<br>DC - 2.5 GHz<br>DC - 3.0 GHz<br>DC - 4.0 GHz | 18<br>10<br>9<br>8 | 23<br>14<br>13<br>12 | | dB<br>dB<br>dB<br>dB |
| Return Loss | DC - 4.0 GHz | | 32 | | dB |
| Input Power for 1 dB Compression 0/+5V Control<br>0/+3V Control | 0.3 - 4.0 GHz | 36<br>33 | 39<br>36 | | dBm<br>dBm |
| Input Third Order Intercept<br>(Two-Tone Input Power = +27 dBm Each Tone) | 0.3 - 4.0 GHz | | 55 | | dBm |
| Switching Characteristics<br>tRISE, tFALL (10/90% RF)<br>tON, tOFF (50% CTL to 10/90% RF) | DC - 4.0 GHz | | <br>70<br>140 | | <br>ns<br>ns |



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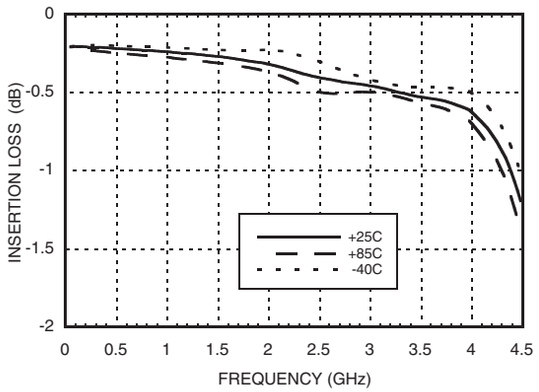
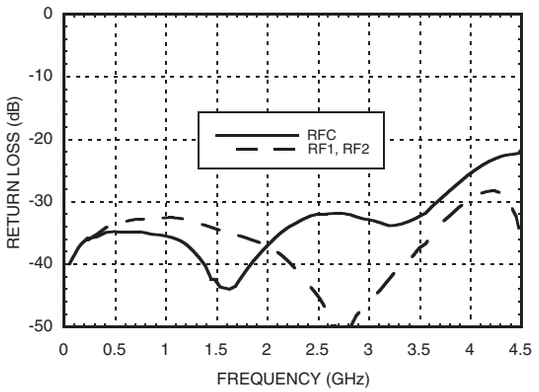
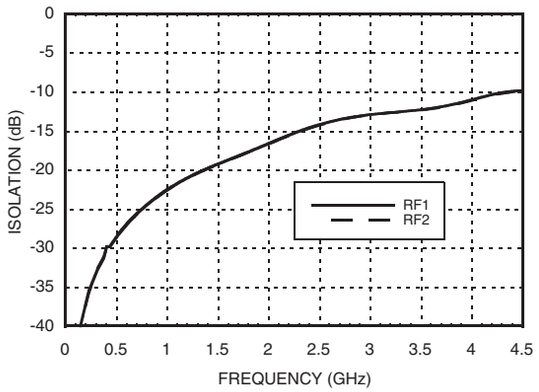
### Insertion Loss



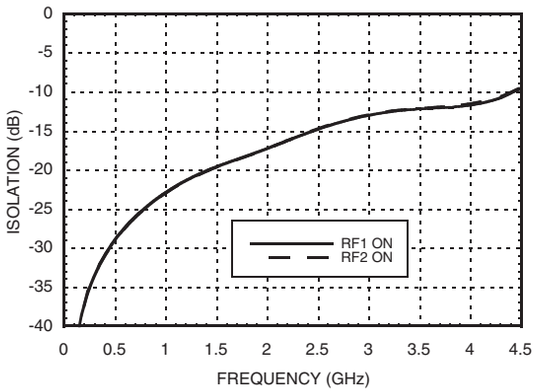

### Return Loss



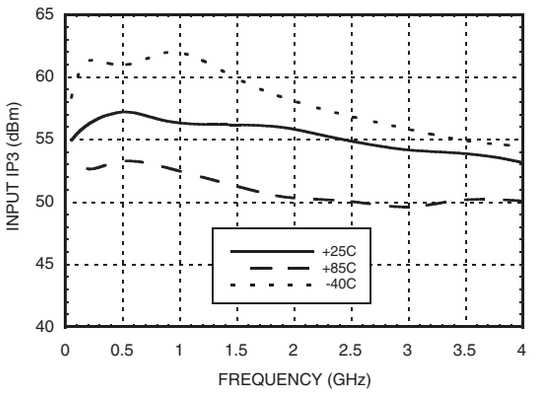

### Isolation Between Ports RFC & RF1 / RF2



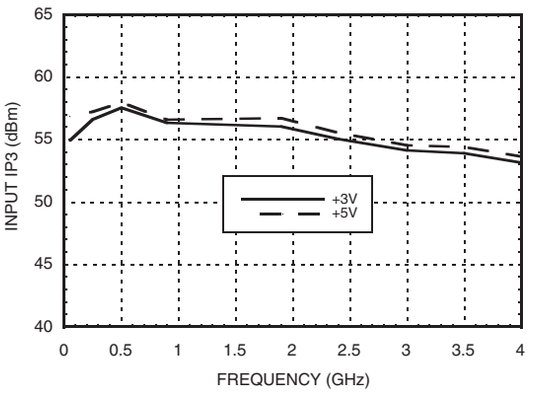

### Isolation Between Ports RF1 & RF2




### Input IP3 vs. Temperature, Vctl = 0/+3V




### Input IP3 vs. Vctl





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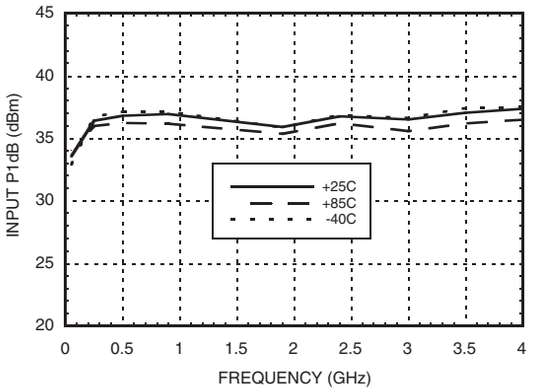
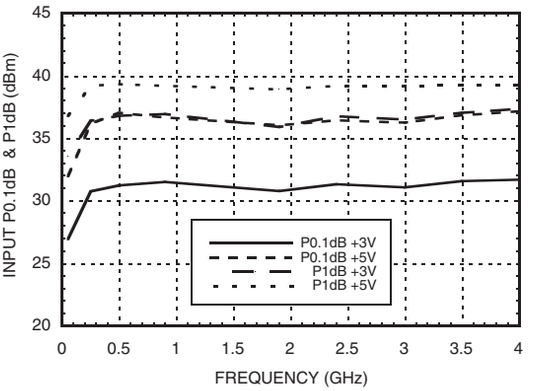
### Input P1dB vs. Temperature, Vctl = 0/+3V




### Compression vs. Vctl




### Truth Table

| Control Input | | Signal Path | |
|---|---|---|---|
| A | B | RFC to RF1 | RFC to RF2 |
| Low | High | On | Off |
| High | Low | Off | On |

### Control Voltages

| State | Bias Condition |
|---|---|
| Low | 0 to 0.2 Vdc @ 1 µA Typical |
| High | +3 Vdc @ 0.5 µA Typical to +5 Vdc @ 2 µA Typical (±0.2 Vdc) |





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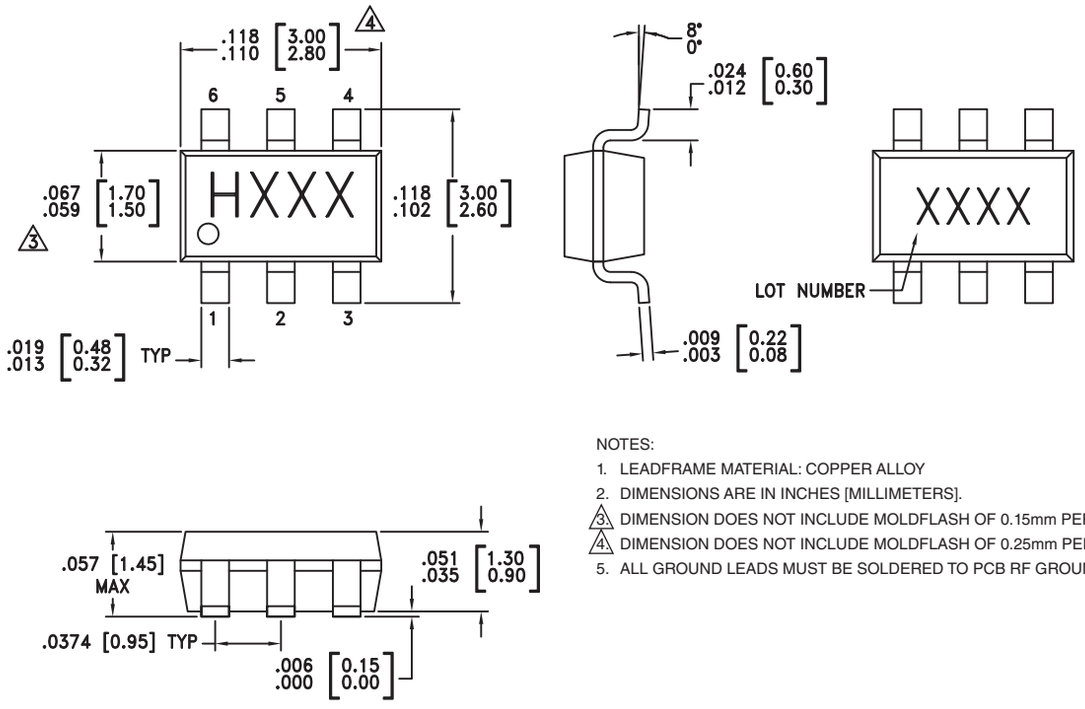
## Absolute Maximum Ratings

| | |
|---|---|
| RF Input Power (Vctl = 0/+5V) | +39 dBm |
| Control Voltage Range (A & B) | -0.2 to +12 Vdc |
| Hot Switch Power Level (Vctl = 0/+5V) | +39 dBm |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T= 85 °C) (derate 7.14 mW/ °C above 85°C) | 0.465 W |
| Thermal Resistance | 140 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |

DC blocks are required at ports RFC, RF1 and RF2.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing




NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [3] |
|---|---|---|---|---|
| HMC544 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 [1] | H544<br>XXXX |
| HMC544E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | 544E<br>XXXX |

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX



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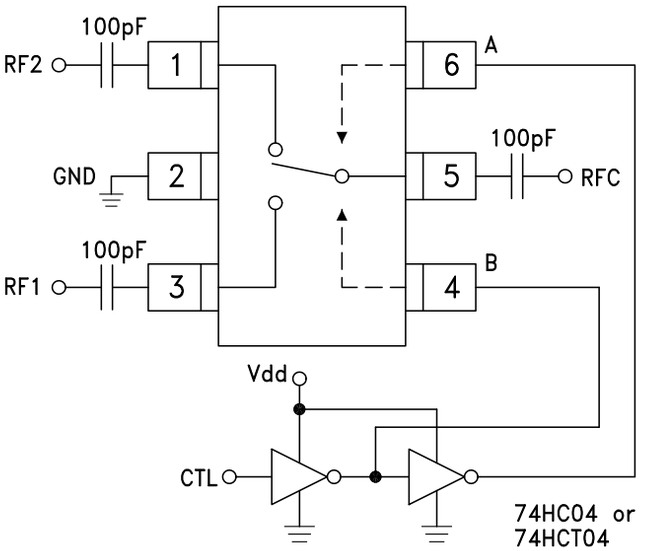
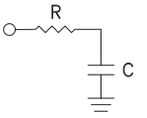
## Typical Application Circuit




**Notes:**

1. Set logic gate Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of +3V to +5V applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.

## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 3, 5 | RF2, RF1, RFC | These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. | |
| 2 | GND | This pin must be connected to RF/DC ground. |   |
| 4 | B | See truth and control voltage tables. |   |
| 6 | A | See truth and control voltage tables. | |





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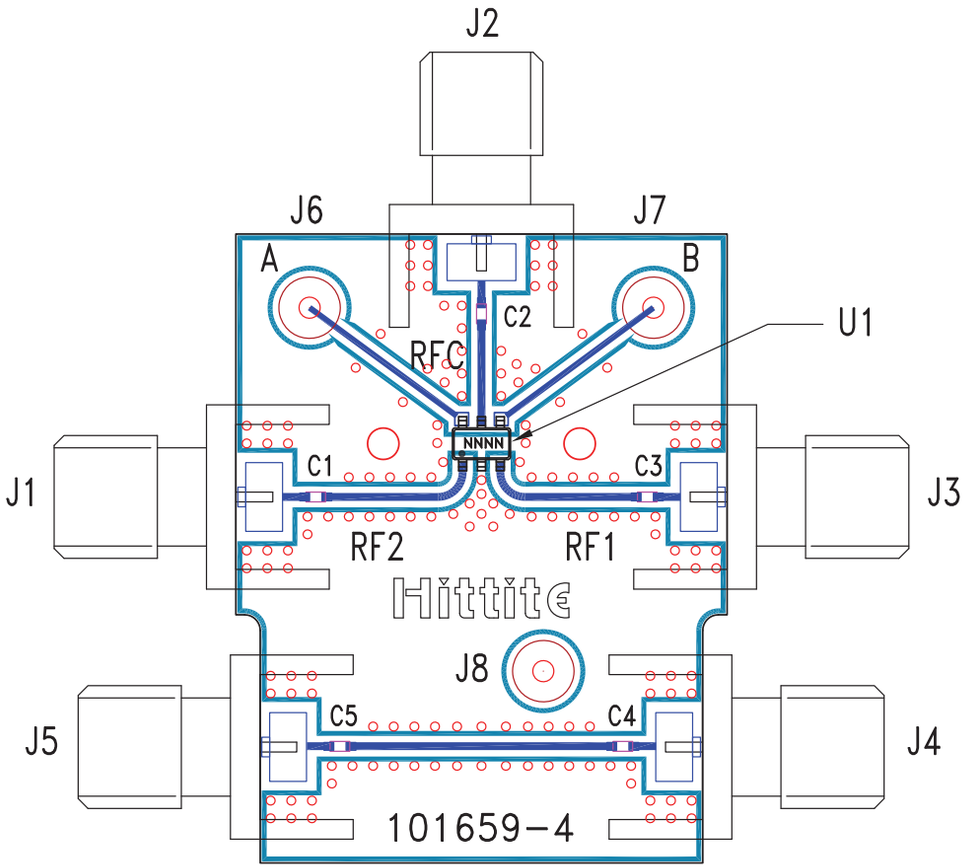
## Evaluation Circuit Board




## List of Materials for Evaluation PCB 101675 [1]

| Item | Description |
|---|---|
| J1 - J5 | PCB Mount SMA RF Connector |
| J6 - J8 | DC Pin |
| C1 - C5 | 330 pF capacitor, 0402 Pkg. |
| U1 | HMC544 / HMC544E SPDT Switch |
| PCB [2] | 101659 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.





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