HMC699LP5 / 699LP5E

v05.0110

7 GHz INTEGER N SYNTHESIZER CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)

Typical Applications

The HMC699LP5(E) is ideal for:

- Satellite Communication Systems
- Point-to-Point Radios
- Military Applications
- Sonet Clock Generation

Features

Ultra Low SSB Phase Noise Floor:
-153 dBc/Hz @ 10 kHz offset @ 100 MHz Reference Frequency.

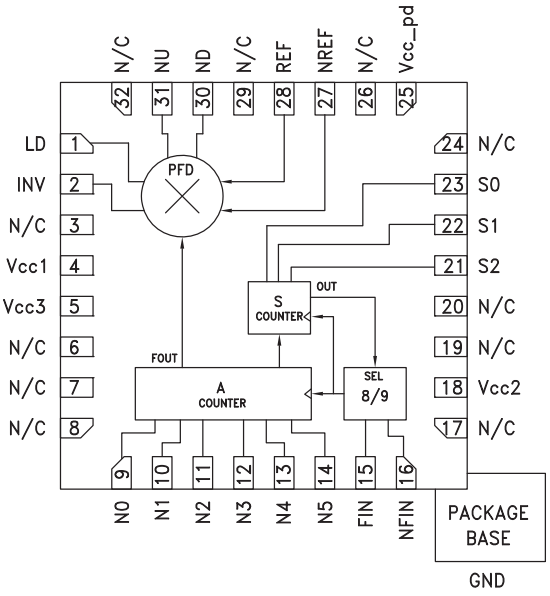
Programmable Divider (N = 16 - 519)
Operating up to 7 GHz

Open Collector Output Buffer Amplifiers for Interfacing w/ Op-Amp Based Loop Filter

Reversible Polarity PFD w/ Lock Detect Output

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



General Description

The HMC699LP5(E) is a frequency synthesizer with a wideband reversible polarity digital PFD and lock detect output. The divider operates from 160 - 7000 MHz with a continuous integer division ratio N = 56 to 519 and non-continuous division ratio N = 16 to 54. The HMC699LP5(E) high frequency operation along with ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast settling and very low phase noise. When used in conjunction with a differential loop filter, the HMC699LP5(E) can be used to phase lock a VCO to a reference oscillator. For continuous division ratio, the A counter and S counter must satisfy the condition: A + 1 ≥ S.

Electrical Specifications, T_A = +25° C, Vcc = Vcc1 = Vcc2 = Vcc3 = Vcc_pd = 5V

Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Ref. Input Frequency	Sine or Square Wave Input [1]	1300			MHz
Minimum Ref. Input Frequency	Square Wave Input [2]			10	MHz
Reference Input Power Range	100 MHz Frequency	-5		+5	dBm
Maximum VCO Input Frequency		7000			MHz
Minimum VCO Input Frequency	Sine Wave Input			160	MHz
VCO Input Power Range	100 MHz Input Frequency	-10		+5	dBm
PFD Output Voltage			2000		mV, Pk - Pk
PFD Gain	Gain = Vpp / 2π Rad.		0.32		V/Rad.
SSB Phase Noise	@ 10 kHz Offset @ 100 MHz Square Wave Ref. Input Pin= 0 dBm		-153		dBc/Hz
Total Supply Current			345		mA

[1] Maximum frequencies may be limited by available counter division ratio.

[2] Square wave input achieves best phase noise at lower reference frequency (see sine & square wave comparison plots)

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HMC699* PRODUCT PAGE QUICK LINKS

Last Content Update: 11/29/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC699LP5 Evaluation Board

DOCUMENTATION

Data Sheet

- HMC699 Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- Using the HMC Design Tool for Synthesizers with a PFD Output

REFERENCE MATERIALS

Product Selection Guide

- RF, Microwave, and Millimeter Wave IC Selection Guide 2017

Quality Documentation

- Package/Assembly Qualification Test Report: 32L 5x5mm QFN Package (QTR: 10009 REV: 05)
- Package/Assembly Qualification Test Report: LP5 & LP5G (QTR: 2014-00150 REV: 02)
- Package/Assembly Qualification Test Report: Plastic Encapsulated QFN (QTR: 05006 REV: 02)
- Semiconductor Qualification Test Report: GaAs HBT-A (QTR: 2013-00228)

DESIGN RESOURCES

- HMC699 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC699 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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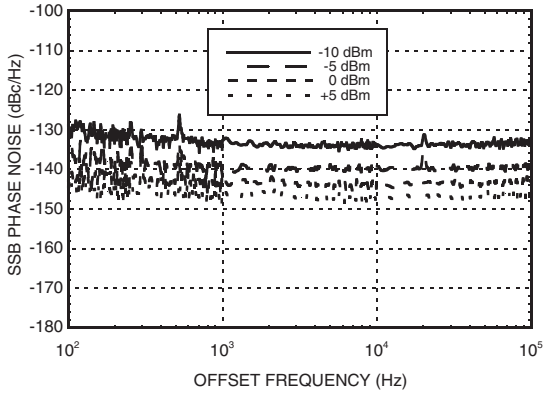
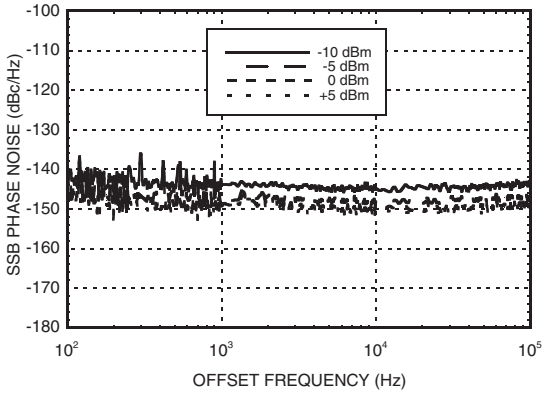
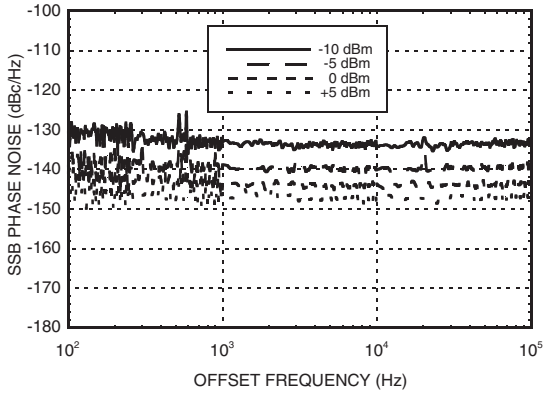
Phase Noise Floor [1][2][3]
Ref = Sine Wave, Vcc = 4.75V



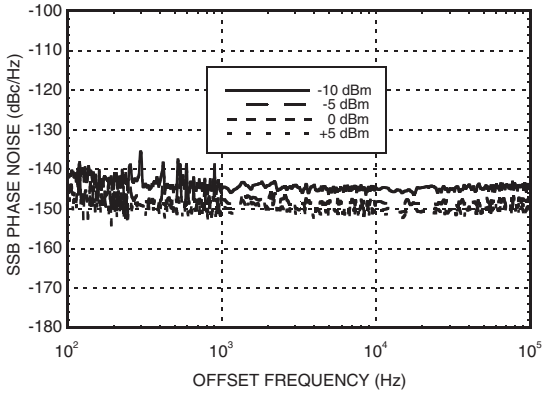
Phase Noise Floor [1][2][3]
Ref = Square Wave, Vcc = 4.75V



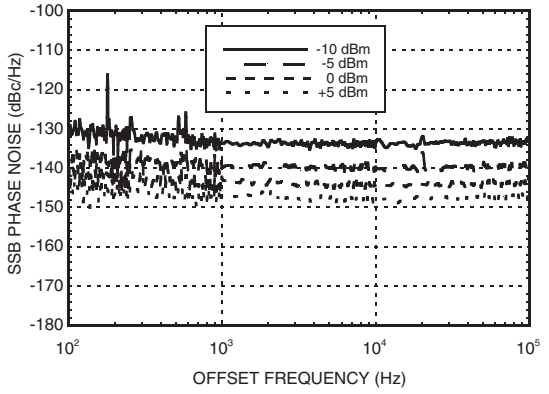
Phase Noise Floor [1][2][3]
Ref = Sine Wave, Vcc = 5V



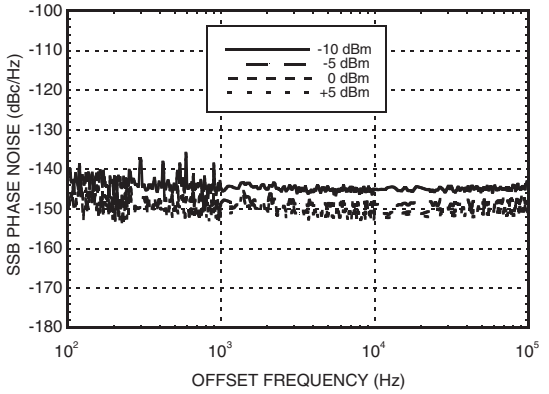
Phase Noise Floor [1][2][3]
Ref = Square Wave, Vcc = 5V



Phase Noise Floor [1][2][3]
Ref = Sine Wave, Vcc = 5.25V



Phase Noise Floor [1][2][3]
Ref = Square Wave, Vcc = 5.25V



[1] Phase Noise Floor vs Offset Frequency with varying Ref Power Level
[2] Fin = 7000 MHz @ 0 dBm, Ref Frequency = 100 MHz, N = 70
[3] Phase Noise Floor remains constant beyond 100 kHz offset frequency

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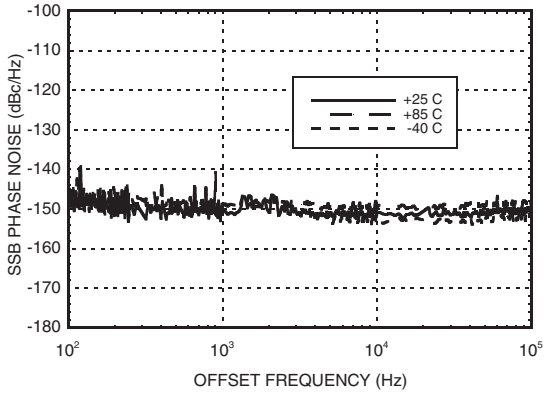
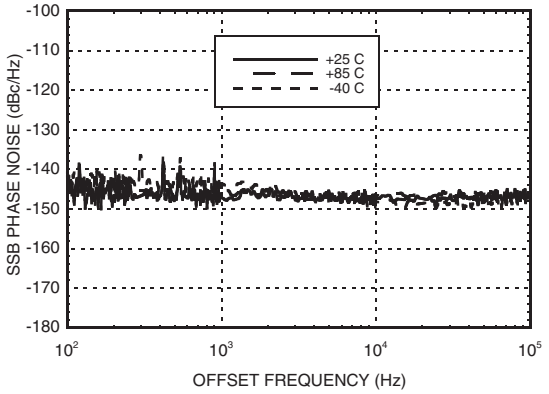
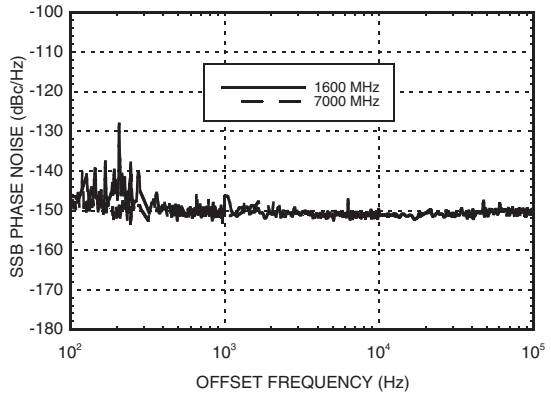
Phase Noise Floor [1][2][3]
Ref = Square Wave @ 5 dBm, Vcc = 5V



Phase Noise Floor [1][2][3]
Ref = Sine Wave @ 5 dBm, Vcc = 5V



Phase Noise Floor vs Offset Frequency with varying Fin @ 0 dbm, Ref = 100 MHz Square Wave @ 5 dBm, Vcc = 5V [3]



Absolute Maximum Ratings

RF Input (Vcc = +5V)	+10 dBm
Supply Voltage (Vcc)	+5.5V
Logic Inputs	-0.5V to (0.5V + Vcc)
Junction Temperature (Tc)	135 °C
Continuous Pdiss (T = 85 °C) (derate 87 mW/°C above 85 °C)	4.3 W
Thermal Resistance (Junction to ground paddle)	11.60 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical DC Characteristics @ Vcc = +5V

Symbol	Characteristics	+25°C			Units
		Min.	Typ.	Max.	
Icc	Power Supply Current	310	345	380	mA
Voh	Output High Voltage, (NU, ND)	5	5	5	V
Vol	Output Low Voltage, (NU, ND)	2.9	3.0	3.1	V

Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
4.75	318
5.00	345
5.25	369

Note: HMC669LP5(E) will work over full voltage range above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

[1] Phase Noise Floor vs Offset Frequency over temperature
[2] Fin= 7000 MHz @ 0 dBm, Ref Frequency = 100 MHz, N = 70
[3] Phase Noise Floor remains constant beyond 100 kHz offset frequency

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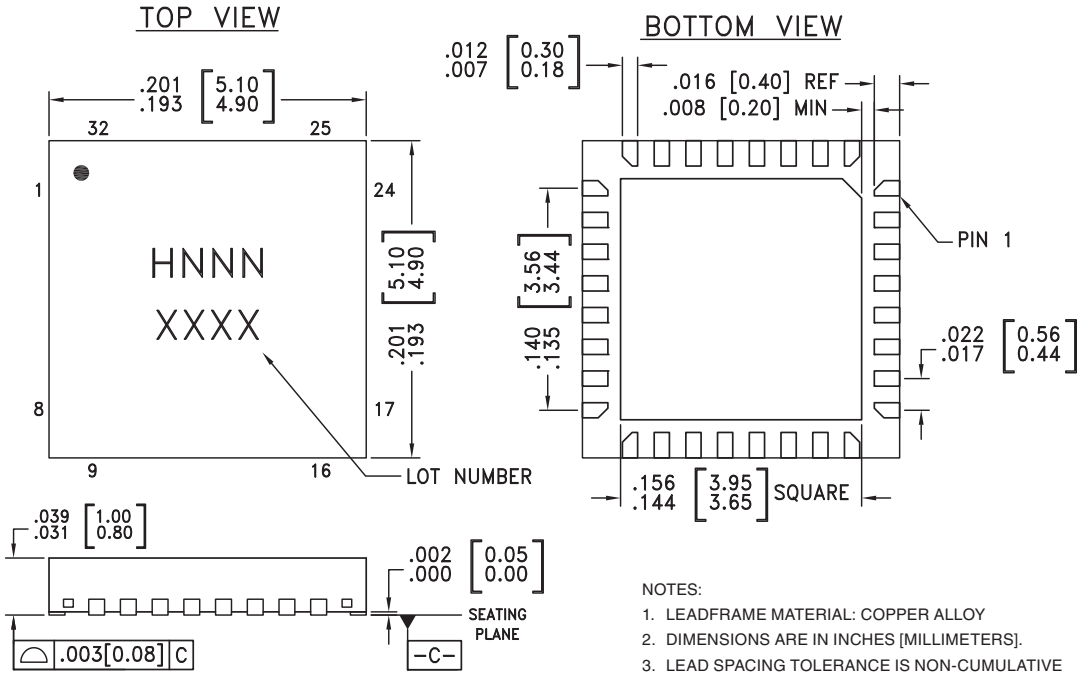
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC699LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H699 XXXX
HMC699LP5(E)	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H699 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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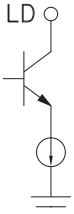
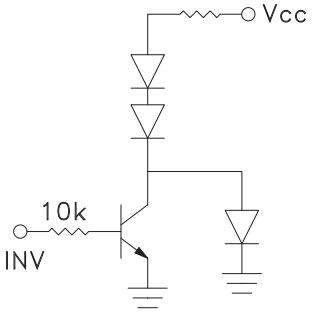
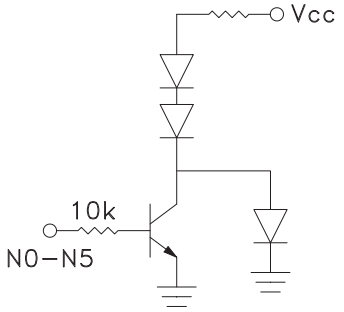
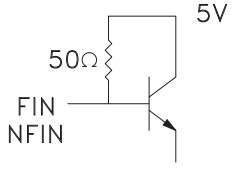
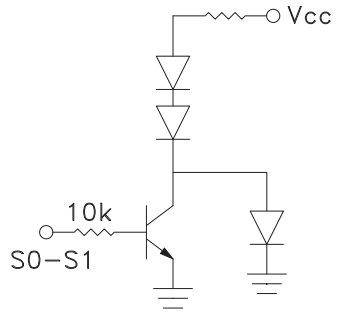
Pin Description

Pin Number	Function	Description	Interface Schematic
1	LD	Pulsed output. Average "LOW" = UNLOCKED. Average "HIGH" = LOCKED	
2	INV	PFD INVERT function CMOS compatible input control bit Logic "LOW" = NORMAL Logic "HIGH" = INVERT	
3, 6 - 8, 17, 19, 20, 24, 26, 29, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
4, 5, 18, 25	Vcc1, Vcc3, Vcc2, Vcc_pd	Supply Voltage 5V ±0.25V	
9 - 14	N0 - N5	CMOS compatible control input bit 0 (LSB) - 5	
15	FIN	(These pins are AC coupled and must be DC Blocked externally.) Frequency Input	
16	NFIN	Frequency Input Complement	
22, 23	S1, S0	CMOS compatible Control Input bit 0 (LSB) -1	

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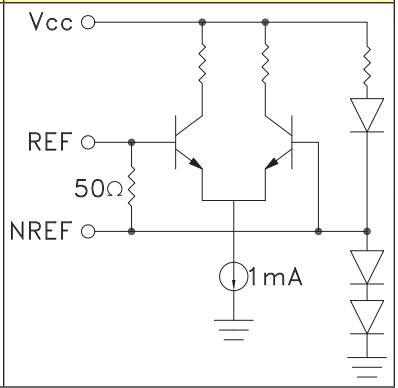
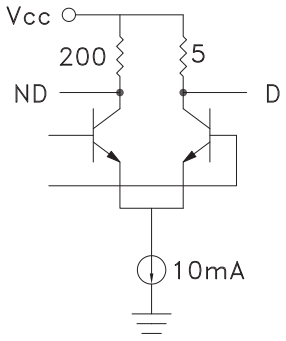
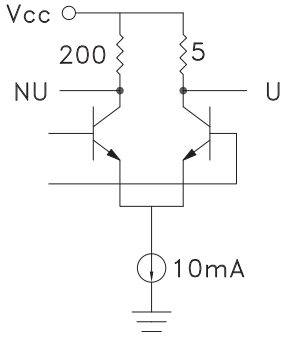
Pin Description *(Continued)*

Pin Number	Function	Description	Interface Schematic
28	REF	Reference Input Reference Input Complement (These pins are AC coupled and must be DC Blocked externally.)	
27	NREF		
30	ND	$\overline{\text{Down Output}}$	
31	NU	$\overline{\text{Up Output}}$	
Ground Paddle	GND	Package bottom has an exposed ground paddle that must be connected to RF/DC ground	

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HMC699LP5(E) Programming

The decimal value of A counter and S counter can be defined as:

$$A = \text{int}\ (\frac{N}{8}) - 1$$

and $S = N - 8\ (A + 1)$

where $N = 16$ to 519

For a valid division ratio N, the A counter and S counter must satisfy the condition: $A + 1 \geq S$

Therefore, N = 16 to 54 will result into non-continuous division ratio

and N = 56 to 519 will be continuous division ratio.

Example: Given a reference frequency, Fref = 11 MHz, and VCO output frequency, Fvco = (198 to 297) MHz, results in N = 18 to 27. The decimal value of A counter and S counter for N = 18 will be:

$$A = \text{int}\ (\frac{18}{8}) - 1 = 1$$

and $S = 18 - 8\ (1 + 1) = 2$

Since the calculated value of A and S satisfy the condition of $A + 1 \geq S$, the N = 18 is usable division ratio.

The division ratio, N = 23, however, will result in A = 1 and S = 7. Under the condition $A + 1 \geq S$, the division ratio N = 23 is not usable.

In this example, the division ratio, N = 19 to 23 cannot be programmed and therefore, the frequency range of 209 MHz to 253 MHz cannot be used.

HMC699LP5(E) Programming Truth Table, Continuous Division Ratios

Division Ratio N	A Counter Decimal Set	Swallow S Decimal Set	(LSB) A0	A1	A2	A3	A4	A5	(LSB) S0	S1	S2
56	6	0	0	1	1	0	0	0	0	0	0
57	6	1	0	1	1	0	0	0	1	0	0
58	6	2	0	1	1	0	0	0	0	1	0
59	6	3	0	1	1	0	0	0	1	1	0
60	6	4	0	1	1	0	0	0	0	0	1
61	6	5	0	1	1	0	0	0	0	0	1
62	6	6	0	1	1	0	0	0	0	1	1
63	6	7	0	1	1	0	0	0	1	1	1
64	7	0	1	1	1	0	0	0	0	0	0
65	7	1	1	1	1	0	0	0	1	0	0
66	7	2	1	1	1	0	0	0	0	1	0
67	7	3	1	1	1	0	0	0	1	1	0

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HMC699LP5(E) Programming Truth Table, Continuous Division Ratios *(Continued)*

Division Ratio N	A Counter Decimal Set	Swallow S Decimal Set	(LSB) A0	A1	A2	A3	A4	A5	(LSB) S0	S1	S2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
512	63	0	1	1	1	1	1	1	0	0	0
513	63	1	1	1	1	1	1	1	1	0	0
514	63	2	1	1	1	1	1	1	0	1	0
515	63	3	1	1	1	1	1	1	1	1	0
516	63	4	1	1	1	1	1	1	0	0	1
517	63	5	1	1	1	1	1	1	1	0	1
518	63	6	1	1	1	1	1	1	0	1	1
519	63	7	1	1	1	1	1	1	1	1	1

HMC699LP5(E) Programming Truth Table, Non-Continuous Division Ratios

Division Ratio N	A Counter Decimal Set	Swallow S Decimal Set	(LSB) A0	A1	A2	A3	A4	A5	(LSB) S0	S1	S2
16	1	0	1	0	0	0	0	0	0	0	0
17	1	1	1	0	0	0	0	0	1	0	0
18	1	2	1	0	0	0	0	0	0	1	0
24	2	0	0	1	0	0	0	0	0	0	0
25	2	1	0	1	0	0	0	0	1	0	0
26	2	2	0	1	0	0	0	0	0	1	0
27	2	3	0	1	0	0	0	0	1	1	0
32	3	0	1	1	0	0	0	0	0	0	0
33	3	1	1	1	0	0	0	0	1	0	0
34	3	2	1	1	0	0	0	0	0	1	0
35	3	3	1	1	0	0	0	0	1	1	0
36	3	4	1	1	0	0	0	0	0	0	1
40	4	0	0	0	1	0	0	0	0	0	0
41	4	1	0	0	1	0	0	0	1	0	0
42	4	2	0	0	1	0	0	0	0	1	0
43	4	3	0	0	1	0	0	0	1	1	0
44	4	4	0	0	1	0	0	0	0	0	1
45	4	5	0	0	1	0	0	0	1	0	1
48	5	0	1	0	1	0	0	0	0	0	0
49	5	1	1	0	1	0	0	0	1	0	0
50	5	2	1	0	1	0	0	0	0	1	0
51	5	3	1	0	1	0	0	0	1	1	0
52	5	4	1	0	1	0	0	0	0	0	1
53	5	5	1	0	1	0	0	0	1	0	1
54	5	6	1	0	1	0	0	0	0	1	1

* Choose values of R2 & R4 between 4.3 and 20 Ohms for best noise performance.

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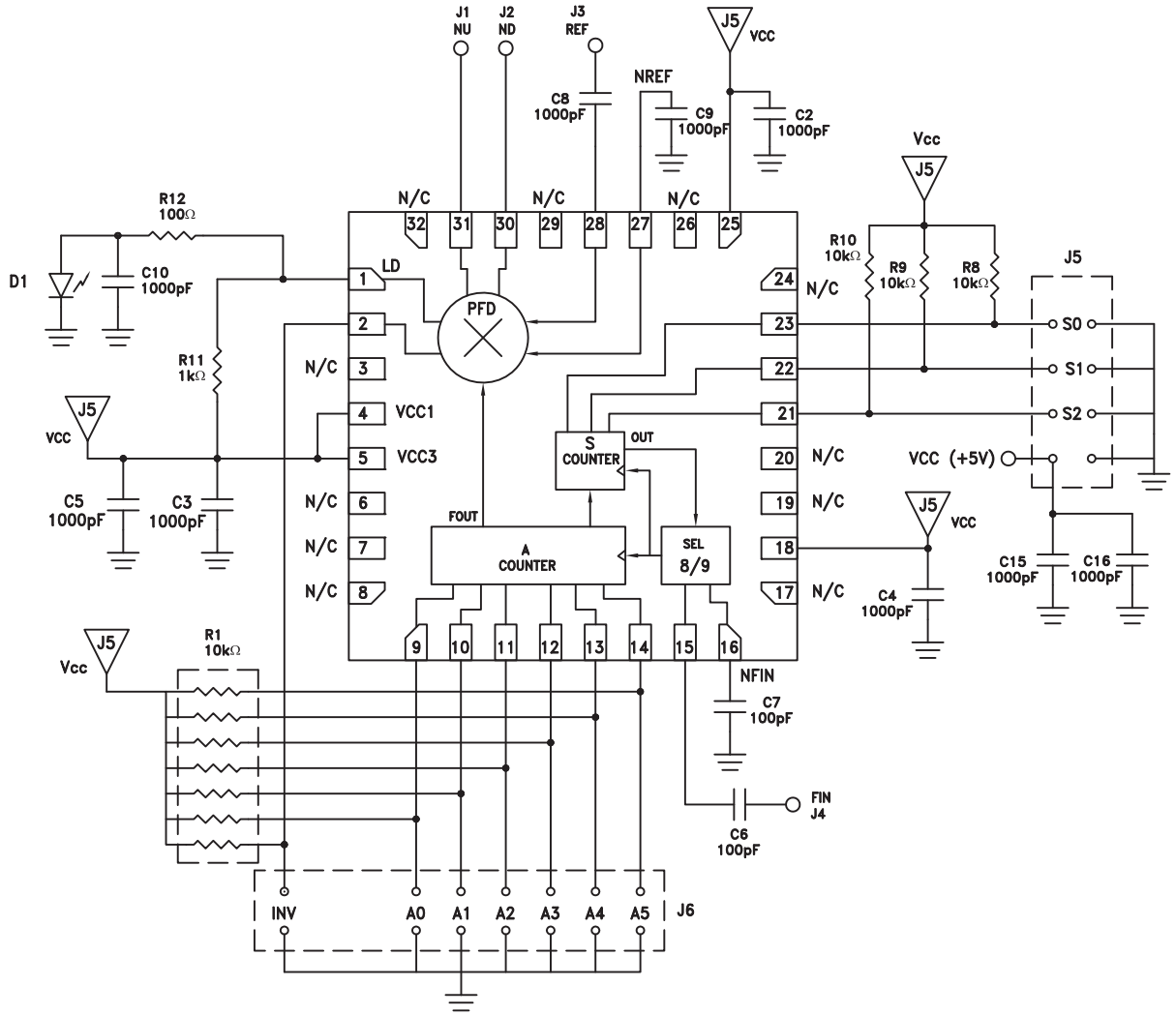
Evaluation PCB Circuit



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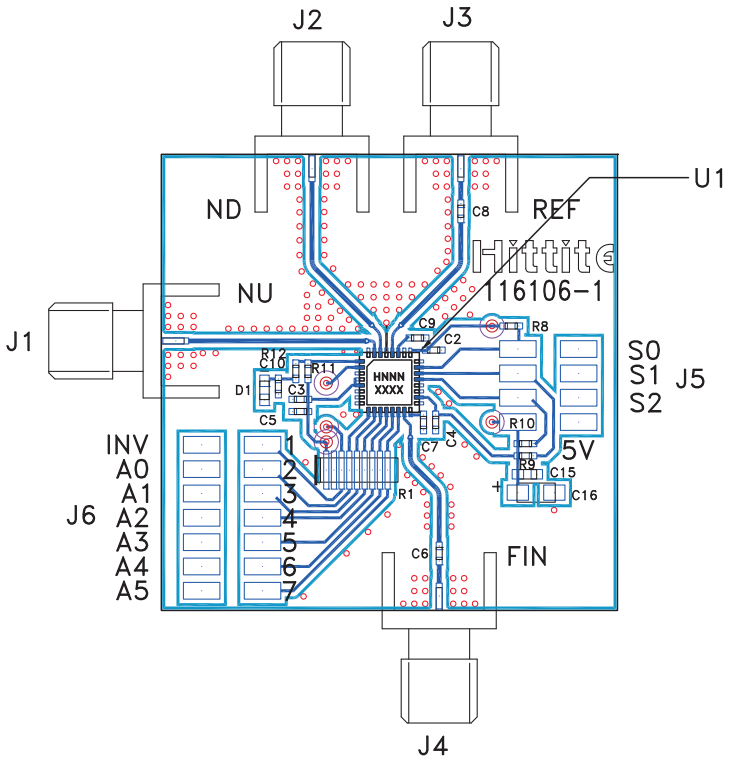
Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

List of Materials for Evaluation PCB 116108 [1]

Item	Description
J1 - J4	PC Mount SMA RF Connector
J5 - J6	2mm DC Header
C1 - C5, C8 - C10	1000 pF Capacitor, 0402 Pkg.
C6 - C7	100 pF Capacitor, 0402 Pkg.
C15	1000 pF Capacitor, 0603 Pkg.
C16	4.7 µF Tantalum Capacitor Case A
D	LED Green, 0603 Pkg., +5V
R1	10k Ohm, Resistor, Array
R8, R10	10k Ohm, Resistor, 0402 Pkg.
R11	1k Ohm, Resistor, 0402 Pkg.
R12	100 Ohm, Resistor, 0402 Pkg.
U1	HMC699LP5(E) Synthesizer
PCB [2]	116106 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

Evaluation PCB Truth Table (see Programming Truth Table)

Note: 0 = Jumper Installed.
1 = Jumper Not Installed.

Note: The evaluation PCB for the HMC699LP5(E) contains 10 kOhm pull up resistors for each of the control inputs A0 through A5 and S0 through S2. Programming the 489 distinct division ratios consists of installing or removing jumpers A0 through A5 and S0 though S2.

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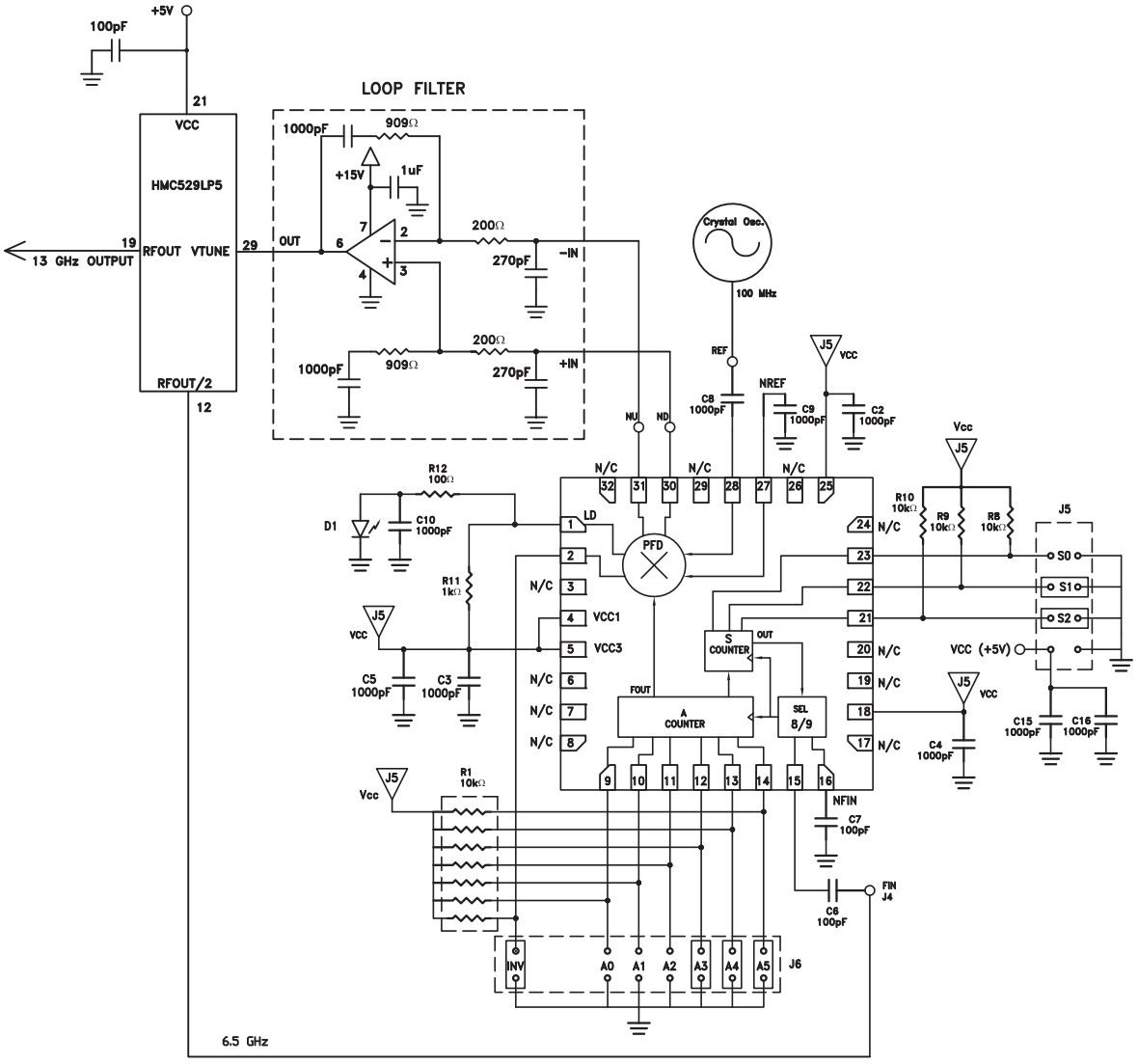
7 GHz INTEGER N SYNTHESIZER CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)

Typical PLL Application Circuit using HMC699LP5

PLL application shown for a 13 GHz Fout. Contact HMC to discuss your specific application.



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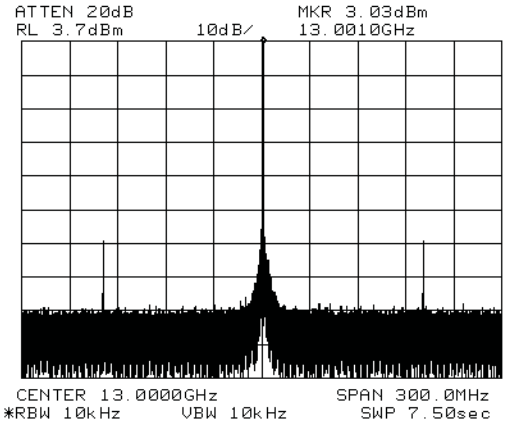
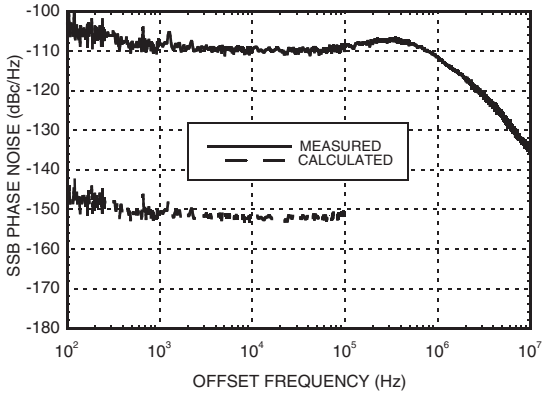
7 GHz INTEGER N SYNTHESIZER CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)

Typical Application Showing Spurious Performance



Typical Application 13 GHz Measured Phase Noise [1]



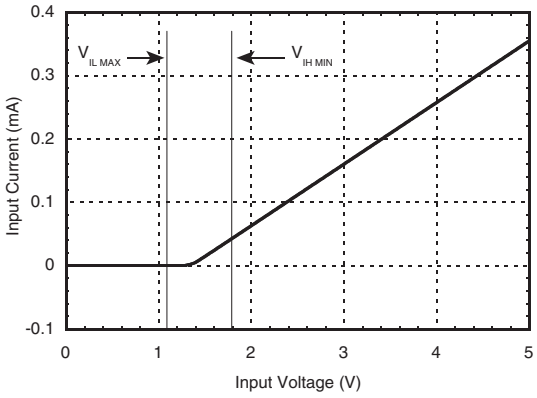
[1] Phase Noise Floor remains constant beyond 100 kHz offset frequency. Measured phase noise using Agilent 5500 with 2 unit measurement technique and corresponding calculated phase noise floor.

CMOS/TTL Input Characteristics

Maximum Input Logic "0" Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 1 µA.

Minimum Input Logic "1" Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 50 µA.

Input IV characteristics for the logic inputs (A0 - A5 and S0 - S2) are shown below:



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