



GaAs HBT HIGH LINEARITY PUSH-PULL AMPLIFIER, 75 Ohm, DC - 1 GHz

Typical Applications

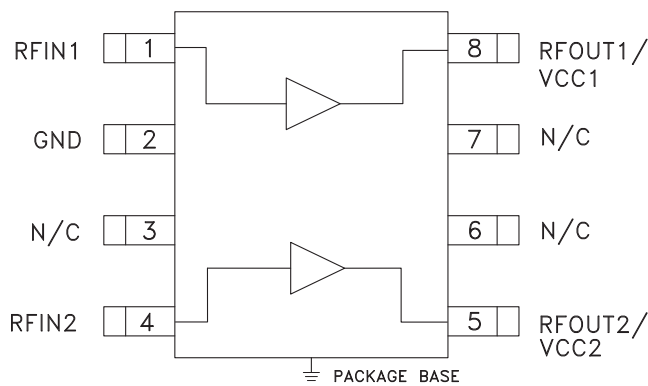
The HMC754S8GE is ideal for:

- CATV / Broadband Infrastructure
- Test & Measurement Equipment
- Line Amps and Fiber Nodes
- Customer Premise Equipment

Features

- Output IP2: +78 dBm
- High Gain: 14.5 dB
- High Output IP3: +38 dBm
- 75 Ohm Impedance
- Single Positive Supply: +5V
- Robust 1000V ESD, Class 1C
- SOIC-8 SMT Package

Functional Diagram



General Description

The HMC754S8GE is a GaAs/InGaP HBT Dual Channel Gain Block MMIC SMT amplifier covering DC to 1 GHz. This versatile product contains two gain blocks, packaged in a single 8 lead plastic SOIC-8, for use with both amplifiers combined in push-pull configuration using external baluns to cancel out second order non-linearities and improve IP2 performance. In this configuration, the HMC754S8GE offers high gain, very low distortion & simple external matching. This high linearity amplifier consumes only 160mA from a single positive supply.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{cc1} = V_{cc2} = 5\text{V}$, $Z_o = 75\text{ Ohm}$ [1]

Parameter		Min.	Typ.	Max.	Units
Gain	0.05 - 0.5 GHz	13.5	14.7		dB
	0.5 - 0.87 GHz	12.7	14.2		dB
	0.87 - 1.0 GHz	12.1	13.4		dB
Gain Variation Over Temperature	0.05 - 0.87 GHz		0.008		dB/ °C
Input Return Loss	0.05 - 0.5 GHz		17		dB
	0.5 - 0.87 GHz		10		dB
Output Return Loss	0.05 - 0.5 GHz		10		dB
	0.5 - 0.87 GHz		20		dB
Reverse Isolation	0.05 - 0.87 GHz		23		dB
Output Power for 1 dB Compression (P1dB)	0.05 - 0.87 GHz	19.5	21		dBm
Output Third Order Intercept Point (IP3) (Pout= 0 dBm per tone, 1 MHz spacing)	0.05 - 0.87 GHz		38		dBm
Output Second Order Intercept Point (IP2)	0.05 - 0.5 GHz		78		dBm
Composite Second Order (CSO) [2]	0.05 - 0.87 GHz		-81		dBc
Composite Triple Beat (CTB) [2]	0.05 - 0.87 GHz		-75		dBc
Cross Modulation (XMOD) [2]	0.05 - 0.87 GHz		-67		dBc
Noise Figure	0.05 - 0.5 GHz		5.5		dB
	0.05 - 0.87 GHz		6.5		dB
Supply Current (Icc1 + Icc2)		145	160	175	mA

[1] Data taken with dual amplifiers combined in push-pull (default) configuration

[2] Input level +15 dBmV, 133 channels - with analog modulation

HMC754* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC754S8GE Evaluation Board

DOCUMENTATION

Application Notes

- AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
- Broadband Biasing of Amplifiers General Application Note
- MMIC Amplifier Biasing Procedure Application Note
- Thermal Management for Surface Mount Components General Application Note

Data Sheet

- HMC754 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- HMC Legacy PCN: S## and S##E packages - Relocation of pre-existing production equipment to new building
- Package/Assembly Qualification Test Report: Plastic Encapsulated SOIC (QTR: 02018 REV: 01)
- Semiconductor Qualification Test Report: GaAs HBT-E (QTR: 2013-00271)

DESIGN RESOURCES

- HMC754 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC754 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

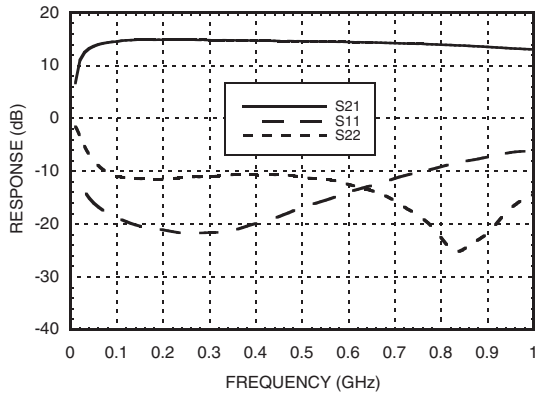
DOCUMENT FEEDBACK

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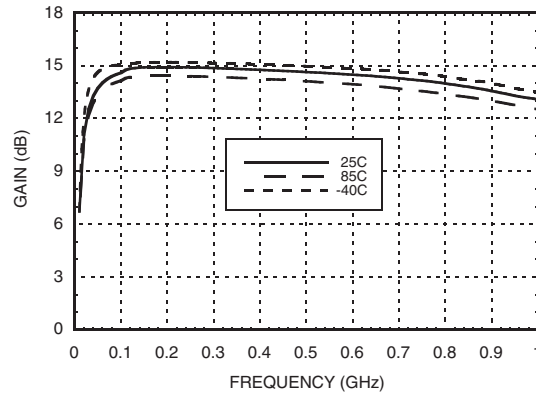


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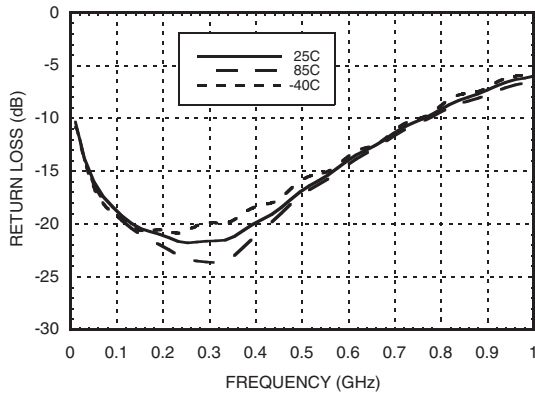
Gain & Return Loss



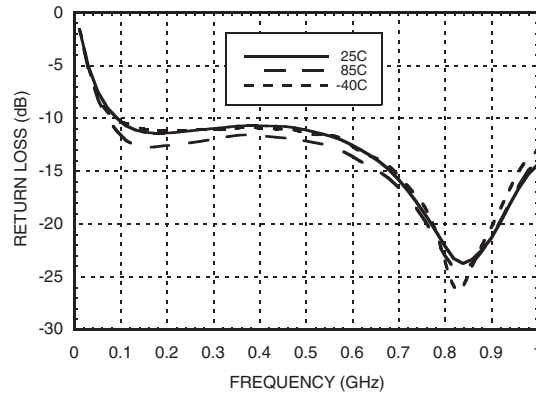
Gain vs. Temperature



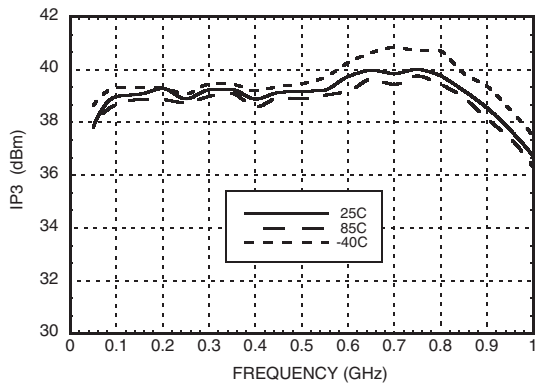
Input Return Loss vs. Temperature



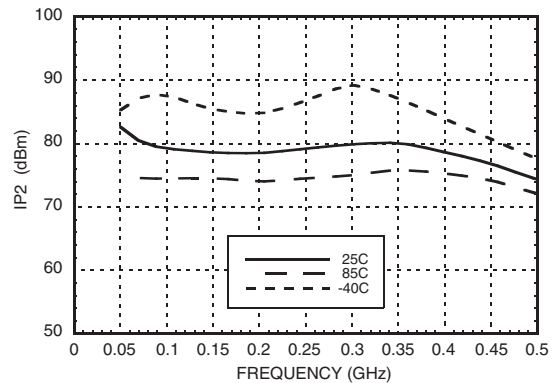
Output Return Loss vs. Temperature



Output IP3 vs. Temperature



Output IP2 vs. Temperature



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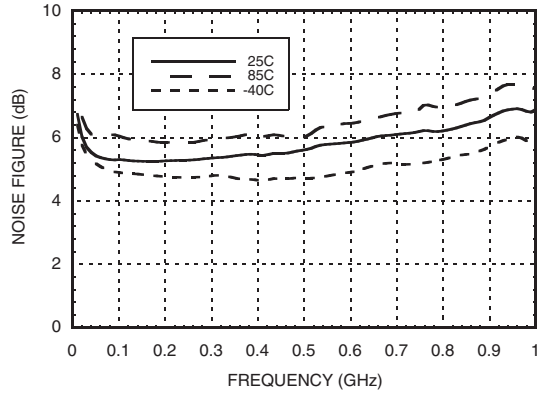


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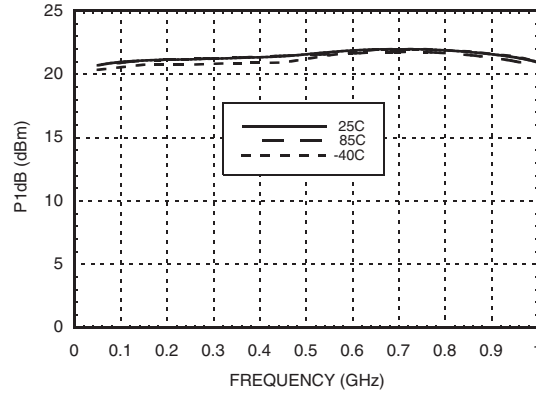
8

AMPLIFIERS - DRIVER & GAIN BLOCK - SMT

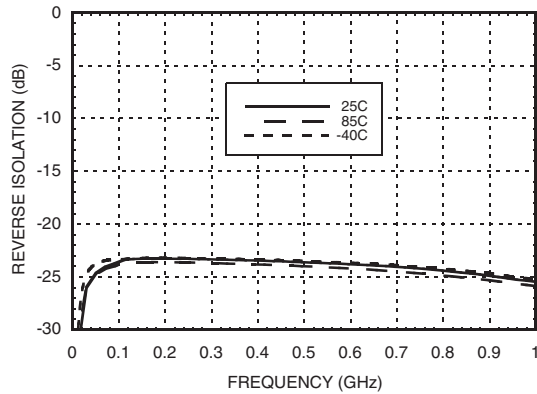
Noise Figure vs. Temperature



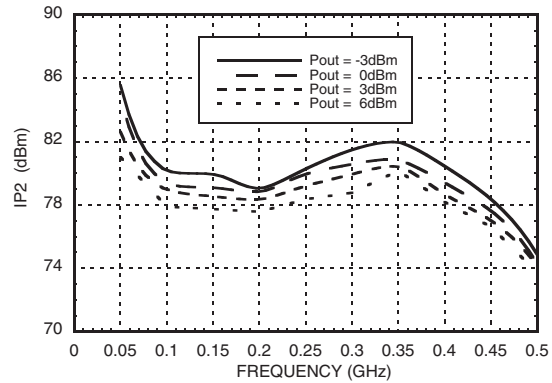
P1dB vs. Temperature



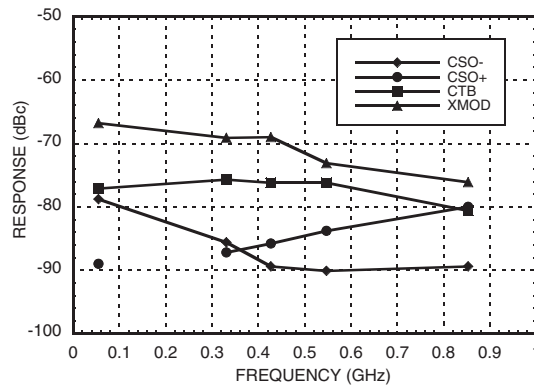
Reverse Isolation vs. Temperature



Output IP2 vs. Output Power



**CSO / CTB / XMOD
@ +15 dBmV input, 133 channels (Analog)**



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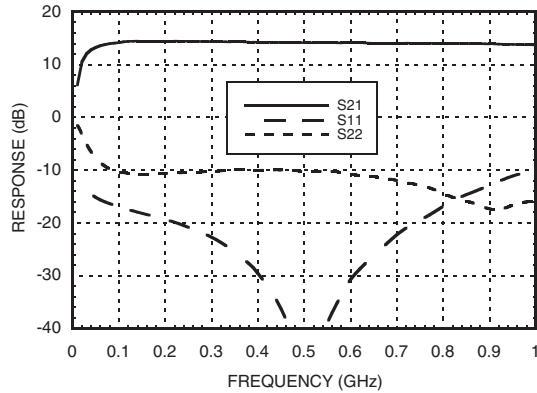
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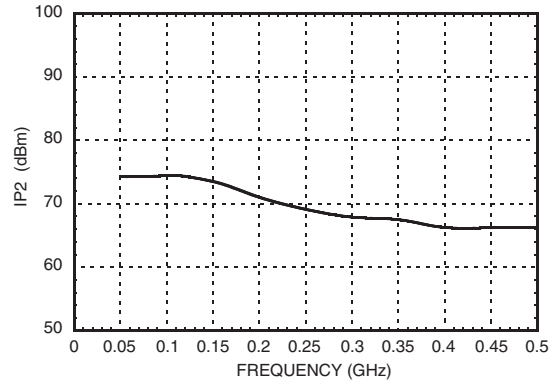
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Option 1 - Improved Input Return Loss & Gain Flatness (with Lower IP2) Application

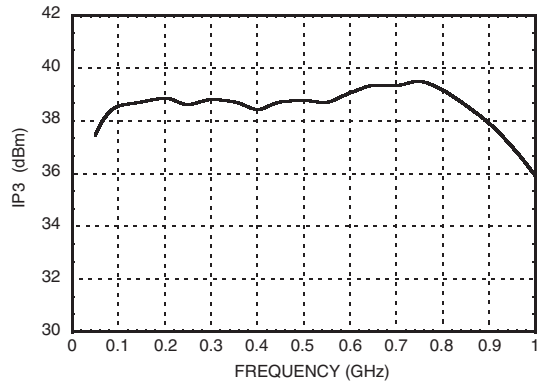
Gain & Return Loss



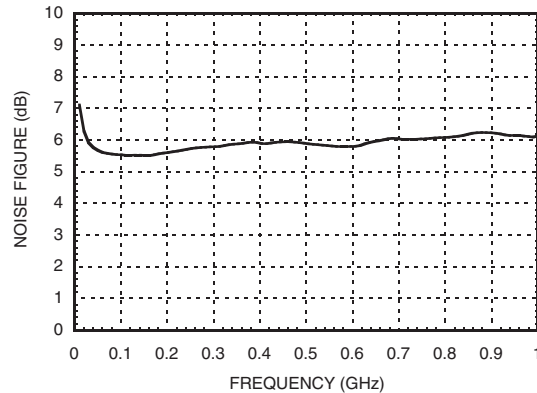
Output IP2 vs. Frequency



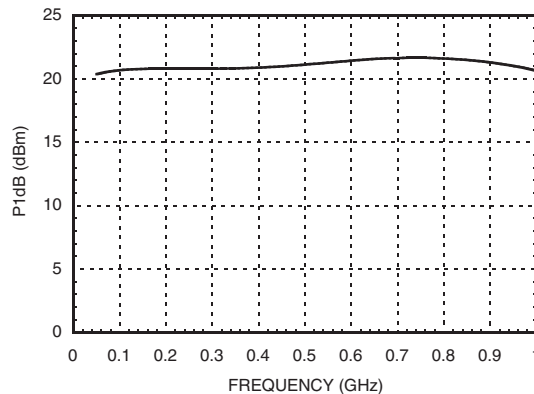
Output IP3 vs. Frequency



Noise Figure vs. Frequency



P1dB vs. Frequency



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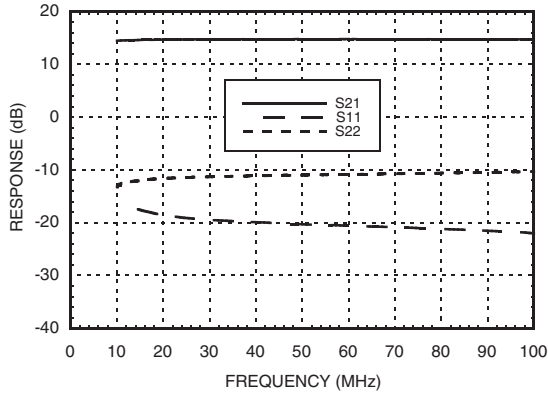
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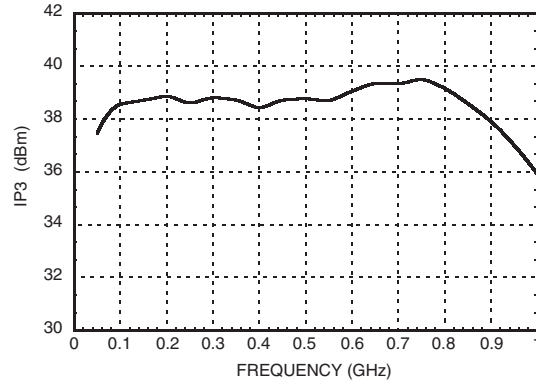
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Option 2 - 10 to 100 MHz Application

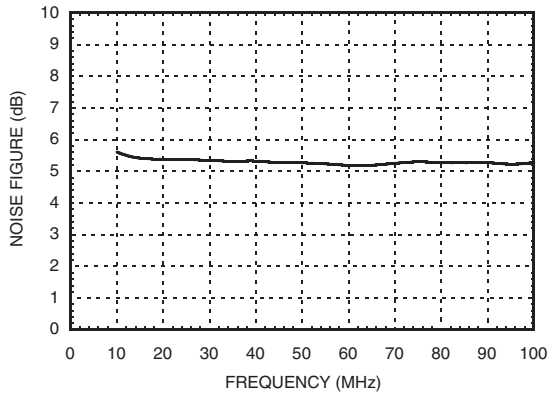
Gain & Return Loss



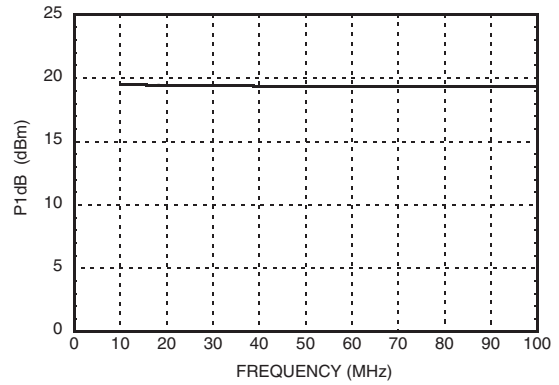
Output IP3 vs. Frequency



Noise Figure vs. Frequency



P1dB vs. Frequency



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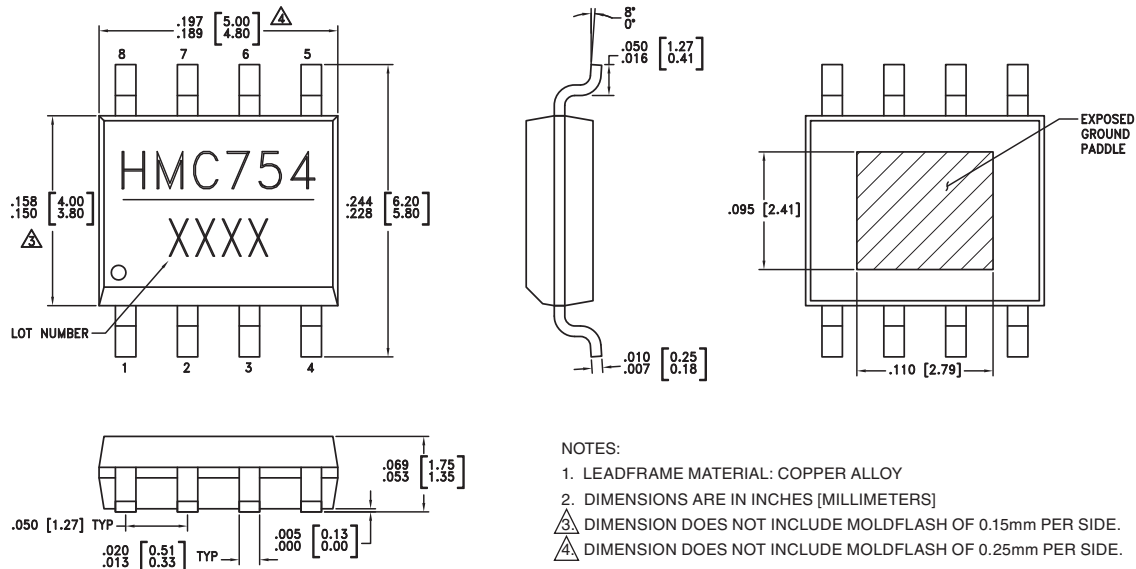
Absolute Maximum Ratings

Collector Bias Voltage (Vcc)	+5.5 Vdc
RF Input Power (RFIN)	+10 dBm
Junction Temperature	150 °C
Continuous P _{diss} (T = 85 °C) (derate 18.69 mW/°C above 85 °C)	1.21 W
Thermal Resistance (junction to ground paddle)	53.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



Package Information

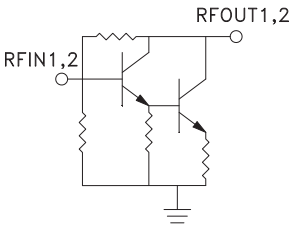

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[3]
HMC754S8GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	HMC754 XXXX

[1] Max peak reflow temperature of 235 °C
 [2] Max peak reflow temperature of 260 °C
 [3] 4-Digit lot number XXXX



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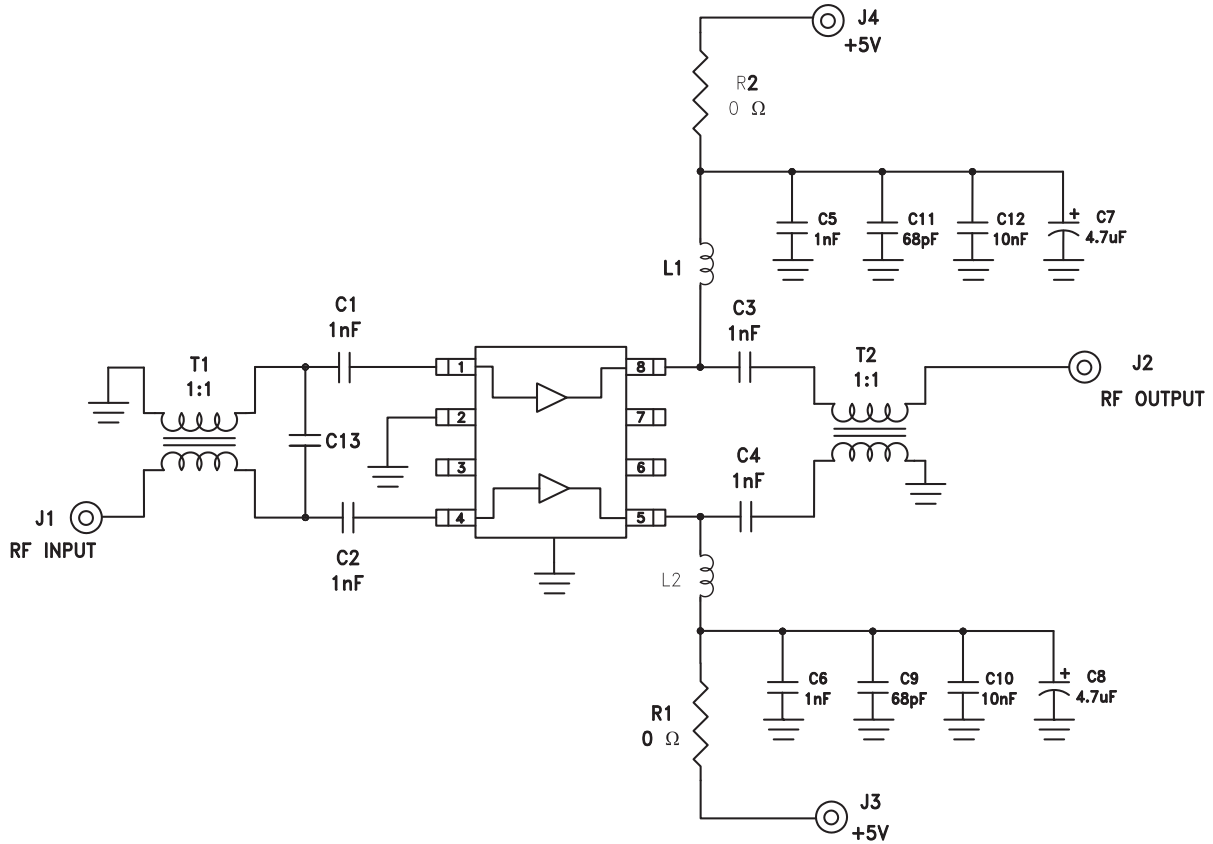
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4	RFIN1, RFIN2	These pins are DC coupled. An off chip DC block capacitor is required.	
5, 8	RFOUT1/VCC1, RFOUT2/VCC2	RF Output and DC bias for the output stage.	
2	GND	These pins and package bottom must be connected to RF/ DC ground.	
3, 6, 7	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	



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Application Circuit for Push-Pull Operation



Components for Selected Options

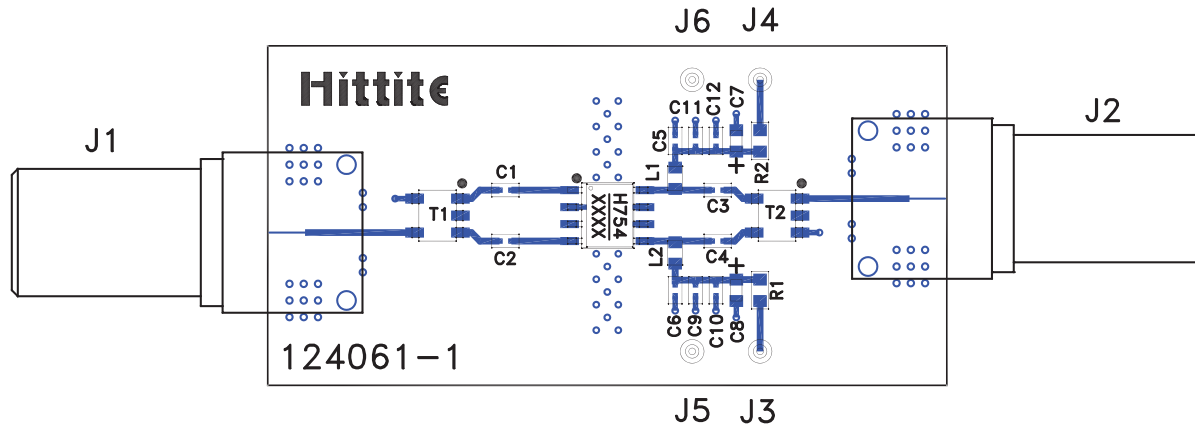
Tune Options	Standard	Option 1	Option 2
Evaluation PCB Number	124063	126311	124825
T1 [1]	ETC 1-1-13	MABACT0039	ETC1-1T-5TR
T2 [1]	ETC 1-1-13	ETC 1-1-13	ETC1-1T-5TR
L1, L2	180 nH	180 nH	10 uH
C13	Open	1.1 pF	Open

[1] 1:1 Transformer



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Evaluation PCB - Standard and Option 2 Application



List of Materials for Evaluation PCB [1]

Item	Description
J1, J2	F-Connector
J3 - J6	DC PIN
C1 - C6	1 nF Capacitor, 0402 Pkg.
C7, C8	4.7 μ F Capacitor, Tantalum, 0603 Pkg.
C9, C11	68 pF Capacitor, 0402 Pkg.
C10, C12	10 nF Capacitor, 0402 Pkg.
L1, L2 [2]	Inductor, 0603 Pkg.
R1, R2	0 Ohm Resistor, 0603 Pkg.
T1, T2 [2]	1:1 Transformer
U1	HMC754S8GE Amplifier
PCB [3]	124061 Evaluation PCB

[1] When requesting an evaluation board, please reference the appropriate evaluation PCB number listed in the table "Components for Selected Options."

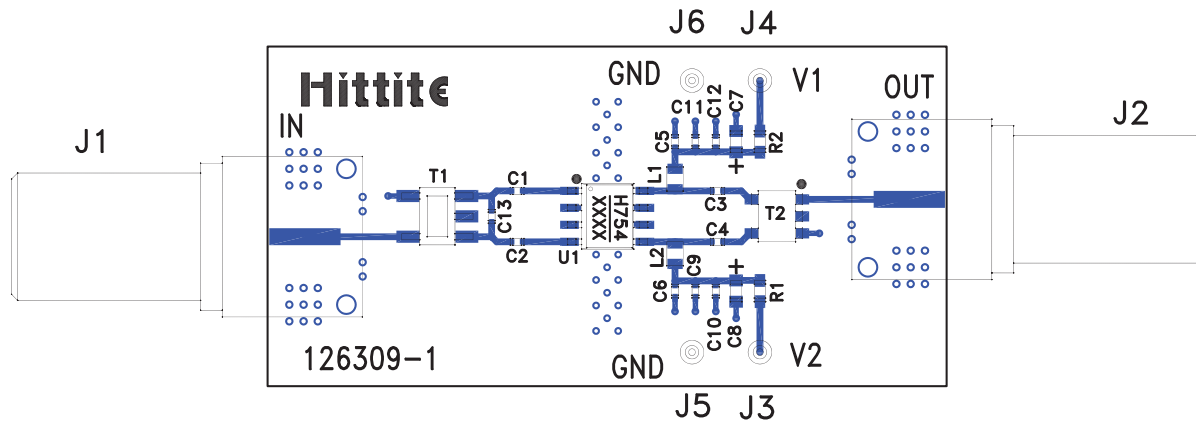
[2] Please refer to "Components for Selected Options" table for values

[3] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 75 ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.



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Evaluation PCB - Option 1 Application

List of Materials for Evaluation PCB [1]

Item	Description
J1, J2	F-Connector
J3 - J6	DC PIN
C1 - C6	1 nF Capacitor, 0402 Pkg.
C7, C8	4.7 μ F Capacitor, Tantalum, 0603 Pkg.
C9, C11	68 pF Capacitor, 0402 Pkg.
C10, C12	10 nF Capacitor, 0402 Pkg.
C13	1.1 pF Capacitor, 0402 Pkg.
L1, L2	180 nH Inductor, 0603 Pkg.
R1, R2	0 Ohm Resistor, 0603 Pkg.
T1, T2 [2]	1:1 Transformer
U1	HMC754S8GE Amplifier
PCB [3]	126309 Evaluation PCB

[1] When requesting an evaluation board, please reference the appropriate evaluation PCB number listed in the table "Components for Selected Options."

[2] Please refer to "Components for Selected Options" table for values

[3] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 75 ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.