Evaluation Board for
500 MSPS DDS with 10-Bit DAC
EVAL-AD9911

FEATURES

PC evaluation software for control and measurement of the AD9911
USB interface
Graphic user interface (GUI) software with frequency sweep capability for board control and data analysis
Factory tested and ready to use

APPLICATIONS

AD9911 performance evaluation
GUI control panel for learning AD9911 programming

GENERAL DESCRIPTION

This data sheet serves as a guide to the setup and use of the AD9911 evaluation board. The AD9911 is a single channel frequency synthesizer that incorporates spur reduction technology and test tone modulation along with many user-programmable functions.

The evaluation board software provides a GUI for easy communication with the device along with many user-friendly features. For example, many elements of the software are clarified by moving the user's pointer over an element such as a box or button. Figure 8 shows how this feature works when users place their pointer over the **Ref Clock** box.

This document is intended for use in conjunction with the AD9911 data sheet available from Analog Devices, Inc. at www.analog.com.

EVALUATION BOARD BLOCK DIAGRAM

Figure 1.

EVAL-AD9911
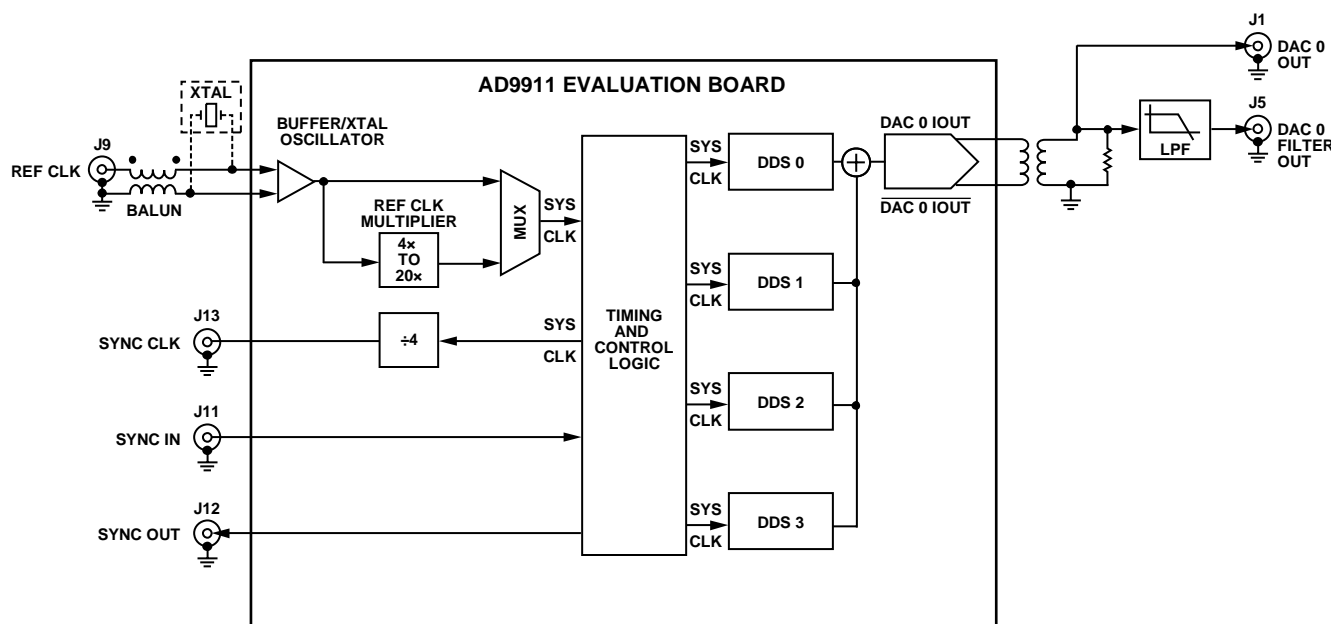
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REVISION HISTORY

12/06—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

PACKAGE CONTENTS

The EVAL-AD9911 kit contains the following items:

- AD9911 evaluation board
- EVAL-AD9911 installation software
- USB cable

REQUIREMENTS

To successfully use the evaluation board and run the software, the requirements listed in Table 1 must be met.

Table 1. EVAL-AD9911 Requirements

Item	Requirement
Operating System	Microsoft® Windows® 98/ME/2000/XP
Processor	Pentium® I or faster
Memory	128 MB minimum
Ports	One USB port
Clocking	Signal generator capable of generating sinusoidal waves of at least 3 dBm power, up to at least 10 MHz
Power Supplies	Capability to generate at least two independent dc voltages (1.8 V/3.3 V)
Measurement	Appropriate measurement device such as a spectrum analyzer or a high bandwidth oscilloscope
Cables	USB 1.1/2.0 cable and SMA-to-X cables (X = SMA or BNC, depending on the connector of the device interfacing with the board)

SETTING UP THE EVALUATION BOARD

Powering the Part

The AD9911 evaluation board has seven power supply connectors: TB1, J10, J16, J17, J18, J19, and J20. TB1 powers the DDS, the PC interface logic, and the USB circuitry. J10 powers the input clock circuitry. J18 provides the reference voltage needed for band gap functionality. J16, J17, J19, and J20 power the analog circuitry of individual DACs.

Table 2 shows the necessary connections and the appropriate biasing voltage.

Table 2. Connections and Biasing Voltage

Connector	Pin No.	Label	Voltage (V)
TB1	1	VCC_USB	3.3
TB1	2	DVDD_I/O	3.3
TB1	3	GND	0
TB1	4	DVDD	1.8
J10[1]		CLK_VDD	1.8
J18[1]		BG_VDD	1.8
J16/J17/J19/J20[1]		AVDD	1.8

[1]The EVAL-AD9911 is preconfigured so that the CLK_VDD, BG_VDD, and all other AVDD connections are tied together. Therefore, only one connection (J10, J18, or J16/J17/J19/J20) needs power for proper functionality.

These AVDD connections can be separated for better channel isolation. This is accomplished by removing the 0 Ω resistors (R38 to R49) that tie the planes together on the back of the evaluation board. When doing this, be sure that the CLK_VDD, BG_VDD, and AVDD connections are powered.

Clocking the Part

The AD9911 architecture provides the user with two options when providing an input signal to the part. Figure 1 shows that the user can directly clock the frequency synthesizer/DDS by connecting an external clocking signal to the REF CLK connector, J9, or by providing an external crystal. Place jumper W11 on REF CLK to use the external clocking option. To use an external crystal as the clocking source, place jumper W11 on XTAL.

Refer to the AD9911 data sheet for details on the maximum input speeds and input sensitivies of these two inputs.

Communicating with the Part

Two interface standards are available on the evaluation board:

- USB 1.1/2.0
- Header row (P1, P2), which places the part under the control of an external controller (such as a µP, FPGA, or DSP)

Analog Devices provides a GUI for the PC; it does not provide control software for external controllers.

Use the jumper settings listed in Table 3 to enable different modes of communication.

Table 3. Jumper Settings for Communication Modes

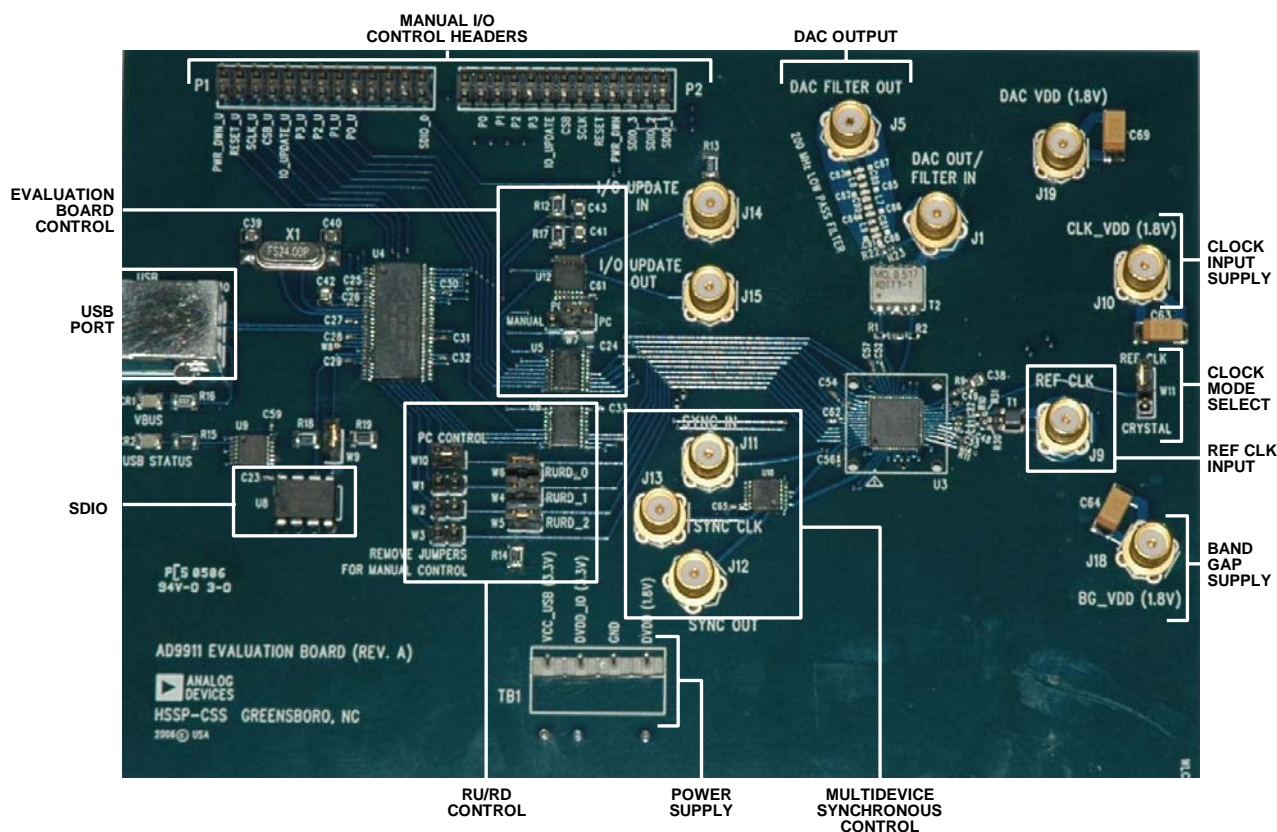| Mode	Settings
PC Control, USB Port	Set W7 to PC. Place a jumper on W1, W2, W3, W9, and W10.
External Control	Set W7 to manual. Place a jumper on W9 and remove W1, W2, W3, and W10 (or leave it stored as a shunt).

EVALUATION BOARD LAYOUT

Figure 2.

Manual I/O Control Headers

Provides the communication interface with the AD9911 when the part is under the control of an external controller (manual control). See the Eval Board Control section for correct jumper settings.

Multi Device Synchronous Control

These connections set up the AD9911 for multidevice synchronous operation.

DAC Output

These connections represent the DAC filtered/unfiltered output and AVDD power supply.

Clock Input Supply

Powers the AD9911 clock input circuitry.

Clock Mode Select

Controls whether the part is driven by a 20 MHz to 30 MHz crystal (user must provide), or by an external signal generator.

REF CLK Input

Input for the external REF CLK signal.

Band Gap Supply

Provides the voltage needed for band gap functionality.

Power Supply

Powers the AD9911 USB circuitry, I/O circuitry, and the digital portion (DVDD) of the DAC. Note that AVDD is not powered via this connector (TB1).

RU/RD Control, SDIO

Jumper W6, Jumper W5, and Jumper W4 must be set to control the ramp-up/ramp-down feature using the SDIO pins.

USB Port

When the part is under PC control (default mode), the evaluation board communicates with the AD9911 via this port.

Eval Board Control

These jumpers set up the AD9911 for manual or PC control (control through the USB port). For manual control, remove Jumper W10, Jumper W1, Jumper W2, and Jumper W3; set W7 on the manual control pin (move jumper one position to the left).

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

Follow these steps to install the AD9911 evaluation software:

1. Log into your PC system with administrative privileges.
2. Uninstall any previous versions of the AD9911 evaluation software from your PC system.
3. Insert the AD9911 evaluation software CD into your CD-ROM drive. Do not connect the AD9911 evaluation board to the computer until the AD9911 evaluation software has been successfully installed. Refer to the **Readme.txt** file located in the Software folder before proceeding with the installation of the AD9911 evaluation software.
4. Run the **setup.exe** file located in the **Software** folder and follow the on-screen installation instructions.

CONFIGURING THE EVALUATION BOARD

Once the software has been successfully installed onto your PC, the next step is to interface the AD9911 evaluation software to the AD9911 evaluation board via the USB port (see Figure 2).

For the evaluation board and software to communicate properly, drivers must be loaded onto your PC system. The following instructions explain how to install these drivers onto your PC system.

Windows 98/ME/2000 Users

1. Power up the AD9911 evaluation board (see Table 2).
2. Connect the evaluation board to the computer using the supplied USB cable via the USB port; the **VBUS LED** (CR1 on AD9911 evaluation board) illuminates.
3. When the USB cable is connected, the **Found New Hardware** window appears.
4. If you are using Windows 2000, click **Finish** in the **Found New Hardware Wizard**.

After the window has disappeared, the **USB Status LED** (CR2 on AD9911 evaluation board) flashes, indicating that the evaluation board is connected properly.

Windows XP Users

1. Power up the AD9911 evaluation board (see Table 2).
2. Connect the evaluation board to the computer using the supplied USB cable via the USB port. Then, the **VBUS LED** (CR1 on AD9911 evaluation board) illuminates.
3. When the USB cable is connected, the **Found New Hardware Wizard** appears to help you install the AD9911 firmware loader. Click **Next** to continue.
4. Click **Continue Anyway** when the **Hardware Installation** warning window appears.
5. Click **Finish** in the **Found New Hardware Wizard** once the install is complete.
6. Click **Next** when the next **Found New Hardware Wizard** appears to install the EZSSP device.
7. Click **Continue Anyway** when the **Hardware Installation** warning window appears.
8. Click **Finish** in the **Found New Hardware Wizard** once the install is complete.

Once this screen has disappeared, you should notice that the USB **Status LED** (CR2 on AD9911 evaluation board) is flashing, indicating that the evaluation board is connected properly.

LOADING THE SOFTWARE

Follow these three steps to load the AD9911 evaluation software:

1. Before starting the software, make sure that the AD9911 evaluation board is powered up, connected to the computer, and that the **USB Status LED** is flashing.
2. Click the **Start** button, located at the bottom left-hand corner of your desktop.
3. Select **Programs > AD9911 Eval Software folder > AD9911 Eval Software** to load the software.

You are then presented with one of several status messages. These messages are discussed in further detail in the next section, Status Messages upon Loading Software.

Status Messages upon Loading Software

Once the AD9911 evaluation software has been loaded, a green splash screen appears as shown in Figure 3. The status box within the splash screen gives the status of the AD9911 evaluation software. A cursor is provided for easy navigation throughout this box. Green writing in the status box indicates that the software has successfully loaded.
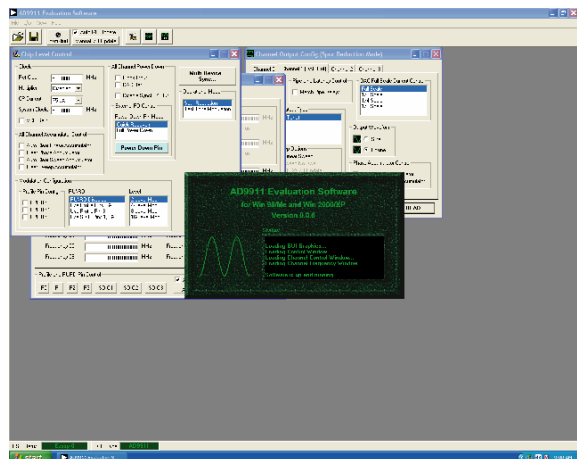

Figure 3. Successful Load

A splash screen with red writing in the status box indicates that the software did not load successfully and an error had occurred (see Figure 4). Scrolling up through the status box with the cursor indicates why the software did not load correctly.

Figure 4. Error Message

Most status message errors can be resolved by checking jumper settings, making sure that the evaluation board is powered up correctly, and inspecting the USB port and cable connections.

When all power, USB port/cable connections, and jumper settings are correct, an error can still appear if the clock input is not properly configured. If this occurs, a pop-up window appears in the center of the splash screen explaining that the software does not recognize the REF CLK input. If this occurs, follow the on-screen instructions (see Figure 5).

Figure 5. REF CLK Not Recognized
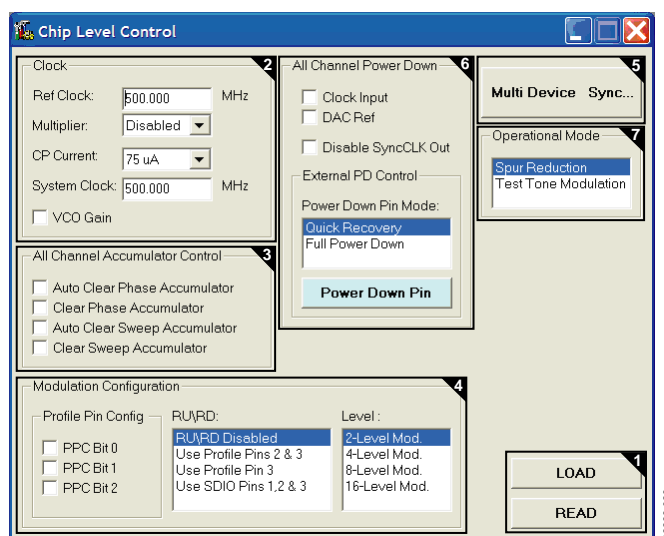
CHIP LEVEL CONTROL WINDOW

Figure 6. Chip Level Control Window

The **Chip Level Control** window is the top cascading window that appears after a successful software load (see Figure 3). This window provides control of the features that affect the primary and auxiliary channels of the AD9911; this window is not channel-specific. The following sections describe the elements of the chip level control window as they are numerically indexed in Figure 6.

1—LOAD and READ

The **LOAD** and **READ** buttons are used to send data and retrieve register settings. All LOAD and READ buttons found in the evaluation software have the same functionality.

When new data is detected, **LOAD** flashes orange, indicating that you need to click **LOAD** to send the updates to the serial I/O buffer where they are stored until an I/O update is issued. The I/O update sends the contents of the serial I/O buffer to active registers.

In the **AD9911 Evaluation Software** main window (see Figure 3), I/O updates can be sent manually (**Manual I/O Update**) or automatically (**Auto I/O Update**). By default, the AD9911 evaluation software is set to **Auto I/O Update**, so that when **LOAD** is clicked, an I/O update signal is automatically sent to the device. If synchronization across channels is desired, use the **Manual I/O Update** button. To do this, clear the **Auto I/O Update** check box and press the **Manual I/O Update** button when you need to send an I/O update (see Figure 7).
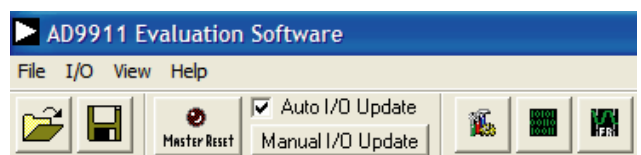

Figure 7.

Click **READ** to perform a readback of the current state of the settings and update the GUI with those settings.

2—Clock

The **Clock** section allows you to configure the reference clock path in the AD9911.

Ref Clock inputs the operating frequency of the external reference clock or crystal. The maximum reference clock frequency of the AD9911 is 500 MHz, which is the default setting of this box. A red outline indicates that the value entered is out of range (see Figure 8).
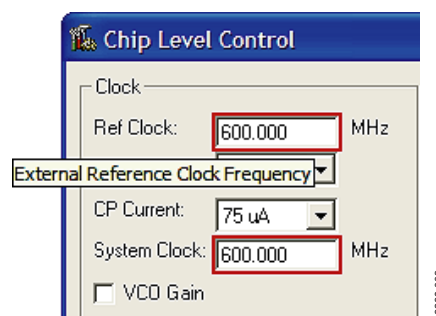

Figure 8.

Multiplier selects the PLL multiplication factor (4× to 20×) by which to scale the input frequency. The default setting of this box is **Disabled**, indicating that the Ref Clock multiplier circuitry is bypassed and the Ref Clock/Crystal input is piped directly to the DDS core.

CP Current selects the charge pump current output of the PLL in the Ref Clock multiplier circuitry. Selecting a higher current output results in the loop locking faster, but there is a trade-off. Increasing this current output also increases phase noise. The default setting of this box is 75 μA.

System Clock displays the operating frequency the DDS core (system). The value shown here is derived from the values entered in the **Ref Clock** and **Multiplier** boxes.

VCO Gain is automatically set when the Ref Clock multiplier is being used to generate a system clock that is greater than 255 MHz. This is done to ensure stability of the Ref Clock multiplier circuitry. A pop-up window appears to alert you to this update (see Figure 9).
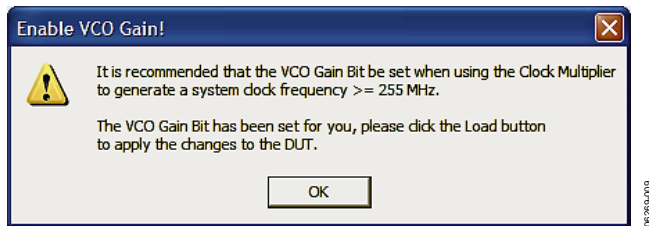
Enable VCO Gain!

It is recommended that the VCO Gain Bit be set when using the Clock Multiplier to generate a system clock frequency >= 255 MHz.

The VCO Gain Bit has been set for you, please click the Load button to apply the changes to the DUT.

OK

Figure 9.

For more information regarding clock modes and operation, refer to the AD9911 data sheet.

3—All Channel Accumulator Control

The **All Channel Accumulator Control** provides control over the phase and sweep accumulators for all channels.

Check the **Auto Clear Phase Accumulator** or **Auto Clear Sweep Accumulator** boxes to clear and release the corresponding accumulator. The auto clear function sets the accumulator to 0 and then begins accumulating.

Select the **Clear Phase Accumulator** or **Clear Sweep Accumulator** to clear and hold the corresponding accumulator. The clear function clears and then holds the contents of the corresponding accumulator to 0 until the box is unchecked.

4—Modulation Configuration

The **Modulation Configuration** section configures the modulation operation of the AD9911.

Profile Pin Config provides access to the PPC bits (FR1[14:12]). These bits are used to control the modulation scheme of the AD9911. **PPC Bit 0** is the LSB (FR1[12]), and **PPC Bit 2** is the MSB (FR1[14]).When a PPC bit is selected, it is set to Logic 1 from its default setting of 0. These bits are discussed in more detail in the AD9911 data sheet.

RU/RD assigns the pins that control the scaling (ramp up/ramp down) of the output amplitude of the AD9911. This feature can be controlled via the profile or SDIO data pins.

Select **Use Profile Pins 2 & 3** if you need to control the RU/RD feature with Profile Pin 2 and Profile Pin 3, or **Use Profile Pin 3** to control this feature using only Profile Pin 3. If you need to

use the SDIO data pins to control this feature, select **Use SDIO Pins 1, 2 & 3**. Note that to use the SDIO pins to control the RU/RD feature, the SDIO RU/RD control jumpers must be placed (see Figure 2). The default setting of this box is **RU/RD Disabled**. In this mode, you are not able to scale the output amplitude.

The AD9911 can be configured to perform many operations in various combinations. For more details regarding the theory of the RU/RD operation and the use of the RU/RD function in combination with the different modes of operation (single-tone, modulation, linear sweep), refer to the AD9911 data sheet.

Level selects the desired level of modulation of the AD9911. The AD9911 can perform 2-level, 4-level, 8-level, or 16-level modulation of frequency, phase, or amplitude (FSK, PSK, ASK).

5—Multi Device Sync…

It is possible to synchronize multiple evaluation boards. Refer to the AD9911 data sheet and the evaluation board schematic (located in the schematic folder of the AD9911 evaluation software CD) for more details on synchronizing multiple AD9911s.

6—All Channel Power Down

The **All Channel Power Down** section allows you to power down all channels collectively using software configurations or the external power-down options found in the **External PD Control** subsection.

Select the **Clock Input**, **DAC Ref**, or **Disable SyncCLK Out** boxes to power down those circuit blocks respectively for each individual channel. Once the selection has been made, click the **LOAD** button to execute the power-down.

When using the **External PD Control,** select from the **Power Down Pin Mode: Quick Recovery** (default setting) or **Full Power Down**. In quick recovery mode, only the digital logic is powered down, whereas all functions are powered down in full power down mode. To execute the power down when using external PD control, you must click the **Power Down Pin**. When pressed, the power down pin is at Logic 1, indicating the powered down mode. When this pin is not pressed, it is at Logic 0, indicating the powered up mode.

7—Operational Mode

The **Operational Mode** section allows you to select the mode of operation. You can choose between **Spur Reduction** for reducing harmonic spurious content or **Test Tone Modulation** for performing an amplitude modulation.
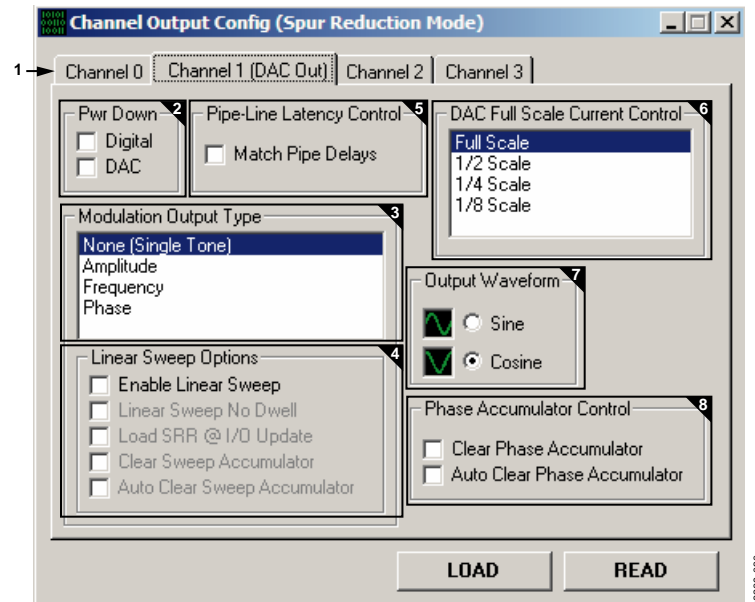
CHANNEL CONTROL WINDOW

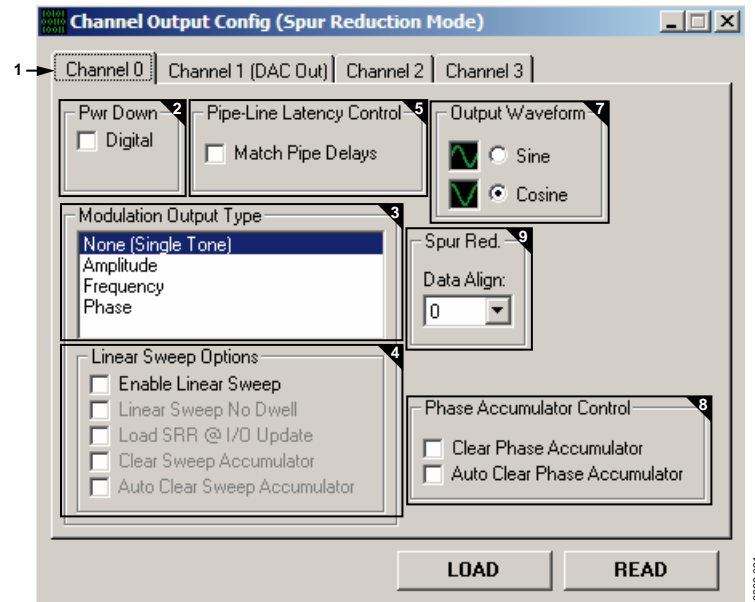Figure 10. Channel Control Window for Channel 1 DAC Out

Figure 11. Channel Control Window for Channel 0, Channel 2, and Channel 3

The **Channel Control** window provides control of the features that affect the AD9911 at a channel-specific level. The following sections describe the elements of the **Channel Control** window as they are numerically indexed in Figure 10 and Figure 11.

1—Channel Select

Use the channel select tabs to select which specific channel options to configure. The AD9911 has four independent channels: **Channel 0**, **Channel 1 (DAC Out)**, **Channel 2**, and **Channel 3**. The default channel select tab setting is **Channel 0**.

Note that Channel 1 is connected to the DAC. Channel 0, Channel 2, and Channel 3 are not connected to the DAC, but

the control in this software allows you to change all of the same variables except the **DAC Full Scale Current Control**.

2—Pwr Down

Use the **Pwr Down** section to power down the digital logic (check **Digital** box) or the DAC circuitry (check **DAC** box). By default, both boxes are unchecked, indicating that the digital logic and the DAC circuitry of that channel are enabled (powered up).

For Channel 1, the DAC can be powered down along with the digital. On Channel 0, Channel 2, and Channel 3, only the digital can be powered down, because those channels are not connected to the DAC.

3—Modulation Output Type

The **Modulation Output Type** box controls what type of modulation is performed on the channel's output. Select **Phase**, **Frequency**, **Amplitude**, or **None (Single Tone)** depending upon the type of modulation you need. The level of modulation for the channel is set using the **Chip Level Control** window under the **Modulation Configuration** section in the **Level** box (see the 4—Modulation Configuration section).

4—Linear Sweep Options

Use the **Linear Sweep Options** section to control the linear sweep features. Select **Enable Linear Sweep** to turn on the linear sweep function and associated options (see Figure 12).
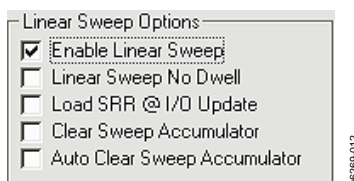

Figure 12.

Select **Linear Sweep No Dwell** to enable this feature. See the AD9911 data sheet for more information regarding the no dwell feature.

When you select **Load SRR @ I/O Update**, the contents of the sweep ramp rate register are loaded into the sweep ramp rate timer every time an I/O_UPDATE is sent to the device.

The **Clear Sweep Accumulator** and **Auto Clear Sweep Accumulator** have the same basic functionality as described in the **All Channel Accumulator Control** section of the **Chip Level Control** window (see the 3—All Channel Accumulator Control section). The difference here is that the function is channel-specific.

See the AD9911 data sheet for a detailed explanation of the linear sweep (shaped) modulation mode.

5—Pipe-Line Latency Control

When you check the **Match Pipe Delays** box in the **Pipe-Line Latency Control** section, the pipeline delay for updates to frequency, amplitude, and phase is equal, but only for the channels operating in single tone mode. The default setting of this box is unchecked, meaning that the pipeline delay for updates to frequency, amplitude, and phase is not equal.

See the AD9911 data sheet for the exact timing delays with and without this feature enabled, and for more information about the single tone mode-matched pipeline delay.

6—DAC Full Scale Current Control

Use the **DAC Full Scale Current Control** section to scale the output current of the DAC to **Full Scale**, **1/2 Scale**, **1/4 Scale**, or **1/8 Scale**. See the AD9911 data sheet for more details about the scalable DAC reference current control mode.

7—Output Waveform

In the **Output Waveform** section, select either a **Sine** or **Cosine** function for the angle-to-amplitude conversion.

8—Phase Accumulator Control

The **Phase Accumulator Control** check box includes **Clear Phase Accumulator** and **Auto Clear Phase Accumulator,** which have the same basic functionality as described in the **All Channel Accumulator Control** section of the **Chip Level Control** window (see the 3—All Channel Accumulator Control section). The difference here is that the function is channel-specific.

9—Spur Red

The **Spur Red** box allows you to set the **Data Align** bit to the number of DAC bits used by the spur reduction signals. The default is set to 0, meaning that the spur reduction signals use 4 bits of the DAC. This value can be set from 0 to 7 to use between 4 and 10 bits of the DAC.
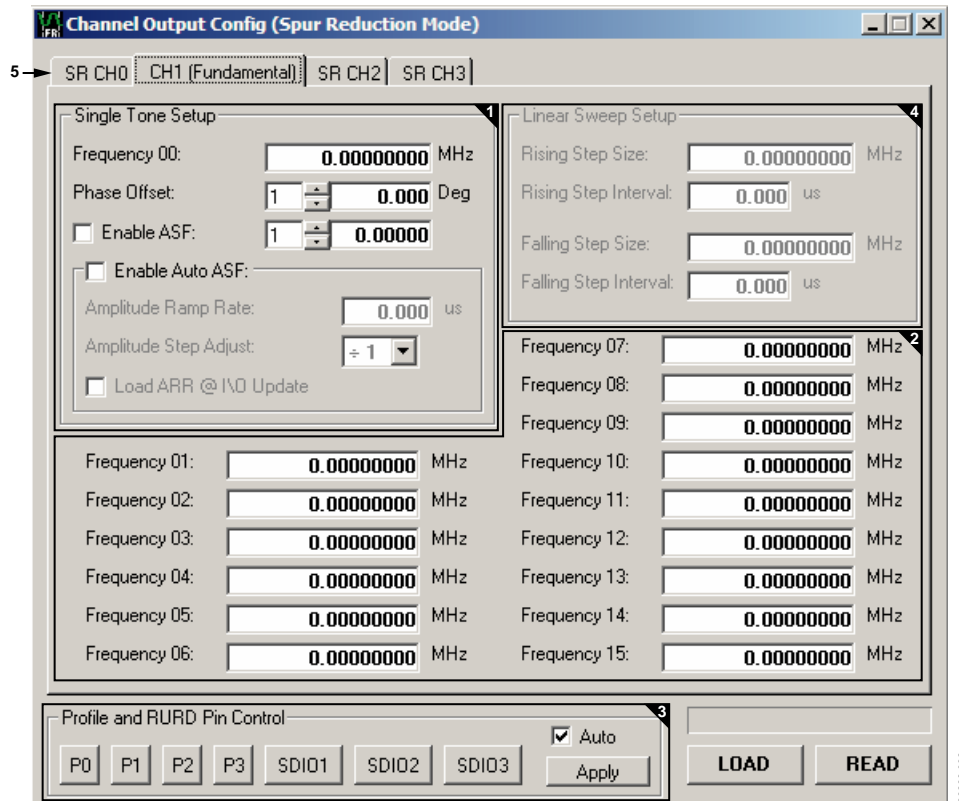
CHANNEL OUTPUT CONFIG

Figure 13. Channel Output Config Window in Spur Reduction Mode

The **Channel Output Config** window configures various output characteristics of the channel(s). **CH1 (Fundamental)** is used for the fundamental channel output. **SR CH0**, **SR CH2,** and **SR CH3** are the spur reduction channels. The following sections describe the elements that are numerically indexed in Figure 13.

1—Single Tone Setup

Use the **Single Tone Setup** section to configure the channel output for the single tone mode of operation (default).

For **CH1 (Fundamental)**, enter the desired output frequency directly in the **Frequency 00** box or double-click the **Frequency 00** box to launch the **Edit output frequency** pop-up box to set the output frequency in the **Frequency** box (see Figure 14). The output frequency can alternatively be set in decimal, hex, or binary format by editing the respective boxes in the **Tuning Word Values** section (see Figure 14). For **SR CH0, SR CH2**, and **SR CH3**, the same can be applied, but there is also a multiplier in front of the frequency entry box. This multiplier sets the frequency for each spur reduction channel to multiples of the fundamental up to the 14th harmonic.
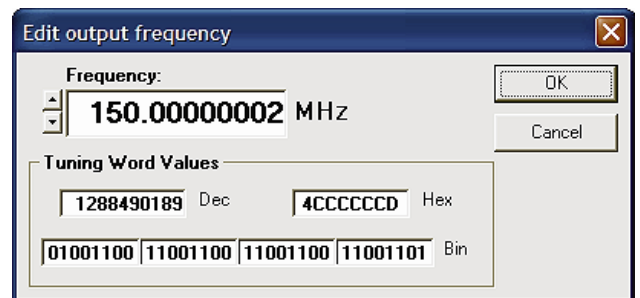

Figure 14. Edit output frequency Pop-Up Box

Note that the **Phase Offset**, **Enable ASF**, **Amplitude Ramp Rate, Frequency 01** to **Frequency 15, Rising Step Size**, **Rising Step Interval**, **Falling Step Size**, and **Falling Step Interval** boxes all offer the edit option shown in Figure 14 by double-clicking their respective boxes.

The **Frequency 00** box also sets the starting point of the linear frequency sweep and the first level in frequency modulation (FSK).

Phase Offset consists of two boxes. In the first box, set the integer factor (1–999) to increment or decrement the phase offset. The default setting of this box is 1, indicating that the phase offset is incremented/decremented by 0.022° when pressing the up or down arrow keys. The value of 0.022° is derived from the following equation:

$$Interger\ Factor \times \left(\frac{1}{2^{(14\ bits\ of\ phase\ resolution)-1}} \right) \times 360°$$

Therefore, entering a factor of 3 in the first box allows you to increment/decrement the phase offset by .066° In the second box, input the desired phase offset (from 0° to 360°) of the output signal.

The **Phase Offset** box also represents the starting point of the linear phase sweep and the first level in phase modulation (PSK).

To use the output amplitude scalar, the **Enable ASF** box must be checked. In the first box, set the integer factor (1 to 999) to increment or decrement the amplitude scale factor. The default setting of this box is 1, meaning the output amplitude is scaled up/down by 0.00098 when pressing the up or down arrow keys. The value of 0.00098 is derived from the following equation:

$$Interger\ Factor \times \left(\frac{1}{2^{(10\ bits\ of\ output\ amplitude\ scalar\ resolution)-1}} \right)$$

In the second box, set the desired output amplitude scale factor (between 0 and 1) of the output signal, where 1 is equivalent to full scale.

The **Enable ASF** box also represents the starting point of the linear amplitude sweep and the first level in amplitude modulation (ASK). Note that when performing linear amplitude sweeps, the **Enable ASF** box must be left unchecked.

When using the RU/RD feature, the **Enable Auto ASF** box must be checked. Once checked, the **Amplitude Ramp Rate**, **Amplitude Step Adjust**, and the **Load ARR @ I\O Update** options become available (see Figure 15).
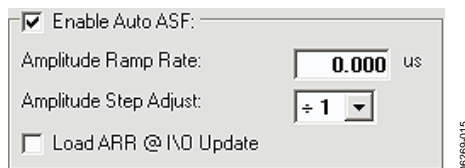
Figure 15.

Use the **Amplitude Ramp Rate** box to set the Amplitude Ramp Rate (ARR) time. This time (entered in µs) can range from a minimum value of

$$\left(\frac{1}{SYNC\ CLK} \right) \times 1$$

to a maximum value of

$$\left[\left(\frac{1}{SYNCCLK} \right) \times 2^{(8\ bits\ of\ output\ ramp\ resolution)-1} \right]$$

This implies that if the system clock is 500 MHz, the ARR value can range from 8 ns (minimum) to 2.040 µs (maximum). If the value entered exceeds the maximum time, a pop-up window appears, alerting you that the value entered is changed to the appropriate maximum value.

In the **Amplitude Step Adjust** box, select the amplitude scale factor step size. The default setting of this box is 1, indicating that step size is 1 LSB.

Select **Load ARR @ I\O Updat**e to load the contents of the amplitude ramp rate register into the amplitude ramp rate timer every time an I/O_UPDATE is sent to the device.

2—Profile Registers

The AD9911 features up to 16 programmable registers per channel as shown in Figure 13. Because of certain channel constraints, however, there are limitations on how the profile registers can be used in some configurations. This is further described in the AD9911 data sheet.

Use the **Frequency 01** to **Frequency 15** boxes to enter the information needed for modulation (FSK, PSK, or ASK) and linear sweep modes of operation. Upon default, these profile registers are configured for frequency inputs, but the registers can be changed to intake phase or amplitude information by selecting the desired modulation type in the **Modulation Output Type** box in the **Channel Control** window (see the 3—Modulation Output Type section). Figure 16 shows how the profile registers appear when phase modulation (PSK) is selected.
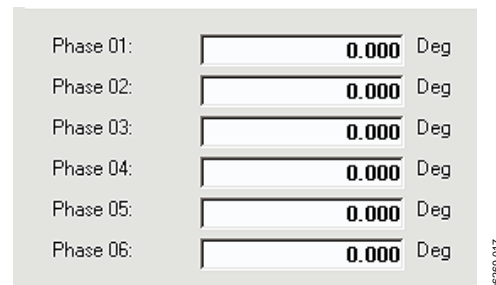
Figure 16.

When the channel is in the modulation or linear sweep mode of operation, input the starting frequency in the **Frequency 00** box, the starting phase in the **Phase Offset** box, and the starting amplitude in the **Enable ASF** box (see the 1—Single Tone Setup section). In modulation mode, use the **Frequency 01** to **Frequency 15** boxes to input frequency, phase, or amplitude information for the level of modulation selected. For instance, if 4-level frequency modulation is selected, input the starting frequency in the **Frequency 00** box, second frequency in the **Frequency 01** box, third frequency in the **Frequency 02** box, and fourth frequency in the **Frequency 03** box. See Figure 17 for an example of selecting 2-level frequency modulation.
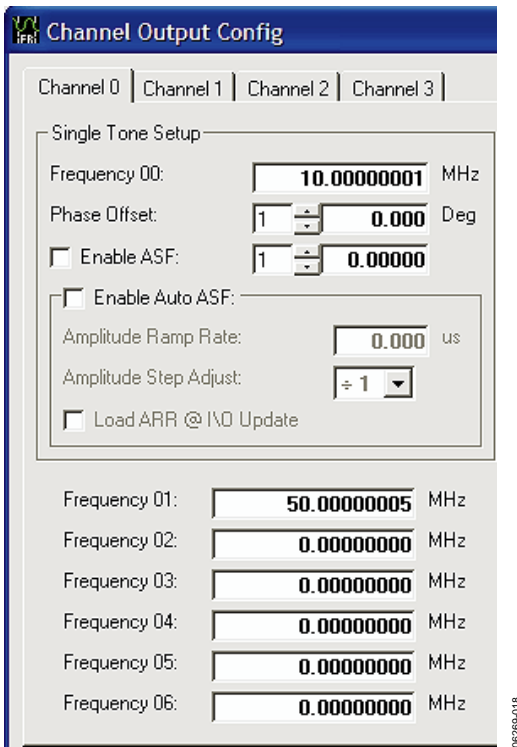
Figure 17.

In the linear sweep mode of operation, only the box (**Frequency 01**, **Phase 01**, or **Amplitude 01**) is used. It indicates the ending point of the sweep. In Figure 17, the frequency linear sweep begins at 10 MHz and ends at 50 MHz.

3—Profile and RURD Pin Control

The **Profile and RURD Pin Control** section covers the profile pins (**P0**, **P1**, **P2**, and **P3**) and SDIO data pins (**SDIO1**, **SDIO2**, and **SDIO3**). The profile pins can be configured to control modulation, linear sweep, or RU/RD operations, whereas the SDIO data pins can only control the RU/RD operation. To perform the desired modulation, linear sweep, or RU/RD operation, click the profile/SDIO data pin(s) associated with that operation. When these pins are pressed, they are set to Logic 1 (see Figure 18).
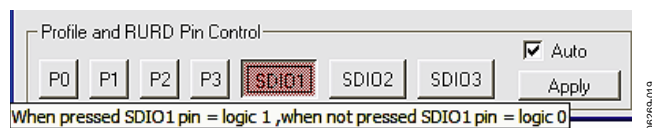

Figure 18.

Upon default, the **Auto** box is checked, meaning that once you click one of the pins (profile or SDIO), the action executes. If this box is unchecked, the **Apply** button must be clicked before the desired action is carried out. The **Apply** button mimics the **LOAD** button; it flashes orange when new data is detected (see the 1—LOAD and READ section). All changes and updates occur simultaneously when **Apply** is clicked.

If performing a 2-level frequency modulation with no RU/RD and with the same configurations as shown in Figure 17, **P0** is used to control the modulation on CH0 (see the AD9911 data sheet for more information). Therefore, the output of CH0 stays at 10 MHz until the **P0** button is pressed. Once **P0** is selected, the frequency changes to 50 MHz. To return to 10 MHz, clear the **P0** button.

For more information regarding the use of the profile and SDIO data pins to control various modulation, linear sweep, and RU/RD schemes, refer to the AD9911 data sheet.

4—Linear Sweep Setup

Use the **Linear Sweep Setup** section to setup the slope of the linear sweep. In the **Rising Step Size** box, enter the desired value for the rising step size. Input the amount of time needed to be spent at each step in the **Rising Step Interval** box.

Input the desired falling step size in the **Falling Step Size** box, and the time that should be spent at each step in the **Falling Step Interval** box. The **Rising Step Size** and **Falling Step Size** boxes are similar to the profile registers (**Frequency 01** to **Frequency 15**); upon default, they are set up for frequency inputs. However, these boxes can be changed to intake phase or amplitude information by selecting the type of linear sweep desired in the **Modulation Output Type** box in the **Channel Control** window (see the 3—Modulation Output Type section).

The range of the rising/falling step interval is computed similar to the time range for the **Amplitude Ramp Rate**. Note that the **Rising Step Interval** and **Falling Step Interval** boxes also have the pop-up window feature exhibited in Figure 15 when the maximum rising/falling step interval value is exceeded.

For more information regarding linear sweep setup, refer to the AD9911 data sheet.

5—Spur Reduction Channel Select

Use these tabs to select between the fundamental channel and the spur reduction channels. **CH1 (Fundamental)** is used for the fundamental channel output. **SR CH0**, **SR CH2**, and **SR CH3** are the spur reduction channels. All options available on the fundamental channel are also available on each of the spur reduction channels. See the Spur Reduction section for more information.

These tabs become the tabs to select the channel used in the test tone modulation mode. CH1 is still the fundamental channel. AM CH0 is used for amplitude modulation. See the Test Tone Modulation section for more information.

DEBUG

To access the **Debug Window** from the **AD9911 Evaluation Software** window, click **View** and select **Debug Window** (see Figure 19).
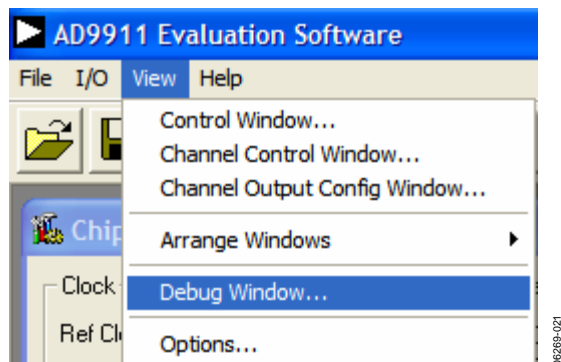
Figure 19.

The **Debug Window**, shown in Figure 20, lets you write directly to any of the AD9911 internal registers and subsequently read them back. Use **View Channel** in the **Serial I/O** section to select which channel's internal registers you need to view. The default setting of this box is Channel 0. To access the internal registers of the selected channel, use the **RegAddr** drop menu to select which register(s) you need to read/write. You can also directly turn off or turn on the states of any external input pins, such as the profile pins (**P1** to **P4**) or SDIO data pins (**SDIO_0** to **SDIO_3**).
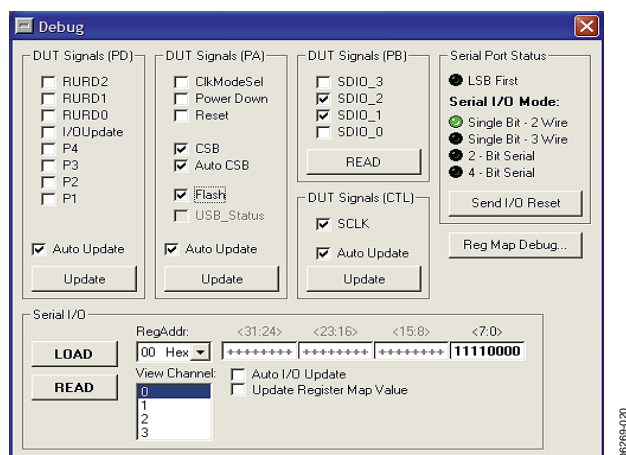

Figure 20. Debug Window

DUT I/O Box

To access the **DUT I/O** box, click **I/O** drop down menu (left of **View** (in Figure 19) and select **DUT I/O**.

The **DUT I/O** dialog box (see Figure 21) controls the I/O configuration for the device. Click **I/O Reset** to send an I/O reset to the corresponding serial port state machine. Select **LSB First** to change the data format to LSB first from the default setting of MSB first. Use the **Serial I/O Mode** drop down menu to select the desired serial I/O mode of operation: **Single Bit - 2 Wire** (default), **Single Bit - 3 Wire**, **2 - Bit Serial**, or **4 - Bit Serial**. For more information about the serial I/O modes of operation, refer to the AD9911 data sheet.
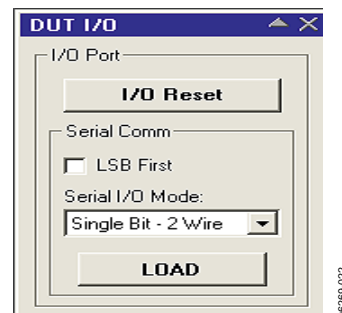

Figure 21. DUT I/O Dialog Box

SPUR REDUCTION

The AD9911 DDS is equipped with spur reduction technology that enables digital reduction of output spurs using up to three auxiliary DDS cores or channels (CH0, CH2, and CH3). Using an auxiliary channel, the targeted output spur for reduction must be duplicated in frequency, approximate magnitude, and be 180° out of phase. Typically, only spurs harmonically related to the output fundamental frequency can be exactly matched in frequency. The lower order fundamental harmonics are typically the worst case spurs in the output, including aliased harmonics of the fundamental. Spur reduction is not as effective at lower fundamental frequencies (CH1) where SFDR performance is already greater than −65 dBc.

Spur Reduction Instructions

The following instructions use the AD9911 evaluation board and evaluation board software. In addition, the data sheet is available for reference.

1. After power-up, reset the part and apply the **Ref Clock** source. Using the **Chip Level Control** window (see Figure 6), enter the **Ref Clock** frequency. Next, check both the **Auto Clear Phase Accumulator** and **Disable SyncCLK Out** box. Click **LOAD**. Note that without the **Auto Clear Phase Accumulator** box checked, spur reduction settings are invalid for file save and reload use later.
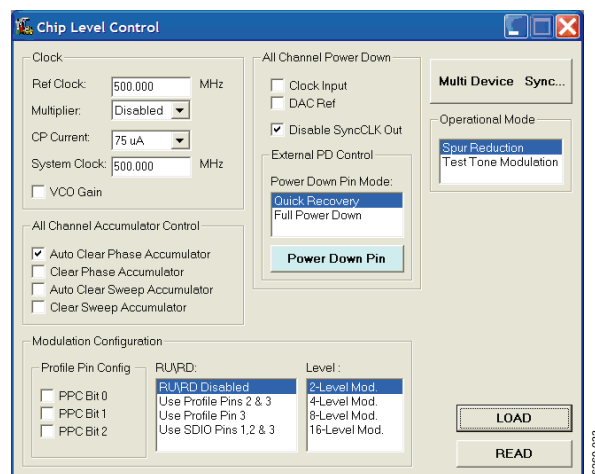

Figure 22.

2. Using the **Channel Output Configuration** window (see Figure 13), enter the desired fundamental frequency (**CH1 Fundamental** tab) directly into the **Frequency 00** box by double-clicking the box. Click **LOAD**. If you intend to use the auto scale factor (**Enable ASF**), enter the value now. Click **LOAD**.

3. Using a spectrum analyzer, find the most problematic spur. The spur must be a harmonic of the fundamental or an aliased harmonic of the fundamental. **SR CH0**, **SR CH2**, and **SR CH3** are the designated spur reduction channels.

4. Select the tab for spur reduction channel **SR CH0** in the **Channel Output Configuration** window. Enter the frequency for **SR CH0** slightly offset from the harmonic spur frequency targeted. (100 KHz offset works well). Check **Enable ASF** box for **SR CH0** and set the scaling factor to 1. Click **LOAD**.

5. Adjust the amplitude of **SR CH0** to match that of the harmonic spur. Note that the spur reduction default produces a signal with approximately −63 dBm amplitude. To reduce spurs greater than −63 dBm, the data align function must be used. Each data align bit adds 6 dB to the amplitude of the spur reduction signal. This is set on the **Channel Control** window. Select the same channel that is being used for spur reduction (see the 9—Spur Red section).

6. Once the amplitude is matched, reset the frequency of the spur reduction signal exactly the same as the harmonic. The software autocalculates the harmonic frequency out to the 14th harmonic. Use the drop-down menu next to the frequency box to access the autocalculated values (see Figure 13).

7. Next, the phase must be matched to 180° of the phase of the harmonic spur. To find the optimal phase relationship, start by entering in the phase in 90° increments, that is, 0°, 90°, 180°, and 270°. Pick the phase that gives the lowest amplitude and use it as a starting point. Once that point is found, adjust the phase offset word until the spur is maximally reduced.

8. Repeat steps 3 through 7 with **SR CH2** and **SR CH3** as needed.

Repeatability and Other Issues

By using the Spur Reduction Instructions, spur reduction is repeatable and reliable. This process has been tested over supply and temperature; the spur reduction holds up well under those conditions. There are some known issues using a specific setting across multiple parts. This is related to an amplitude variation in harmonic spurs across parts. Because this process is very specific to amplitude, any variation in amplitude can cause worse than expected performance across parts. Any variation in

spur reduction performance is expected across parts. Best performance can be achieved by using a part that has average harmonic performance and tuning the settings to that one part and using it for all parts. The other option is to optimize each part independently.

One known issue concerning spur reduction is the introduction of other spurious content as the other DDS cores are activated. As each core is turned on, other spurs appear in the spectrum. These spurs appear random in nature and are typically insignificant. They may not have a direct effect on SFDR performance due to nonharmonically related spurious content from the fundamental. This is illustrated in Figure 23 and Figure 24.

Figure 23 and Figure 24 show the change resulting from spur reduction. The output fundamental frequency is 197.7 MHz. The 2nd and 3rd harmonics fold back to 104.6 MHz and 93.1 MHz, respectively. The spurs have been virtually eliminated. The plots show wide band and narrow band before and after spur reduction. Only the 2nd and 3rd harmonics are reduced in Figure 24.
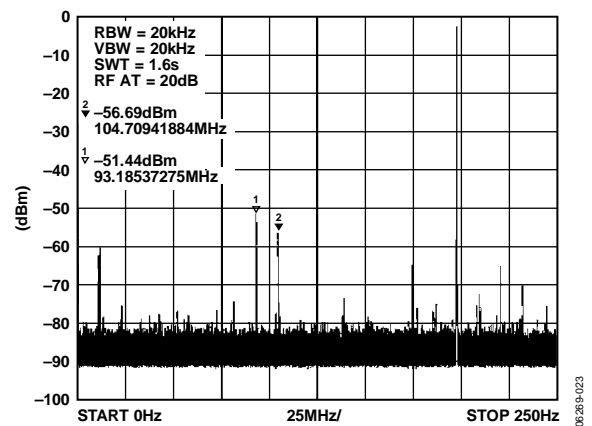

Figure 23. Wideband Spectrum Before Spur Reduction
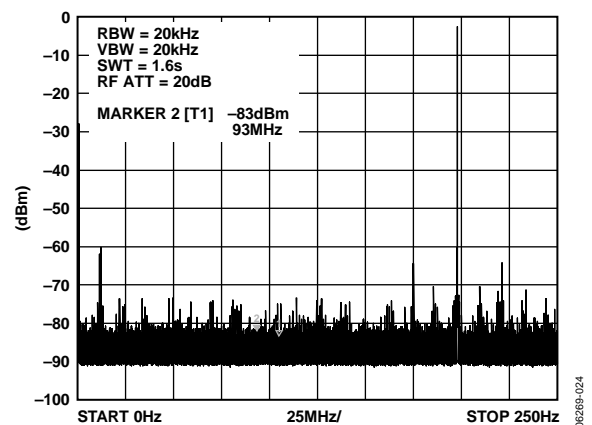

Figure 24. Wideband Spectrum After Spur Reduction

TEST TONE MODULATION

Use the following instructions for test tone modulation:

1. Power up or reset the part. Using the **Chip Level Control** window, set the **Operational Mode** to **Test Tone Modulation**.
2. Using the **Channel Output Config** window (see Figure 13), click the **CH1 (Fundamental)** tab. Type in the fundamental frequency and amplitude.
3. AM CH0 is the DDS channel used for amplitude modulation.
4. For AM, select the **AM CH0** tab (see Figure 25). Set the frequency offset in MHz in the **Frequency 00** box. This frequency is set to an offset of the fundamental. For example, if 1 MHz is entered, the modulation is offset 1 MHz from the fundamental.
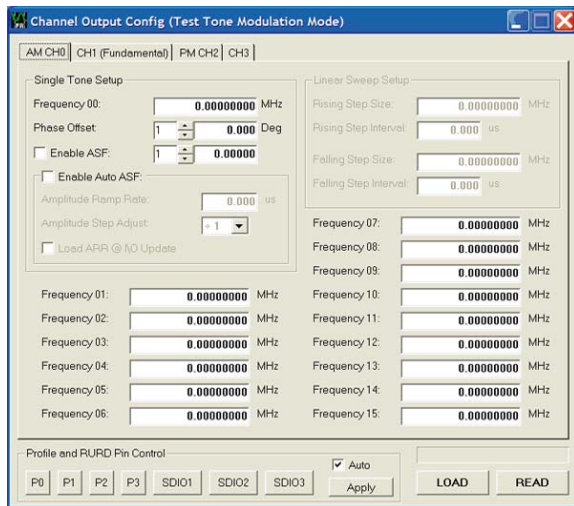
Figure 25.

5. Using the auto scale factor, the amplitude of the modulation signal can be varied. To do this, check the **Enable ASF** box and set the scaling factor to the right. This value varies from 0 to 1.
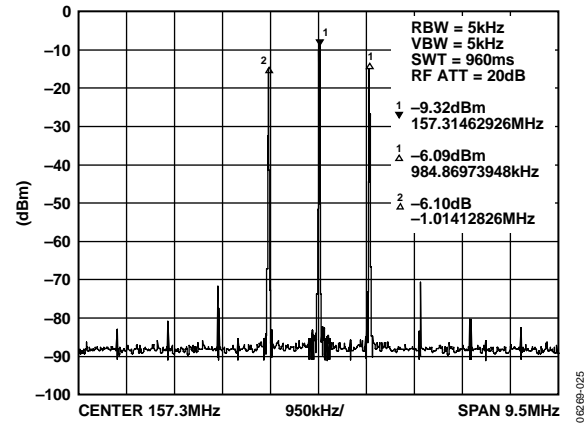
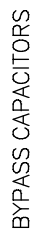*Figure 26. Example of AM with 1 MHz Offset*

SCHEMATIC

06269-035

Figure 27. AD9911/PCB Schematic, Page 1
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DAC OUT/FILTER IN

J1

DAC1_OUT

R23
0

R22
0

200 MHz LOW PASS FILTER

GND C88 8.2PF

C81 0.75PF

L9 56NH

GND C86 12PF

L7 47NH

C90 5PF

GND C85 10PF

C89 10PF

L8 33NH

GND C87 5PF

C91 8.2PF GND

C84 12PF GND

C82 10PF GND

C83 5PF GND

DAC FILTER OUT

J5

OPTIONAL POWER PLANE STITCH

R49 0

R48 0

R47 0

R46 0

R45 0

R44 0

AVDD

CLK_VDD

R43 0

R42 0

R41 0

R40 0

R39 0

R38 0

CLK_VDD

BG_VDD

POWER SUPPLY CONNECTION

DVDD

C37 10UF

GND

DVDD_IO

C47 10UF

GND

VCC_USB

C35 10UF
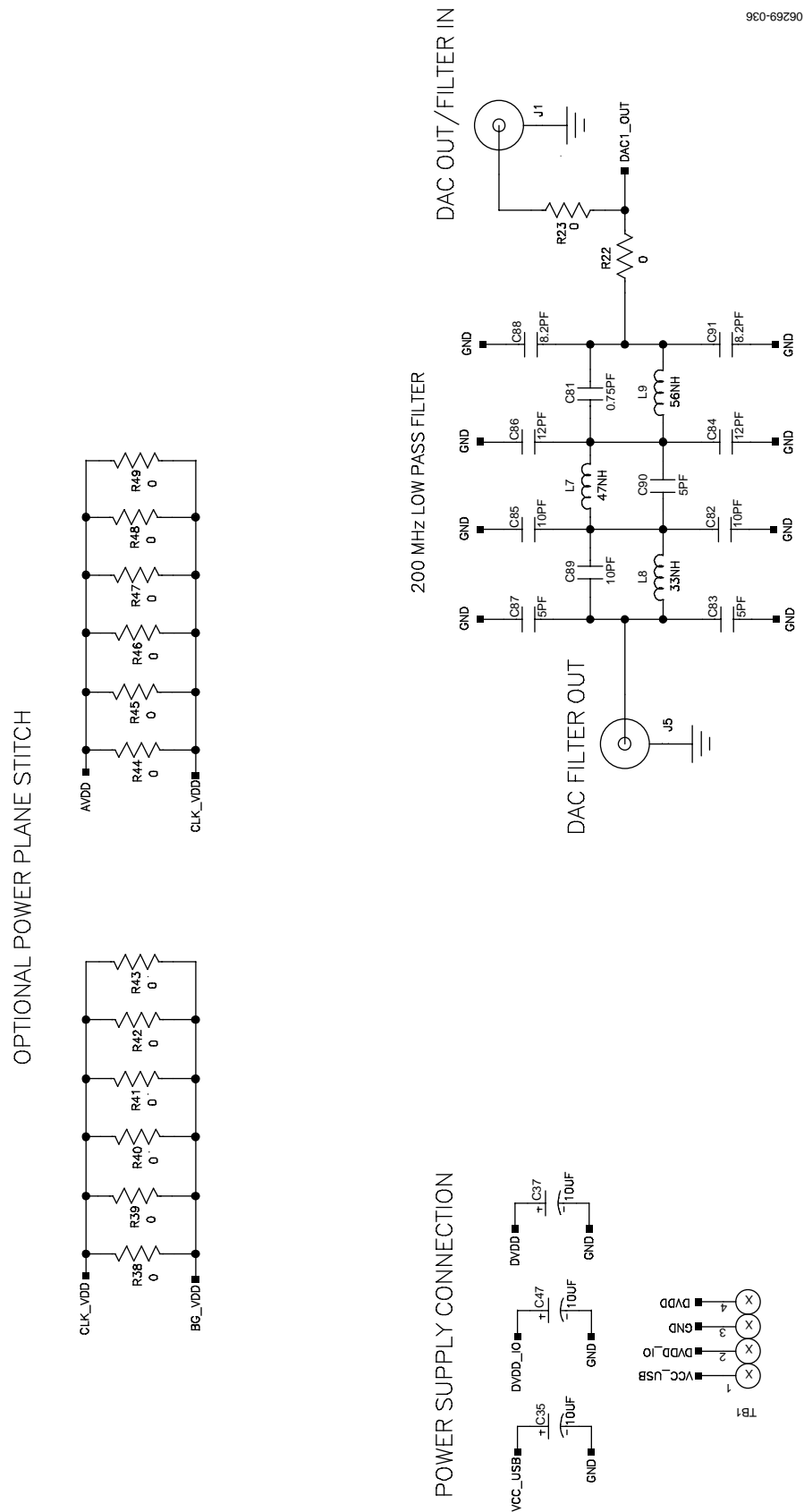
GND

TB1

1 VCC_USB
2 DVDD_IO
3 GND
4 DVDD
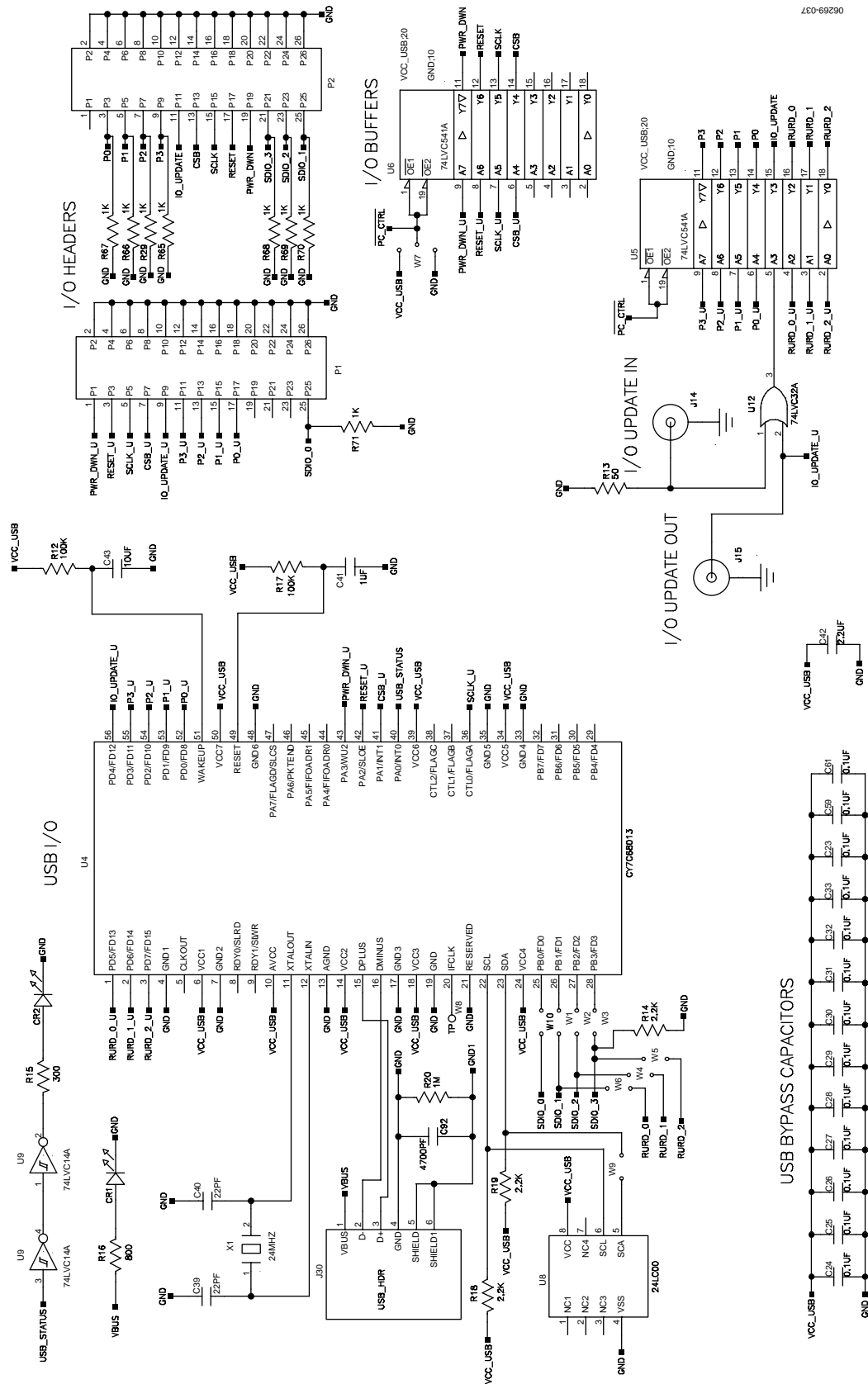
Figure 28. AD9911/PCB Schematic, Page 2

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Figure 29. AD9911/PCB Schematic, Page 3

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
AD9911/PCB	Evaluation Board
AD9911/PCBZ[1]	Evaluation Board

[1] Z = Pb-free part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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