ADP1051-240-EVALZ/ADP1050DC1-EVALZ User Guide
UG-664

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

240 W Evaluation Board Kit for the ADP1050, Digital Controller for Isolated Power Supply with PMBus Interface

FEATURES

Full support evaluation kit for the ADP1050
240 W full bridge topology
Input voltage range: 36 V dc to 75 V dc
Output voltage: 12 V dc
Nominal output current: 20 A
Synchronization as slave device
On-board tests for housekeeping functions
LED indicated key status
PMBus communication
Graphical user interface (GUI) software

EVALUATION KIT CONTENTS

ADP1051-240-EVALZ evaluation board
ADP1050DC1-EVALZ daughter card
CD with ADP1050-51 GUI installer, ADP1050 data sheet, ADP1051-240-EVALZ/ADP1050DC1-EVALZ (UG-664) user guide, and schematics and bill of materials for the ADP1051-240-EVALZ and ADP1050DC1-EVALZ

ADDITIONAL EQUIPMENT/SOFTWARE NEEDED

ADP-I2C-USB-Z USB-to-I²C connector
ADP-I2C-USB-Z drivers CD

GENERAL DESCRIPTION

The ADP1051-240-EVALZ evaluation board, together with an ADP1050DC1-EVALZ daughter card, allows the user to evaluate the ADP1050 in a power supply unit (PSU) environment. The boards are fully compatible with the ADP1050-51 GUI software. With the ADP-I2C-USB-Z USB-to-I²C connector and the GUI software, the ADP1050 on the evaluation board can be interfaced with a PC via a USB port.

The evaluation board allows the ADP1050 to be exercised without the need for external components. The board is set up to act as an isolated PSU, outputting a rated load of 12 V, 20 A from a 36 V dc to 75 V dc source.

Multiple test points allow easy access to all critical points/pins. Three LEDs give the user a direct visual indication of variations in the board status, such as the system input voltage, PGOOD output, and FLAGIN input.

Full performance details are provided in the ADP1050 data sheet, which should be consulted in conjunction with this user guide.

EVALUATION BOARD SETUP

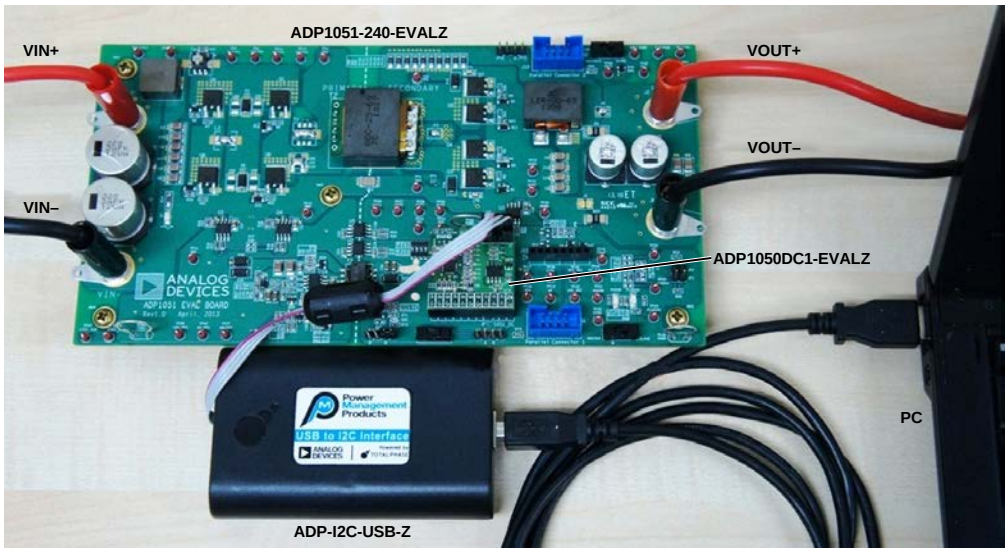


Figure 1. ADP1051-240-EVALZ Evaluation Board Setup with ADP1050DC1-EVALZ Daughter Card and ADP-I2C-USB-Z USB-to-I²C Interface

TABLE OF CONTENTS

REVISION HISTORY

1/14—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADP1051-240-EVALZ evaluation board can be used as an evaluation tool for the ADP1050 and the ADP1051. The ADP1051-240-EVALZ evaluation board and the ADP1050DC1-EVALZ daughter card feature the ADP1050 in a dc-to-dc switching power supply in full bridge topology with synchronous rectification. Figure 2 shows a photograph of the evaluation board hardware. Figure 4 shows a block diagram of the main components on the board. The circuit is designed to provide a rated load of 12 V, 20 A from a dc input voltage source of 36 V dc to 75 V dc. The ADP1050 provides functions such as output voltage regulation, synchronization, prebias startup, and comprehensive protection.

The main transformer on the evaluation board breaks the dc-to-dc power supply into primary side and secondary side, creating isolation. On the primary side, the full bridge stage switches and inverts the dc voltage derived from the input terminals (J1 and J5) into ac voltage. The control signals for the full bridge stage come from the ADP1050 through the digital isolators (ADuM3210) and the half bridge drivers. There is also a current transformer (CT) sensing and transmitting the primary side current information to the ADP1050 on the secondary side.

On the secondary side, the full wave synchronous rectifiers (SRs) rectify the ac voltage to dc voltage. An LC filter smooths the pulsated dc voltage. The output terminals, J2 and J6, are used for the load connection.

The ADP1050DC1-EVALZ daughter card shown in Figure 3 can be plugged into the ADP1050/ADP1051 daughter card connector (J8). It provides the signals that are used to regulate the output voltage, limit the output current, and control the on/off switch of the evaluation board. A 4-pin connector (J2) on the daughter card is used for I^{2}C/PMBus™ communication through a USB-to-I^{2}C connector, ADP-I2C-USB-Z. This allows the GUI software to communicate with the evaluation board through the USB port of the PC. If the J17 or J18 parallel connector is connected, the GUI can visit all the evaluation boards through a single USB-to-I^{2}C connector. With this interface, users can monitor and program the ADP1050.

An auxiliary power supply on the evaluation board is used to generate a 10 V bias power on the primary side (10V_PRI) for full bridge drivers, a 5 V bias power on the primary side (5V_PRI) for the primary side power supply of the ADuM3210, and a 10 V bias power on the secondary side (10V_SEC) for the ADP3654 driver (see Figure 4). A 10 V bias power (10V_VCC) is generated from an OR-diode network using a 10 V bias power on the secondary side (10V_SEC) and a 5 V voltage source from the USB-to-I^{2}C connector (see Figure 4). This allows the GUI access to the ADP1050 when the auxiliary power circuit is not powered up. The ADP3303 LDO converts the 10V_VCC to a 3.3 V bias power on the secondary side (3V3_SEC) for the ADP1050 and the secondary side power of the ADuM3210. Alternatively, the auxiliary power input can also come from an independent dc source through TP47 and TP50.

There are three blue LEDs on the evaluation board to provide the status of the evaluation board. D7 indicates the input voltage signal. D17 indicates the PGOOD output (PG/$\overline{\text{ALT}}$ pin output signal). D18 indicates the FLAGIN signal.

There are three complete switches on the evaluation board. The SW1 switch is used to control the voltage level of the hardware CTRL pin. The SW2 and SW3 switches are used to change the part operating state to master or slave when synchronization is enabled.

Figure 2. ADP1051-240-EVALZ Evaluation Board

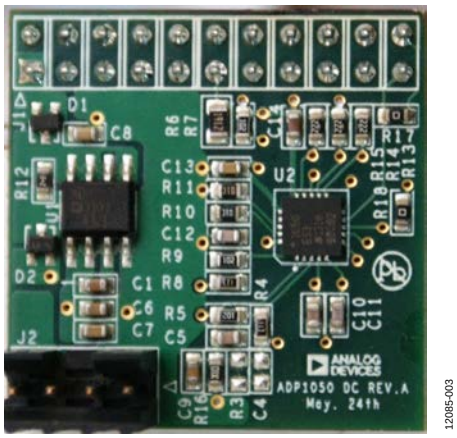


Figure 3. ADP1050DC1-EVALZ Daughter Card

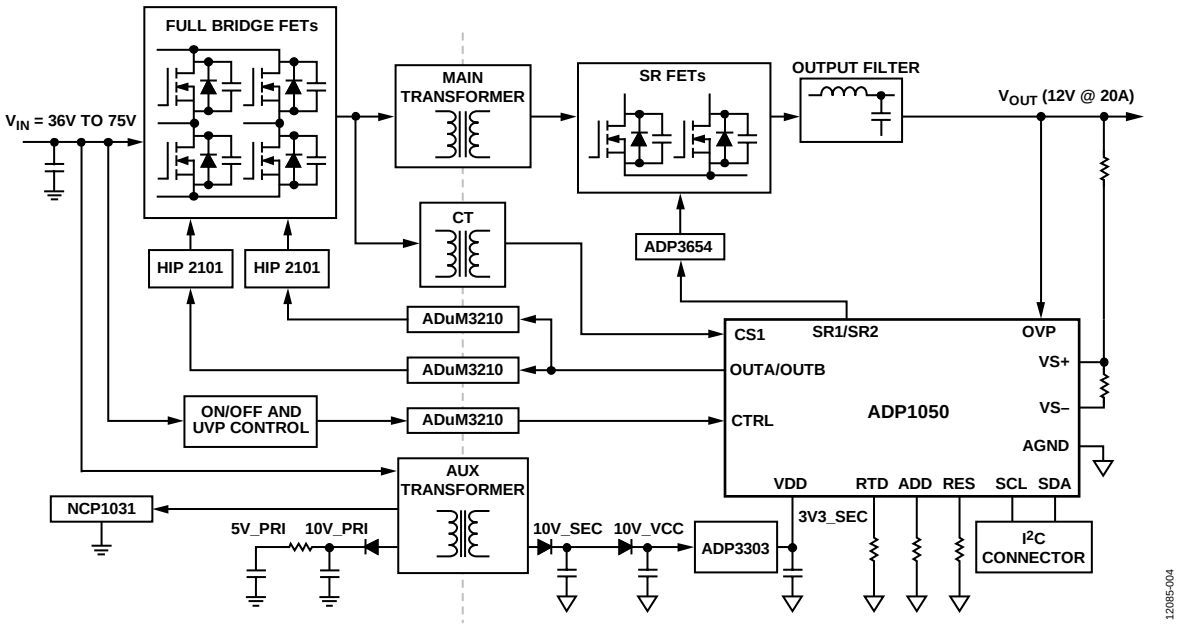


Figure 4. Block Diagram of ADP1050 Evaluation Board System

EVALUATION BOARD CHARACTERISTICS

Table 1. Evaluation Board Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE	V_{IN}	36	48	75	V dc	
OUTPUT VOLTAGE SETPOINT	V_{OUT}		12		V dc	
V_{OUT} Overvoltage Fault Limit (Default)			14		V dc	
Output Voltage Ripple			200		mV	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A
OUTPUT CURRENT	I_{OUT}	0		20	A	
I_{OUT} Overcurrent Fault Limit (Default)			25			
OPERATION TEMPERATURE	T_A		25	50	°C	Natural convection
			25	85	°C	Airflow = 200 LFM or above
Overtemperature Fault Limit (Default)	T_{OT_FAULT}		110		°C	
EFFICIENCY	η		94.5		%	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 20 A
SWITCHING FREQUENCY	f_{SW}		120		kHz	
DIMENSION						
Width	W		210		mm	
Length	L		110		mm	
Component Height	H		40		mm	

CONNECTORS

The connections to the ADP1051-240-EVALZ evaluation board are shown in Table 2. Table 3 and Table 4 show the details about these connectors.

Table 2. Evaluation Board Connections

Connector	Function
J1	VIN+, dc input
J5	VIN–, ground return for dc input
J2	VOUT+, dc output
J6	VOUT–, ground return for dc output
J8	ADP1050/ADP1051 daughter card connector
J15	Analog current share daughter card connector[1]
J17	Parallel Connector 1[1]
J18	Parallel Connector 2[1]

[1] For ADP1051 only.

ADP1050/ADP1051 Daughter Card Connector (J8)

The connections to J8 are shown in Table 3.

Table 3. J8 Connections

Pin	Function
1	10V_VCC
2	VS–
3	VS+
4	CS2–[1]
5	CS2+[1]
6	VF
7	CS1
8	SR1
9	SR2
10	OUTA
11	OUTB
12	OUTC[2]
13	OUTD[3]
14	SCL
15	SDA
16	CTRL
17	PG/$\overline{\text{ALT}}$
18	SYNI/FLGI
19	3V3_SEC
20	AGND
21	RTD
22	OVP

[1] For ADP1051 only. These pins are left unconnected for the ADP1050.
[2] In the ADP1050DC1-EVALZ daughter card, this pin (OUTC) is connected to the OUTB pin of the ADP1050.
[3] In the ADP1050DC1-EVALZ daughter card, this pin (OUTD) is connected to the OUTA pin of the ADP1050.

Daughter Card I²C/PMBus Connector (J2)

The connections to J2 in the ADP1050DC1-EVALZ daughter card are shown in Table 4.

Table 4. J2 Connections

Pin	Function
1	5V
2	SCL
3	SDA
4	AGND

HARDWARE CONNECTION

Caution

This evaluation board is supplied with high voltages and currents. Take extreme caution, especially on the primary side, to ensure safety for the user. It is strongly advised to switch off the evaluation board when it is not in use. A current-limit dc source is recommended to use as the input.

Required Equipment

- DC power supply capable of 36 V dc to 75 V dc, 10 A output
- Electronic load capable of 12 V, 25 A input
- Oscilloscope capable of 500 MHz bandwidth or higher
- PC with Microsoft Windows® XP (32-bit), Windows Vista (32-bit), Windows 7 (32-bit), or Windows 8 (32-bit)
- Precision digital multimeters (6-digit HP34401 or equivalent)
- Portable digital multimeters (fluke) for measuring up to 25 A dc current
- ADP-I2C-USB-Z USB-to-I²C connector (see Figure 5) available from Analog Devices, Inc.

Figure 5. ADP-I2C-USB-Z USB-to-I²C Interface Connector

Evaluation Board Configurations

There are a series of jumpers used for ADP1051-240-EVALZ hardware settings. All the jumper configurations have been completed during the evaluation board assembly. Table 5 shows the details of jumper configurations.

T1 and T4 are current transformers for primary side current sense. Typically, T4 is used while T1 is not connected by default.

Users do not need to complete any additional hardware configuration unless special test items will be conducted.

Connecting the Hardware

Do not connect the ADP-I2C-USB-Z connector to the evaluation board until after the GUI software has been installed.

Figure 6 shows the test configuration of the evaluation board. The digital multimeters are optional. An independent dc source can be applied on TP47 and TP50 to generate all bias power supplies even if the dc input is lower than 30 V. The board evaluation can start when the dc input voltage is increased from 0 V.

Table 5. Jumpers Configuration

Jumper	Function
JP1	Short this jumper to short R46. This jumper can be used as a signal injection point during the control loop test. It is open by default.
JP2	Short this jumper to short R53. It is open by default.
JP3	When SW1 is used to control the PSU, short this jumper. It is shorted by default.
JP4	When multiple evaluation boards are connected in parallel, proper configuration of this jumper allows a single switch to control all evaluation boards. It is shorted by default.
JP5	Short this jumper to configure the CTRL pin so that the ADP1050 is in the off state. This jumper is open by default.
JP11	This jumper is not used by the ADP1050.
JP12	This jumper is not used by the ADP1050.
JP13	This jumper is not used by the ADP1050.
JP14	This jumper is not used by the ADP1050.

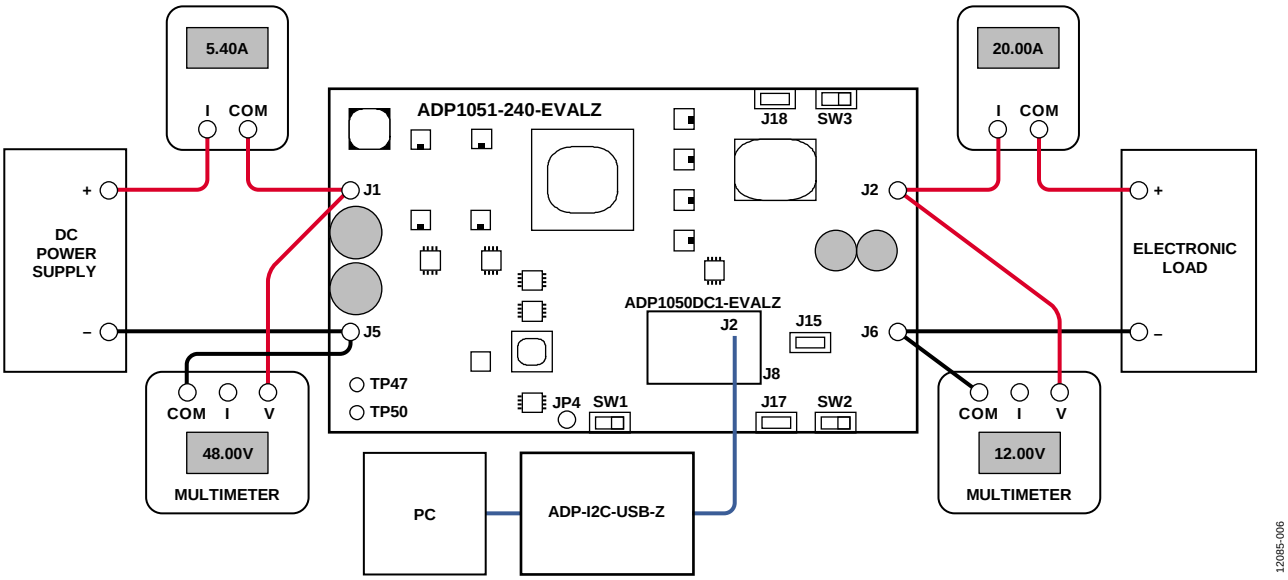


Figure 6. Test Configuration for the Evaluation Board

EVALUATION BOARD GUI SOFTWARE

OVERVIEW

The ADP1050-51 GUI is a free software tool for programming and configuring the ADP1050 and ADP1051.

DOWNLOADING THE GUI

The ADP1050-51 GUI setup file is included on the CD in the ADP1050 evaluation kit.

Users can also visit http://www.analog.com/ADP1050 to obtain the latest version of the GUI software.

INSTALLING THE GUI

Warning

Do not connect the USB cable to the evaluation board until the software has been installed.

Installation Steps

To install the ADP1050-51 GUI software, use the following steps:

1. Insert the CD.
2. Double-click the **ADP1050-51 Setup.msi** installation file to start the installation.
3. Follow the prompts in subsequent windows (see Figure 7) to install the software.
4. In the **Total Phase USB Setup** window, click **Next**.
5. Check **I accept the terms in the License Agreement** after reading it. Then click **Next**.
6. Check the **Install USB drivers** option when the driver is not installed. If the driver has been installed, clear the **Install USB drivers** option. Then click **Install**.
7. After the installation, click **Close** to complete the driver installation.
8. When the **Adobe Flash Player Installer** window appears, check **I have read and agree to the terms of the Flash Player License Agreement** after reading it. Then click **INSTALL**. If a newer version of Adobe Flash Player is already installed in the system, click **Quit**.
9. Click **Close** to exit the setup.

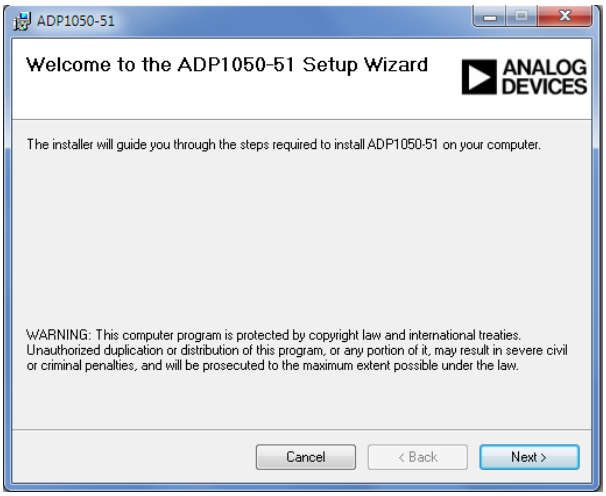


Figure 7. GUI Installation

LAUNCHING THE GUI

To launch the GUI, use the following steps:

1. Plug the ADP1050DC1-EVALZ daughter card into the J8 connector.
2. Ensure that the CTRL switch (SW1) is turned to the off position. The off position is the left side by default.
3. Plug the ADP-I2C-USB-Z connector into the USB port in the PC.
4. If the **Found New Hardware - Total Phase Aardvark I2C/SPI Host Adapter** message appears, the PC automatically installs the hardware driver. Wait until the installation is finished. If this window does not appear, skip this step.
5. Connect the ADP-I2C-USB-Z connector to J2 on the ADP1050DC1-EVALZ daughter card.
6. Double-click the **ADP1050-51.exe** file. The GUI software should report that the ADP1050 has been detected on the board, as shown in Figure 8.
7. Click **Finish** to proceed to the **Monitor** window (see Figure 10).
8. Click **Unlock the chip password** (Button I in Figure 10) and enter the chip password in the pop-up window that appears. The default chip password is 0xFFFF. Press ENTER after typing in the password to proceed to the **Setup** tab of the main window, as shown in Figure 11.

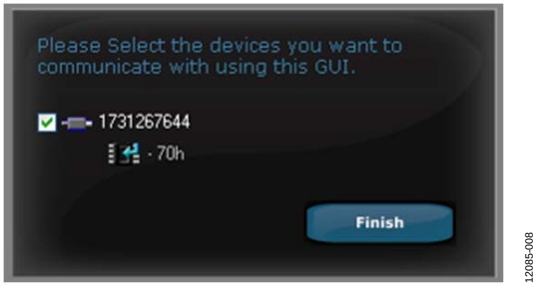


Figure 8. Getting Started—Device Detected on the Board

LOADING COMMAND AND BOARD SETTINGS

If the user wants to load the default command and board settings file from a local folder, click **Load Command and Board settings from a .50s file to the ADP1050 device** (Button A in Figure 11) and select the **ADP1050-240-EVALZ-Default.50s** file when specifying the folder, as shown in Figure 9. Because the ADP1050 in the evaluation kit is preprogrammed with the board and command settings, this step is optional.

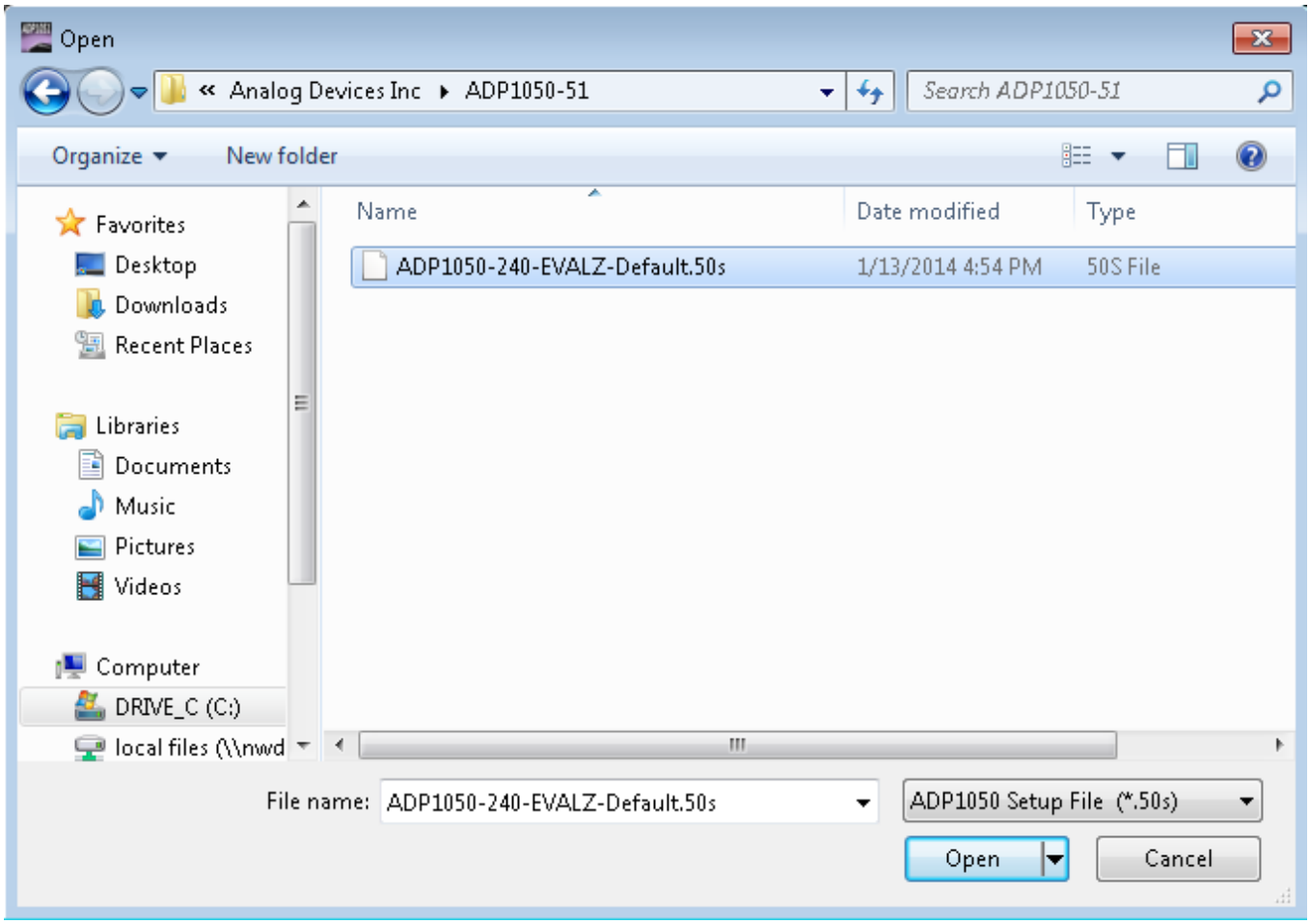


Figure 9. Load Board and Command Settings File

Table 6 shows a list of key buttons in the GUI.

Table 6. Key Buttons in the GUI

Button Letter	Button	Description
A		Load command and board settings from a .50s file to the ADP1050 device.
B		Save command and board settings from the ADP1050 device to a .50s file.
C	HEX	Generate a hexadecimal file of the command and board settings.
D	EPM	Access the EEPROM.
E		Scan for the ADP1050 device.
F		Open a spy window to monitor PMBus communication between the GUI and the ADP1050 device.
G		Program command and board settings into the EEPROM.
H		Unlock/lock the trim password.
I		Unlock/lock the chip password.

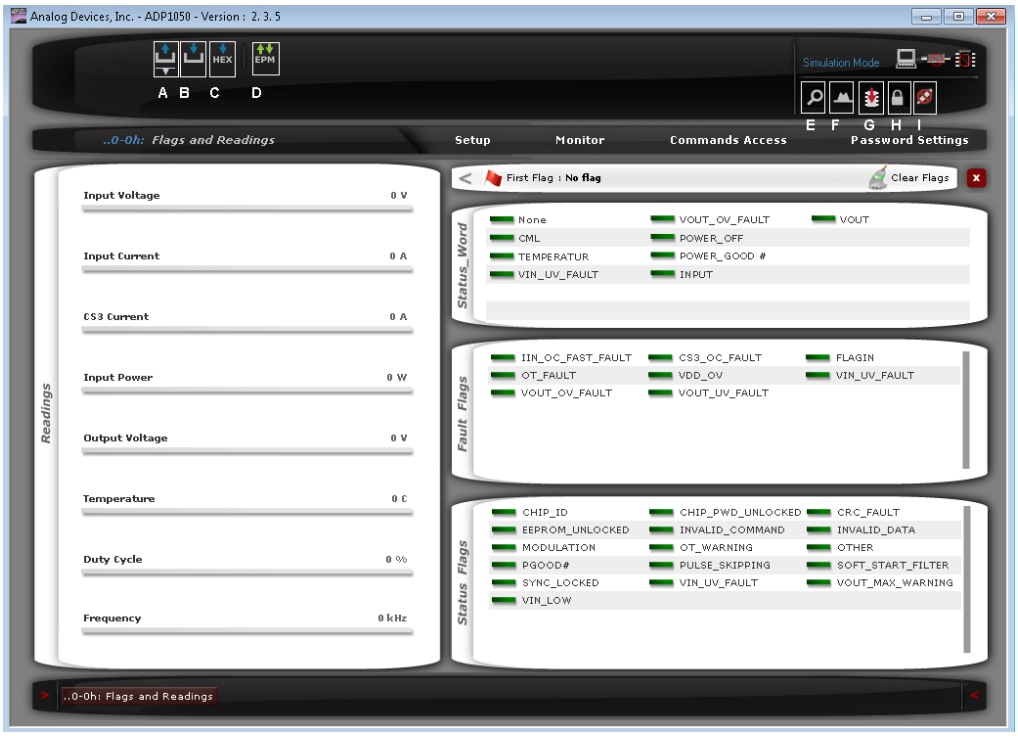


Figure 10. Monitor Window in the GUI

GETTING STARTED

1. Connect a dc source (voltage range of 36 V dc to 75 V dc) at the J1 and J5 input terminals, and connect an electronic load at the J2 and J6 output terminals. See Figure 6 for the correct configuration.
2. Connect the multimeters on the input terminals and output terminals separately as shown in Figure 6.
3. Connect the voltage probes at different test points. Ensure that differential probes are used and that the grounds of the probes are isolated if the measurements are performed simultaneously on the primary and secondary sides of the transformer.
4. Turn the CTRL switch (SW1) to the on position.

The evaluation board is now up and running, and ready for evaluation. The output should read 12 V dc.

After a successful startup, the PSU is in a steady state. The LEDs of the board provide the status of the board. When D17 is turned on, there are no faults detected. When a fault is detected, the PGOOD LED is turned off, indicating that a flag has been triggered. The **Monitor** tab of the main window in the GUI displays the appropriate state of the PSU.

After completing the programming of the ADP1050, click **Program command and board settings into the EEPROM** (Button G in Figure 11) to program the command and board settings into the EEPROM if the user wants to save the settings in the device. Moreover, the user can use the **Save command and board settings from the ADP1050 device to a .50s file** button (Button B in Figure 11) to generate a .50s file for the command and board settings.

Software Main Window

Figure 11 shows the main window. There are four tabs in the main window:

- **Setup** tab: All the setting controls, including board and command settings, can be accessed via this tab.
- **Monitor** tab: The readings and flags are monitored in this tab.
- **Commands Access** tab: This tab provides the command maps for direct access.
- **Password Settings** tab: The PMBus command WRITE_PROTECT and chip password can be configured in this tab.

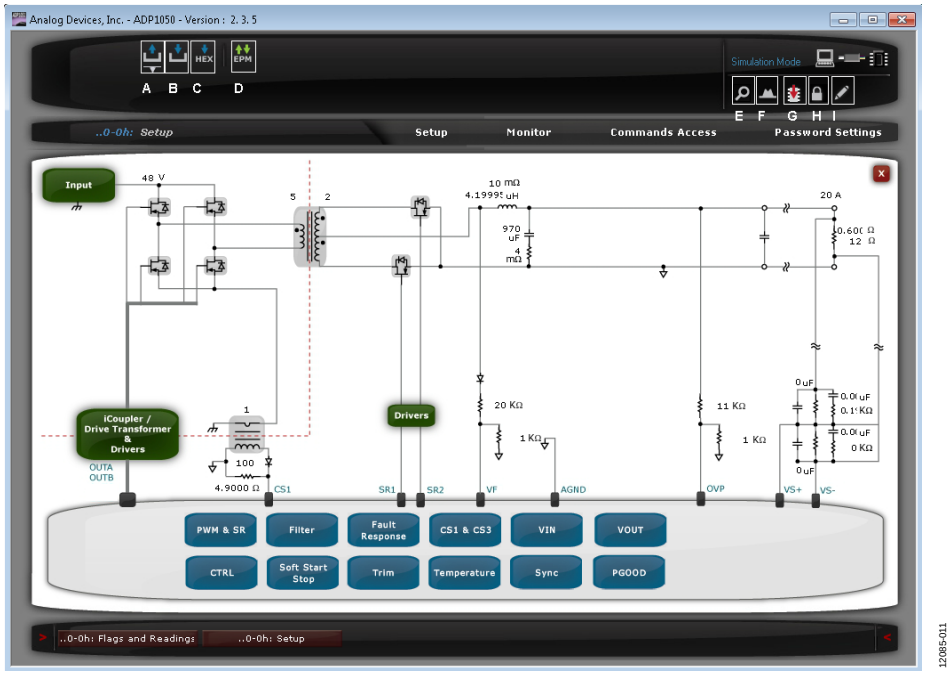


Figure 11. Main Setup Window of the GUI (See Table 6)

EVALUATING THE BOARD

This ADP1050 evaluation kit allows the user to gain insight into the flexibility offered by the extensive ADP1050 programming options. The following sections provide an overview of the options that are available to evaluate the key features of the ADP1050.

ON/OFF CONTROL AND SOFT START

This section specifies the power-on control behavior, the power-off control behavior, and the soft start timing of the PSU. By default, the AND logic of the hardware CTRL pin logic and the software OPERATION command are used to turn on the ADP1050, as shown in the **CTRL Settings** window (see Figure 12), accessed via the **Setup** tab. It is recommended that Switch SW1 be used to control the operation state of the PSU.

The turn-on delay time, turn-on rise time, and turn-off delay time can be programmed in the **Soft Start and Stop Settings** window (see Figure 13), accessed via the **Setup** tab. The **Additional Soft Start Settings** window is shown in Figure 14.

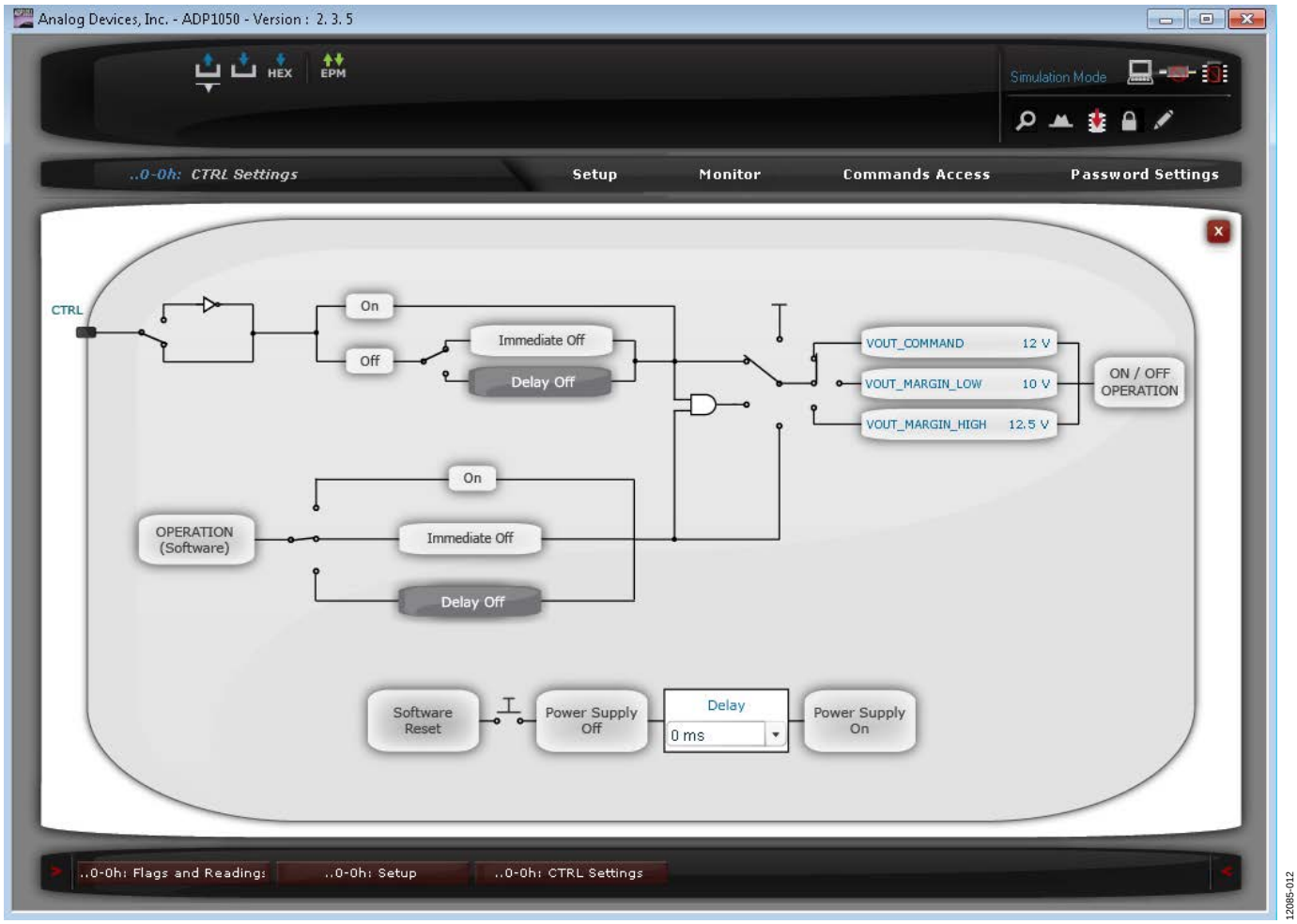


Figure 12. CTRL Settings Window

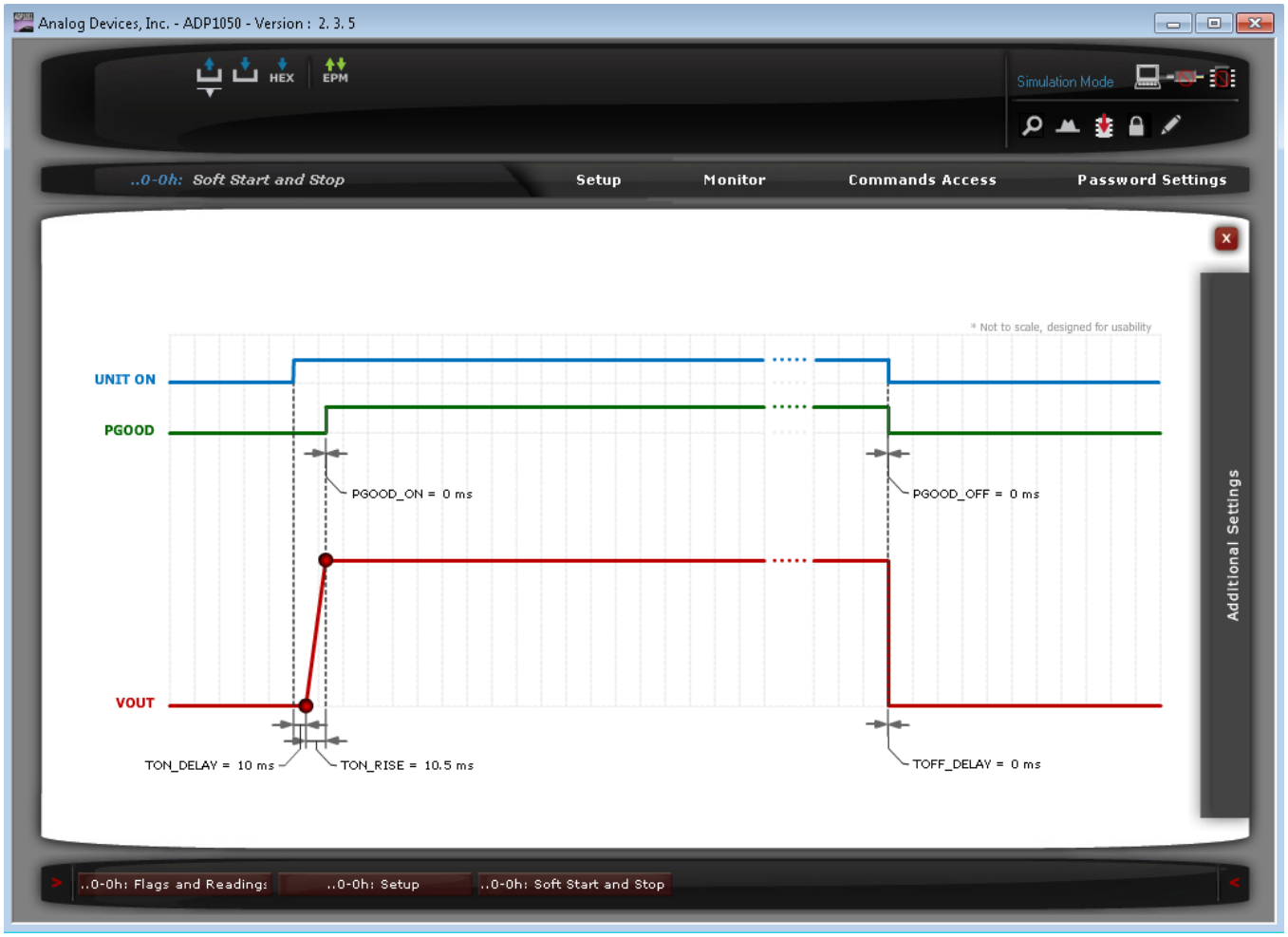


Figure 13. Soft Start and Stop Settings Window

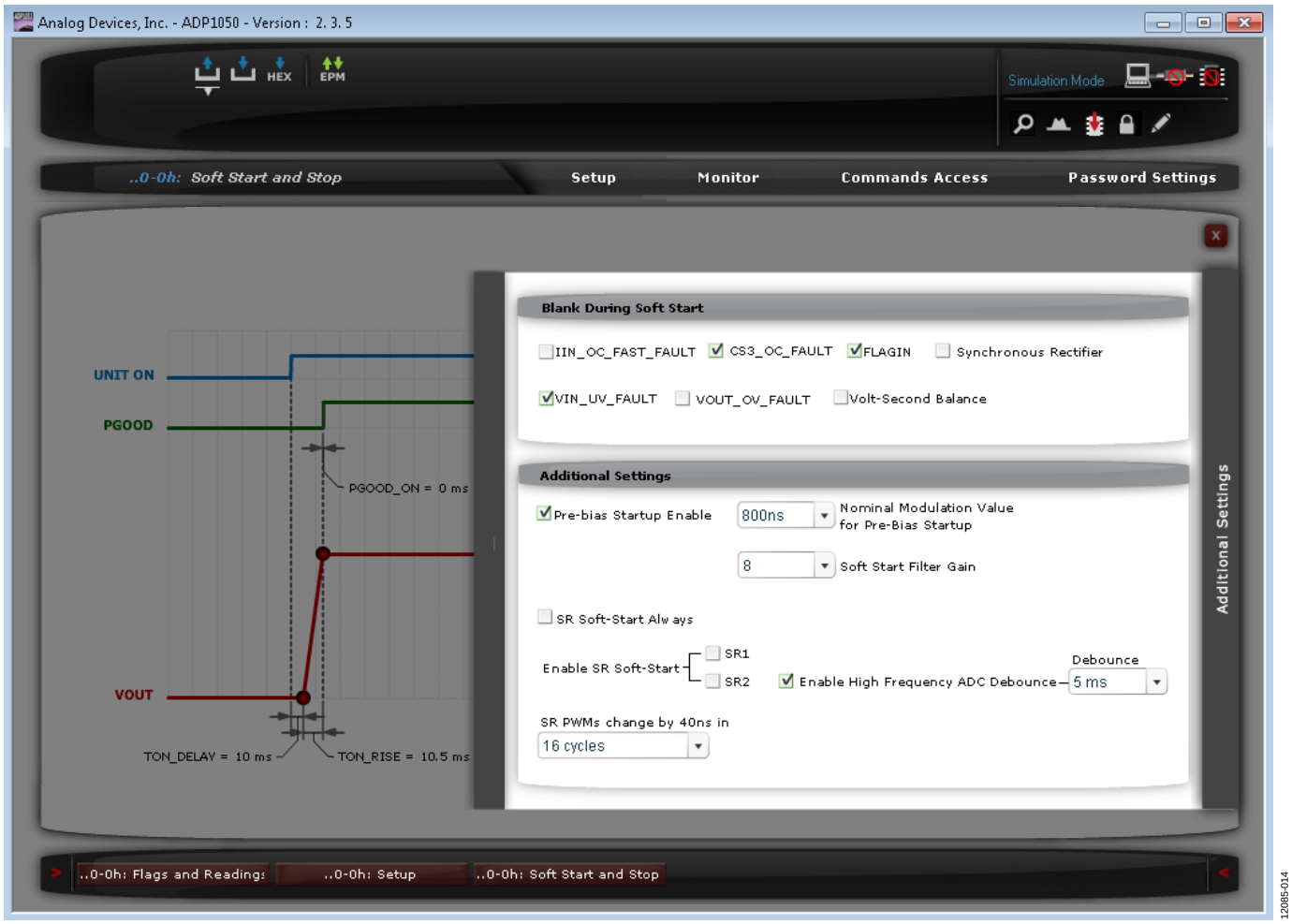


Figure 14. Additional Soft Start Settings Window

Figure 15 and Figure 16 show the results of a soft start at 0 A load and 20 A load, respectively. The soft start rise time is programmed to 10 ms. Figure 17 shows an example of a soft start with disabled synchronous rectifiers during the soft start ramp.

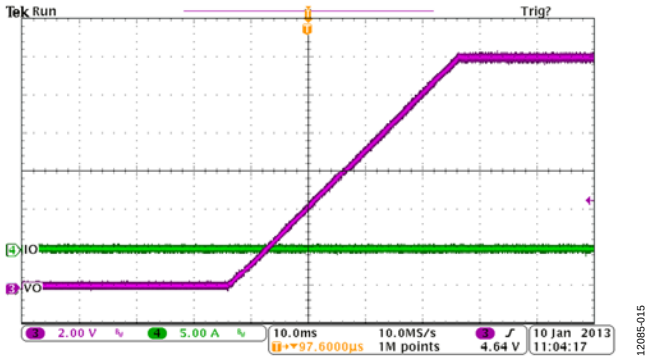


Figure 15. Soft Start at 48 V DC Input, 0 A Load

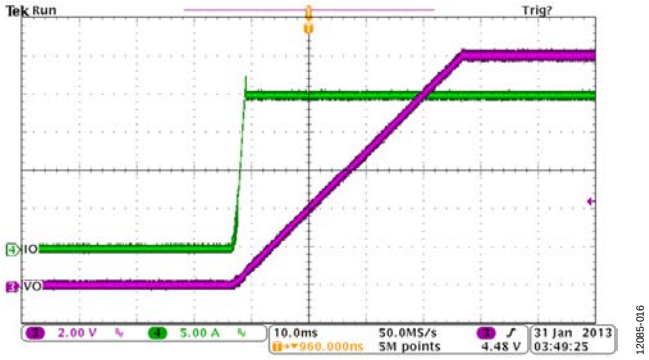


Figure 16. Soft Start at 48 V DC Input, 20 A Load

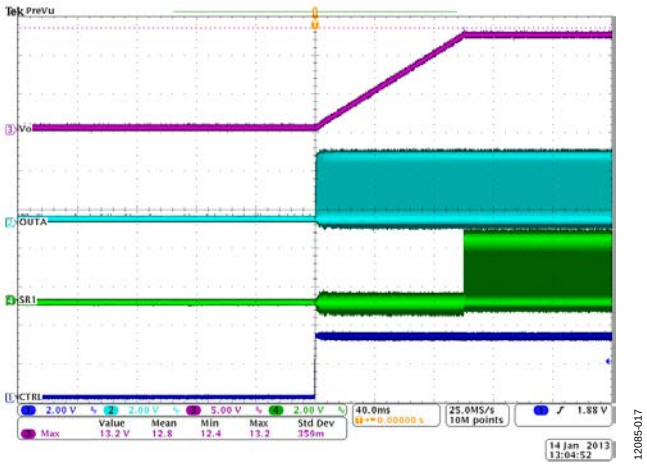


Figure 17. Soft Start with Disabled Synchronous Rectifiers

Prebias Start-Up Function

The prebias start-up function provides the capability to start up with a prebiased voltage on the output. To set up the prebias start-up function, use the following steps:

1. In the **Additional Soft Start Settings** window (see Figure 14), enable the prebias start-up function and program the appropriate nominal modulation value for prebias startup.
2. Select the type of prebias startup in the **Feedforward Selection** window (see Figure 18):
   - If the closed-loop input voltage feedforward operation is enabled and the input voltage information is available for the ADP1050 before the PSU starts up, select the **Feed Forward always Activated** option (Option A in Figure 18).
   - If the closed-loop input voltage feedforward operation is disabled and the input voltage information is available for the ADP1050 before the PSU starts up, select the **Feed Forward only during Startup** option (Option B in Figure 18).
   - If the closed-loop input voltage feedforward operation is disabled and the input voltage information is not available for the ADP1050 before the PSU starts up, select the **Feed Forward always Disabled** option (Option C in Figure 18).

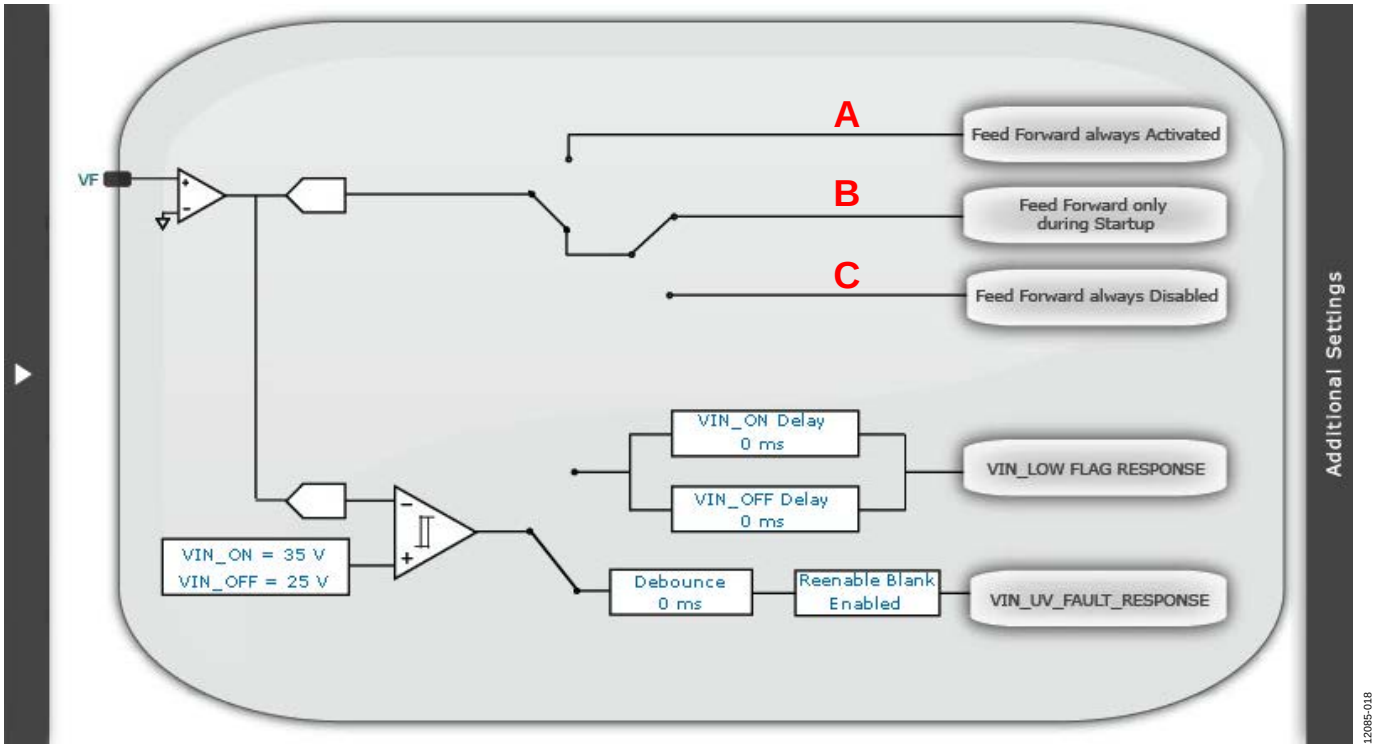


Figure 18. Feedforward Selection Window

Figure 19 and Figure 20 show the prebias start-up waveforms when the **Feed Forward always Activated** option (Option A in Figure 18) is selected.

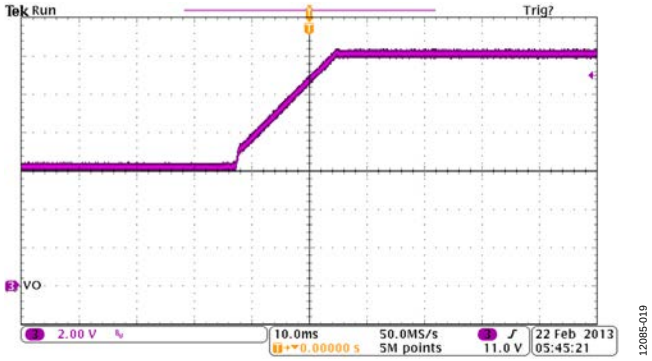


Figure 19. Prebias Startup at 36 V DC Input and Low Residual Voltage

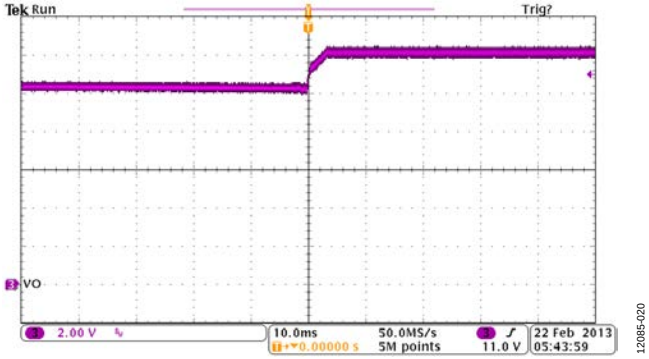


Figure 20. Prebias Startup at 60 V DC Input and High Residual Voltage

Because the input voltage cannot be sensed through the transformer windings of the auxiliary power circuit in this evaluation board, it is recommended that the **Feed Forward always Disabled** option (Option C in Figure 18) be selected for evaluation.

Other evaluation options include the following:

- Program a different turn-on rise time in combination with a different turn-on delay time (see Figure 13).
- Select different flags to blank during the soft start ramp (see Figure 14).
- Choose different soft start gains to optimize the soft start ramp (see Figure 14).
- Enable the synchronous rectifier soft start and select a different synchronous rectifier soft start speed (see Figure 14) to prevent a glitch at the output voltage ramp.

PWM SETTINGS

The PWM timings for the primary side switches and the secondary side synchronous rectifiers are programmed in the **PWM SR Settings** window (see Figure 21), accessed via the **Setup** tab. This window allows the programming of the switching frequency, the rising edge and falling edge timings, the type of modulating edge (rising edge or falling edge), the modulation type (positive or negative), and the modulation limit. Figure 21 shows the gate drive signals at the output pins of the ADP1050. The QA/QD, QB/QC, Q7/Q8, and Q3/Q4 switches on the ADP1051-240-EVALZ evaluation board are driven separately by PWM outputs OUTA, OUTB, SR1, and SR2.

Although the switching frequency can be adjusted, the GUI software does not account for the dead times. The PWM timings must be programmed manually to guarantee normal operation of the PWM outputs.

Additional PWM and synchronous rectifier evaluation options include the following:

- Enable and disable the pulse skipping mode and measure the standby power of the PSU.
- Double the switching frequency from 120 kHz to 240 kHz. The board is designed to operate at a switching frequency of up to 240 kHz with airflow cooling.
- Program an imbalance in the on time of the QA and QB switches, and evaluate the volt-second balance control function.
- Run the software in simulation mode and program the PWM settings for different topologies, such as hard-switched full bridge, half bridge, push-pull, two-switch forward, or active clamp forward converters.
- Align all synchronous rectifier edges to the OUTA and OUTB edges and adjust the primary-secondary propagation delay by programming the SR1 and SR2 delay.

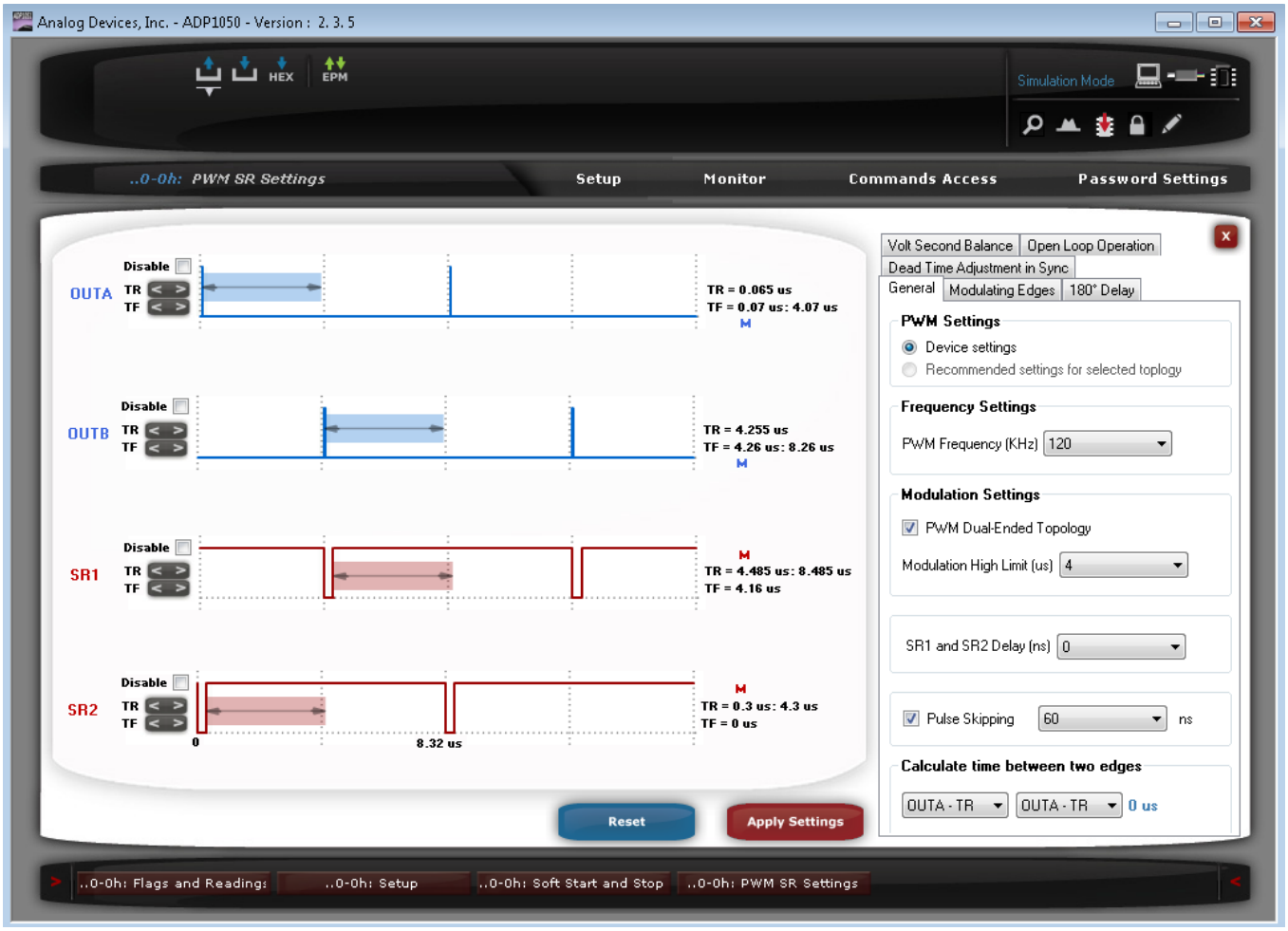


Figure 21. PWM SR Settings Window

DIGITAL COMPENSATOR AND LOAD TRANSIENT RESPONSE

The digital compensator can be configured by the **Filter Settings** window (see Figure 22), accessed via the **Setup** tab. The digital compensator can be changed by manipulating the position of the poles and zeros in the s-domain.

The digital compensator is a Type III compensator. The first pole is placed at a dc position to eliminate the steady state error. The second pole can be placed anywhere, but ideally should be placed at the ESR zero position. The third pole is fixed at half the switching frequency.

Warning

Although varying the parameters of the compensator is possible when the part is running, the wrong combination of parameters may cause the system to become unstable.

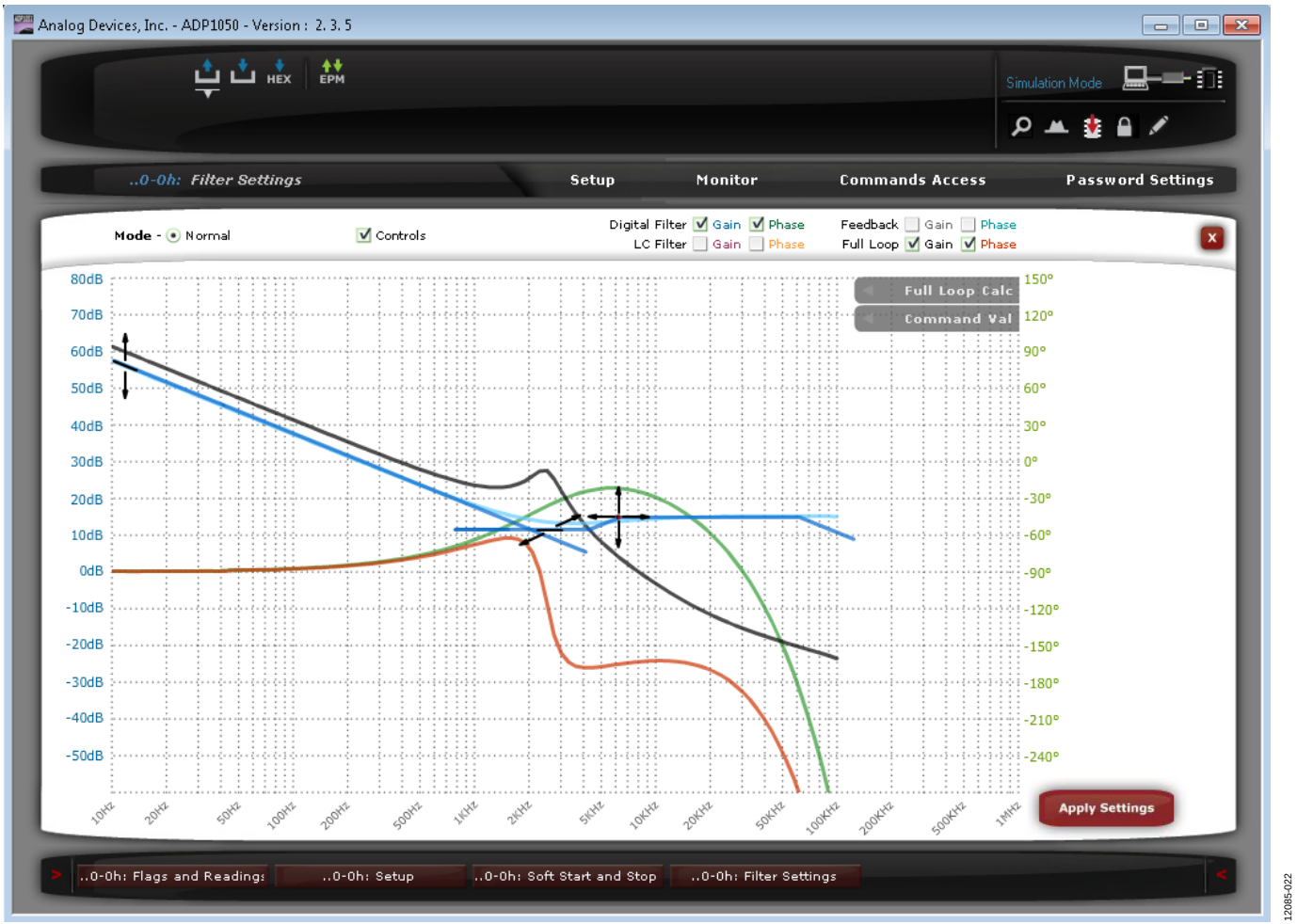


Figure 22. Filter Settings Window

Control Loop Configuration

To configure the control loop, use the following steps:

1. Make sure the board parameters are set correctly, including the topology, the turn ratio of the main transformer, the output LC filter parameters, and the output voltage sense network parameters. Using this information, the GUI software generates the bode plots of the power stage and the output voltage sense network separately.
2. The switching frequency is determined in the **PWM SR Settings** window. Changing the switching frequency changes the low frequency gain and the third pole position.
3. The user can start to place the zeros and poles and can set the low frequency gain and high frequency gain of the digital compensator, based on the stability rules.
4. The GUI then displays the full loop gain crossover frequency, the phase margin, the gain margin, and the phase crossover frequency.
5. Using a loop analyzer, such as an AP300, the user can verify the programmed control loop (an example is shown in Figure 23). During the control loop test, the test signal from the loop analyzer can be easily injected in JP1 of the evaluation board.

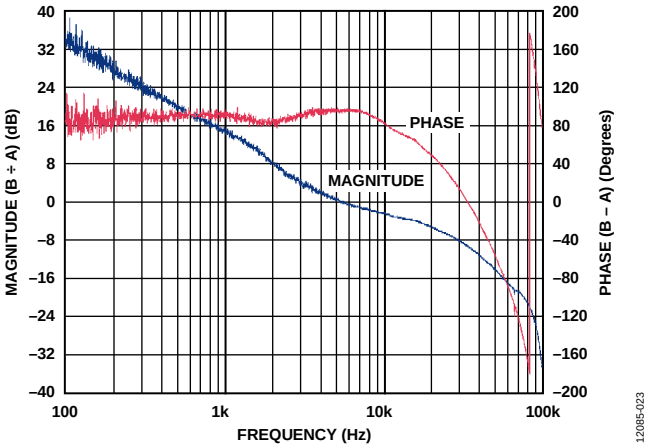


Figure 23. Control Loop Test Using an AP300 Loop Analyzer

Transient Response for the Load Step

A dynamic electronic load can be connected to the output of the evaluation board to evaluate the load transient response. Set up an oscilloscope to capture the transient waveforms of the PSU output. Figure 24 and Figure 25 show examples of load transient responses.

The user can vary the digital compensator via the GUI software to change the transient response. This evaluation kit allows the digital compensator to be easily programmed to optimize the load transient response of the PSU.

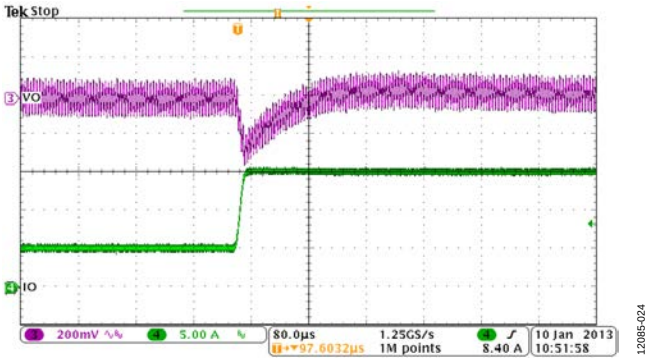


Figure 24. Transient Response with Load Steps: 25% to 50% to 25%

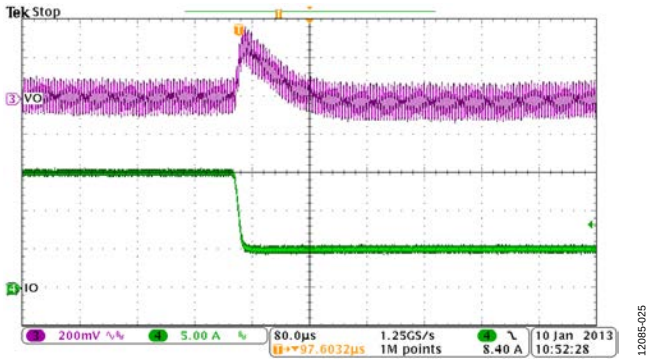


Figure 25. Transient Response with Load Steps: 50% to 75% to 50%

INPUT VOLTAGE SETTINGS

If the input voltage can be sensed by ADP1050 before the PSU is turned on (for example, the input voltage is sensed through the transformer windings of the auxiliary power circuit), the V_{IN} on and V_{IN} off limits can be programmed to control the input UVLO protection. Using the **VIN Settings** window (see Figure 26), accessed via the **Setup** tab, the user can program the V_{IN} on and V_{IN} off limits.

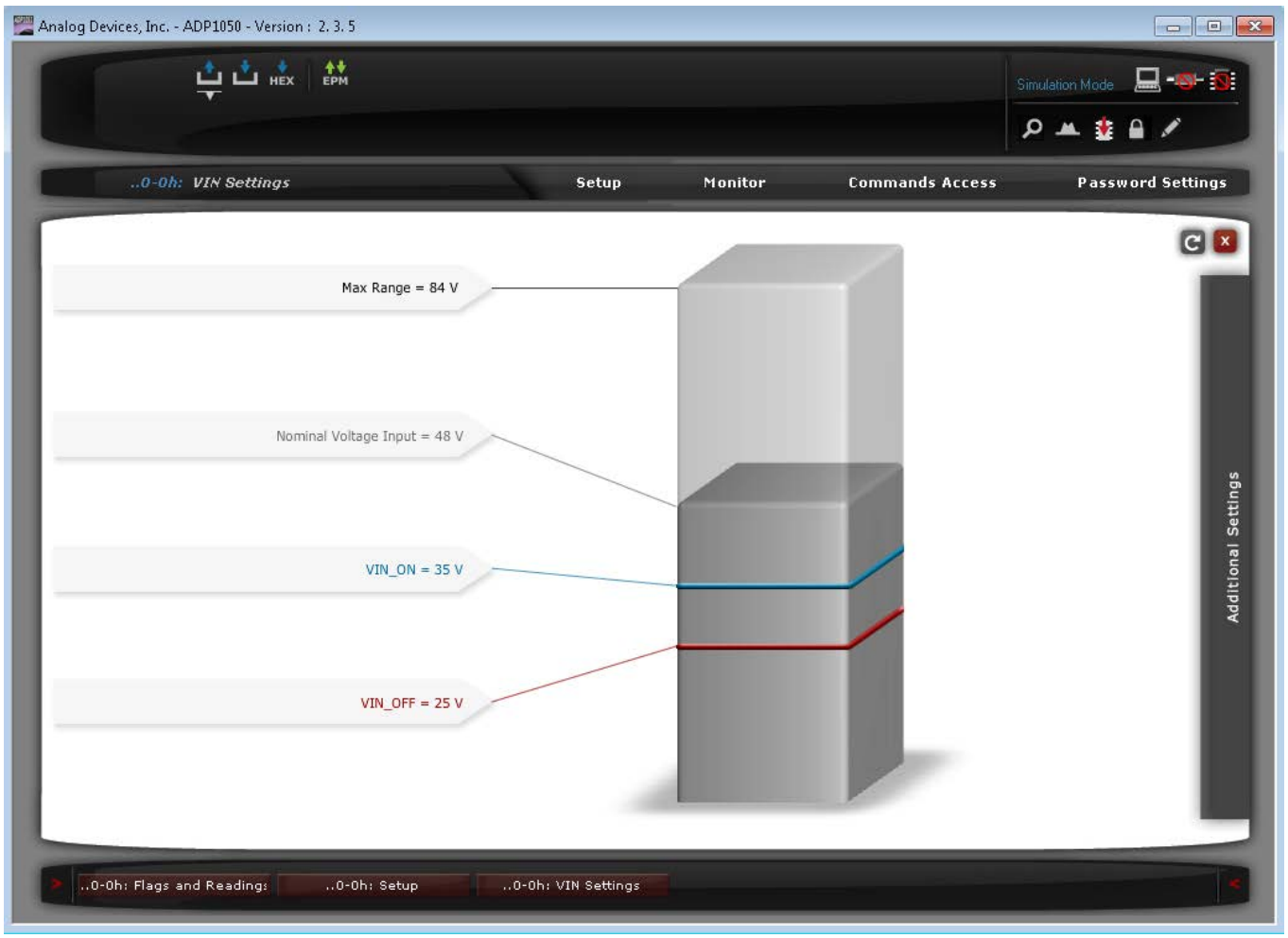


Figure 26. VIN Settings Window

By selecting different input voltage feedforward options (labeled A, B, and C in Figure 18) in the **Feedforward Selection** window, the input voltage feedforward can be evaluated in different ways. Figure 27 shows an input voltage transient response when the feedforward is disabled (Option C—**Feed Forward always Disabled** in Figure 18). Figure 28 shows an input voltage transient response when the feedforward is enabled (Option A—**Feed Forward always Activated** in Figure 18).

Additional input voltage related evaluation options include the following:

- Apply a different input voltage compensation multiplier (Register 0xFE59) to attain an accurate input voltage sense at both no load and heavy load conditions.
- Select the input voltage signal to trigger the VIN_LOW flag or the VIN_UV_FAULT flag in the **Feedforward Selection** window (see Figure 18).

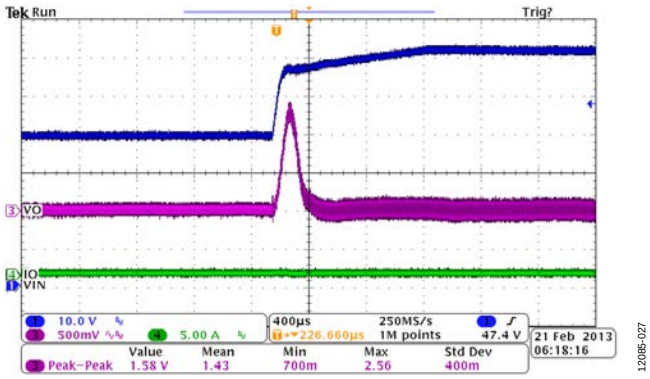


Figure 27. Input Voltage Transient Response with Feedforward Disabled

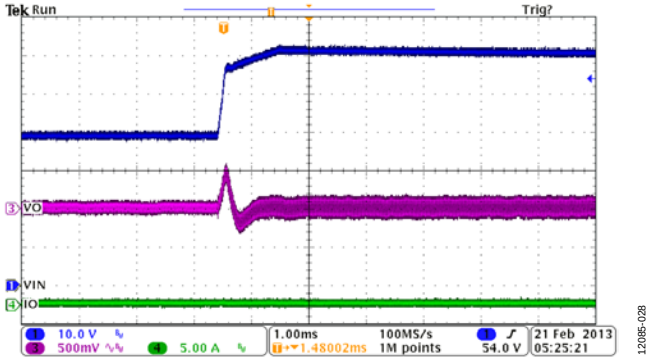


Figure 28. Input Voltage Transient Response with Feedforward Enabled

OUTPUT VOLTAGE SETTINGS

The **VOUT Settings** windows (shown in Figure 29 and Figure 30) set all the output voltage related parameters, such as the output voltage settings, the output voltage transition rate (through the VOUT_TRANSITION_RATE command), and the conditional overvoltage protection setting. The window shown in Figure 29 can be accessed by clicking **VOUT** in the **Settings** tab of the main window, and the window shown in Figure 30 can be accessed by clicking **Additional Settings** in **VOUT Settings Window 1**.

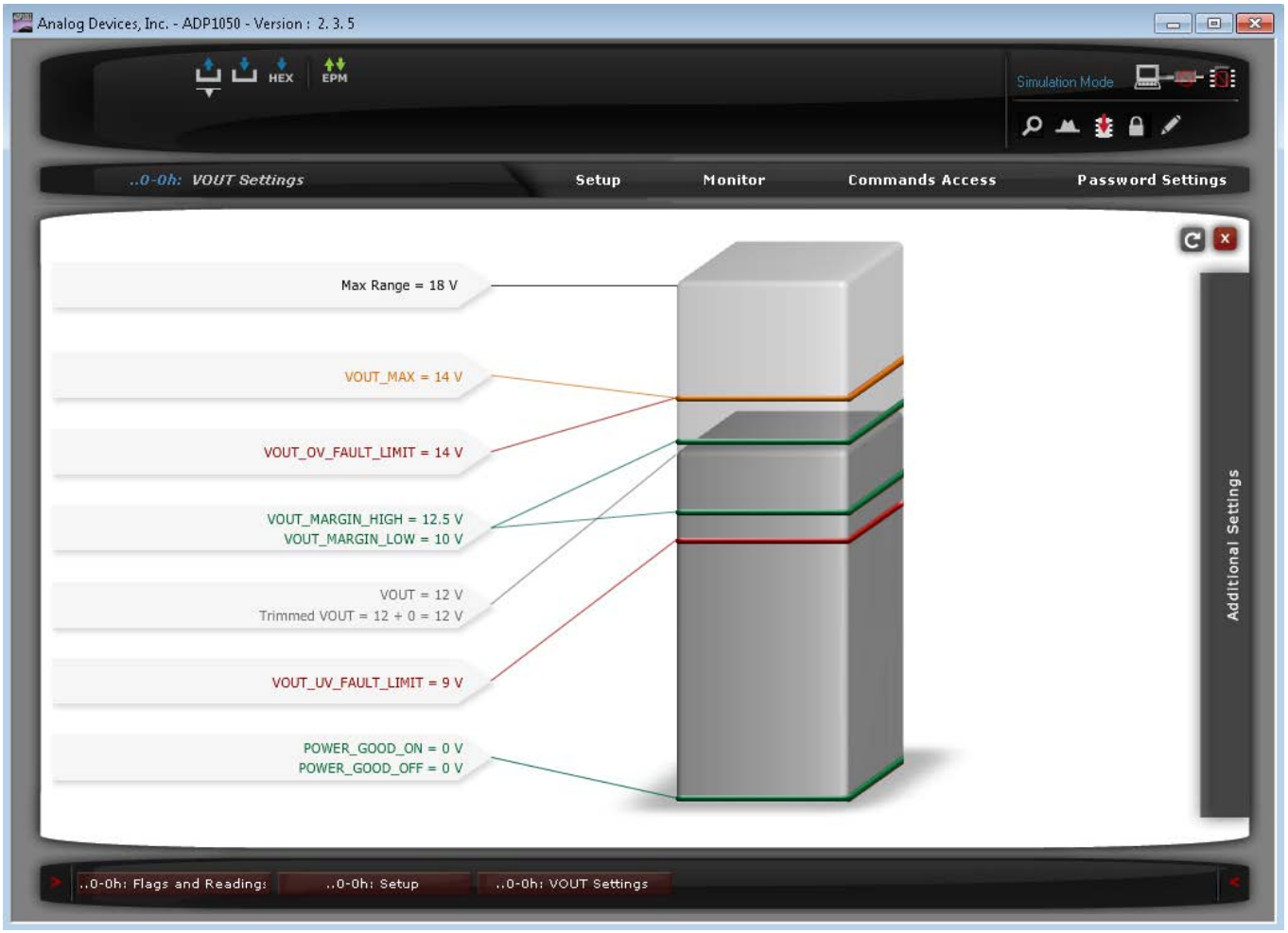


Figure 29. VOUT Settings Window 1

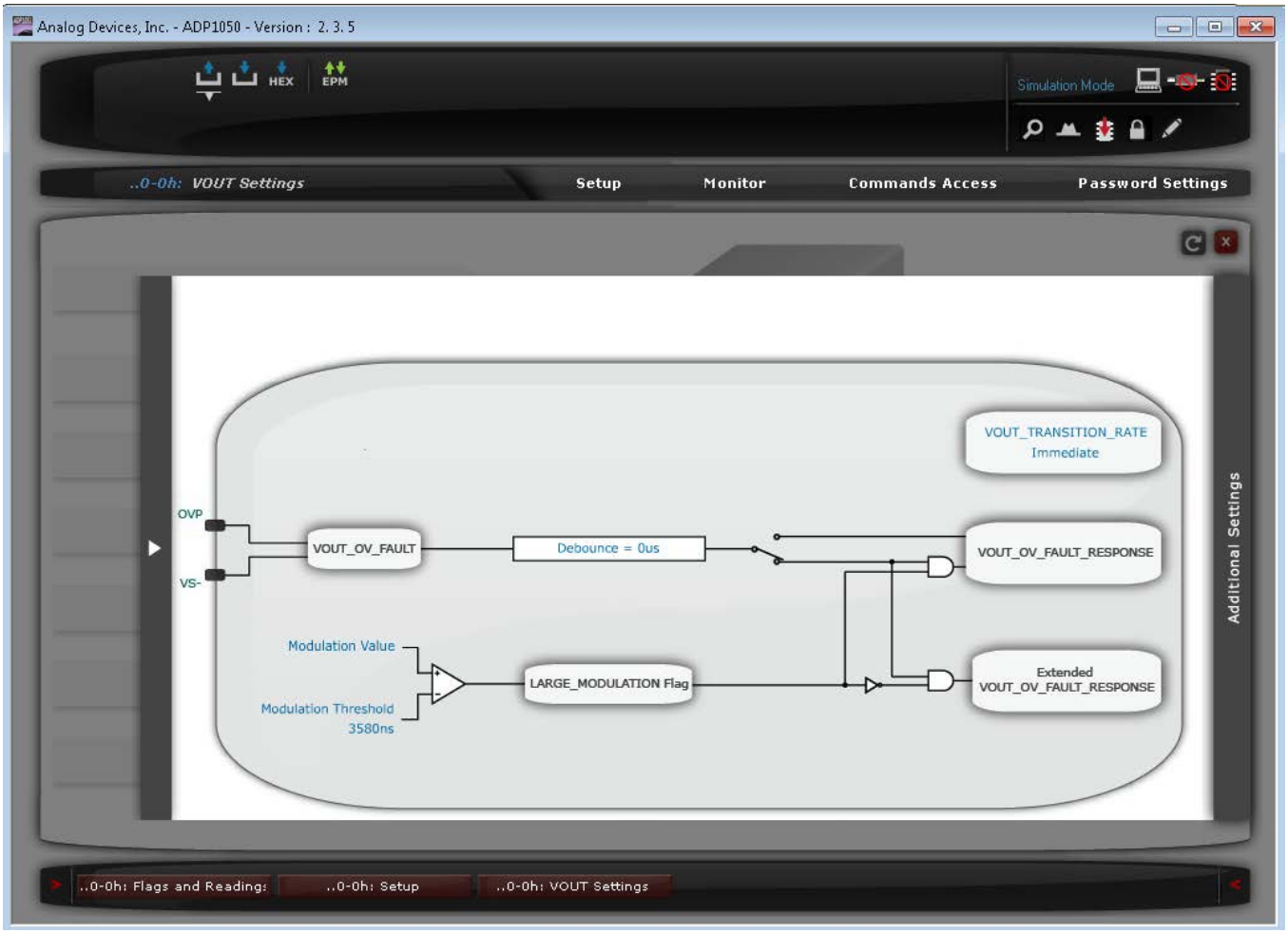


Figure 30. VOUT Settings Window 2

Figure 31 and Figure 32 show the results of adjusting the output voltage when the V_{OUT} transition rate is programmed as 3.125 µV/µs.

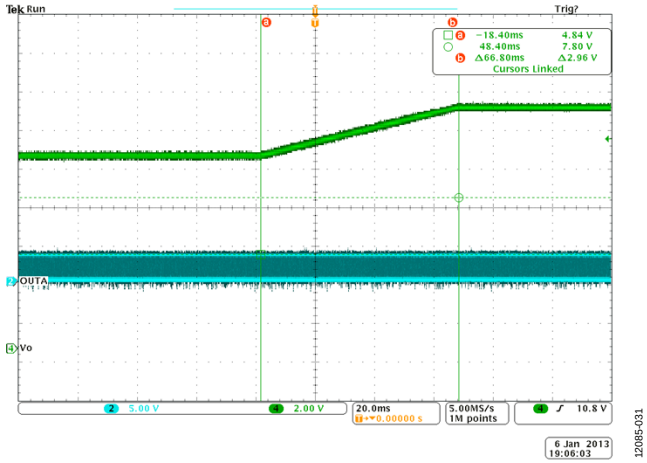


Figure 31. V_{OUT} Adjusted from 10 V to 12.5 V with 3.125 µV/µs Transition Rate

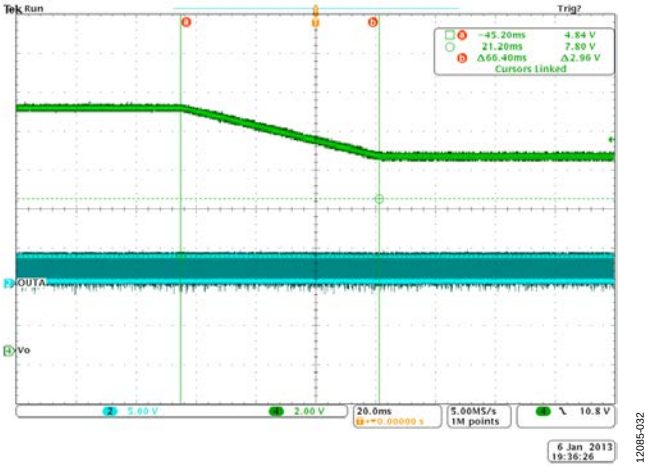


Figure 32. V_{OUT} Adjusted from 12.5 V to 10 V with 3.125 µV/µs Transition Rate

Output Overvoltage Protection

This test can be conducted in several ways. The simplest way is to set the output voltage to a value higher than the V_{OUT} overvoltage fault limit (see **VOUT_OV_FAULT_LIMIT** in Figure 29). Alternatively, the user can short the VS+ pin to AGND in the ADP1050DC1-EVALZ daughter card to cause a fast output overvoltage condition. The responses of the fault conditions can be programmed in the **Fault Response** window (see the Flags and Fault Response Configurations section and Figure 37). Figure 33 shows an example of waveforms in response to an output overvoltage condition.

The ADP1050 also supports conditional output overvoltage protection. The settings of conditional output overvoltage protection can be accessed via **VOUT Settings Window 2** (see Figure 30). Figure 34 shows a result of conditional overvoltage protection when the outputs of two evaluation boards are connected to a common bus.

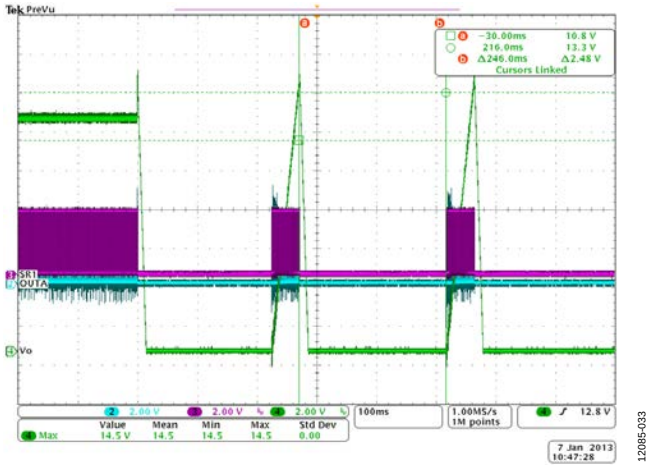


Figure 33. Overvoltage Protection Waveforms

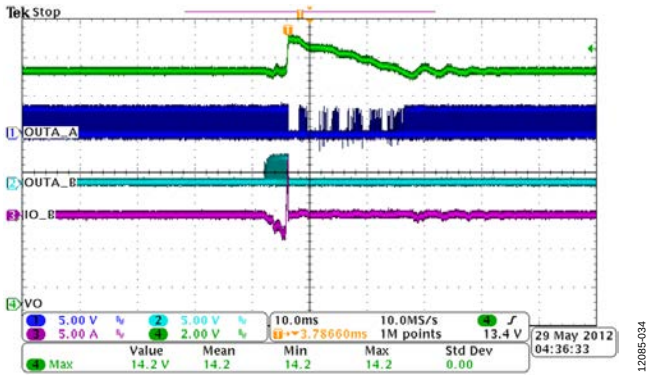


Figure 34. Conditional Overvoltage Protection with Two Evaluation Boards Connected to a Common Bus

Output Undervoltage Protection

This test can be done in several ways. The simplest way is to set the output voltage to a value lower than the V_{OUT} undervoltage fault limit value (see **VOUT_UV_FAULT_LIMIT** in Figure 29). Even a shorted load or an internal short (such as shorting of the synchronous rectifiers) can cause an output undervoltage condition. The response of the fault condition can be programmed in the **Fault Response** window (see the Flags and Fault Response Configurations section and Figure 37).

INPUT AND OUTPUT CURRENT SETTINGS

The input and output current settings are accessed using the **CS1 and CS3 Settings** window (see Figure 35), accessed via the **Setup** tab. This window is used to program the CS1 cycle-by-cycle current limiting, the input overcurrent fast fault protection, the CS3 output overcurrent protection, and the volt-second balance control.

CS1 Cycle-by-Cycle Current Limiting

The leading edge blanking time, the leading edge blanking reference, the debounce time, the PWM disabling selection, and the matched cycle-by-cycle current limiting can be programmed in the **CS1 and CS3 Settings** window (see Figure 35).

Input Overcurrent Fast Fault Protection (CS1 Overcurrent Protection)

This test can be conducted by shorting the load. Using the **CS1 and CS3 Settings** window (see Figure 35), the user can specify the I_{IN} overcurrent fast fault limit value to 2, 8, 16, 64, 128, 256, 512, or 1024. The fault response can be configured in the **Fault Response** window (see the Flags and Fault Response Configurations section and Figure 37).

Output Overcurrent Fast Fault Protection (CS3 Overcurrent Protection)

This test can be conducted by applying an overload. Using the **CS1 and CS3 Settings** window (see Figure 35), the user can specify the CS3 overcurrent fast fault limit value. The fault response can be configured by clicking **CS3_OC_FAULT** in the **Fault Response** window (see the Flags and Fault Response Configurations section and Figure 37).

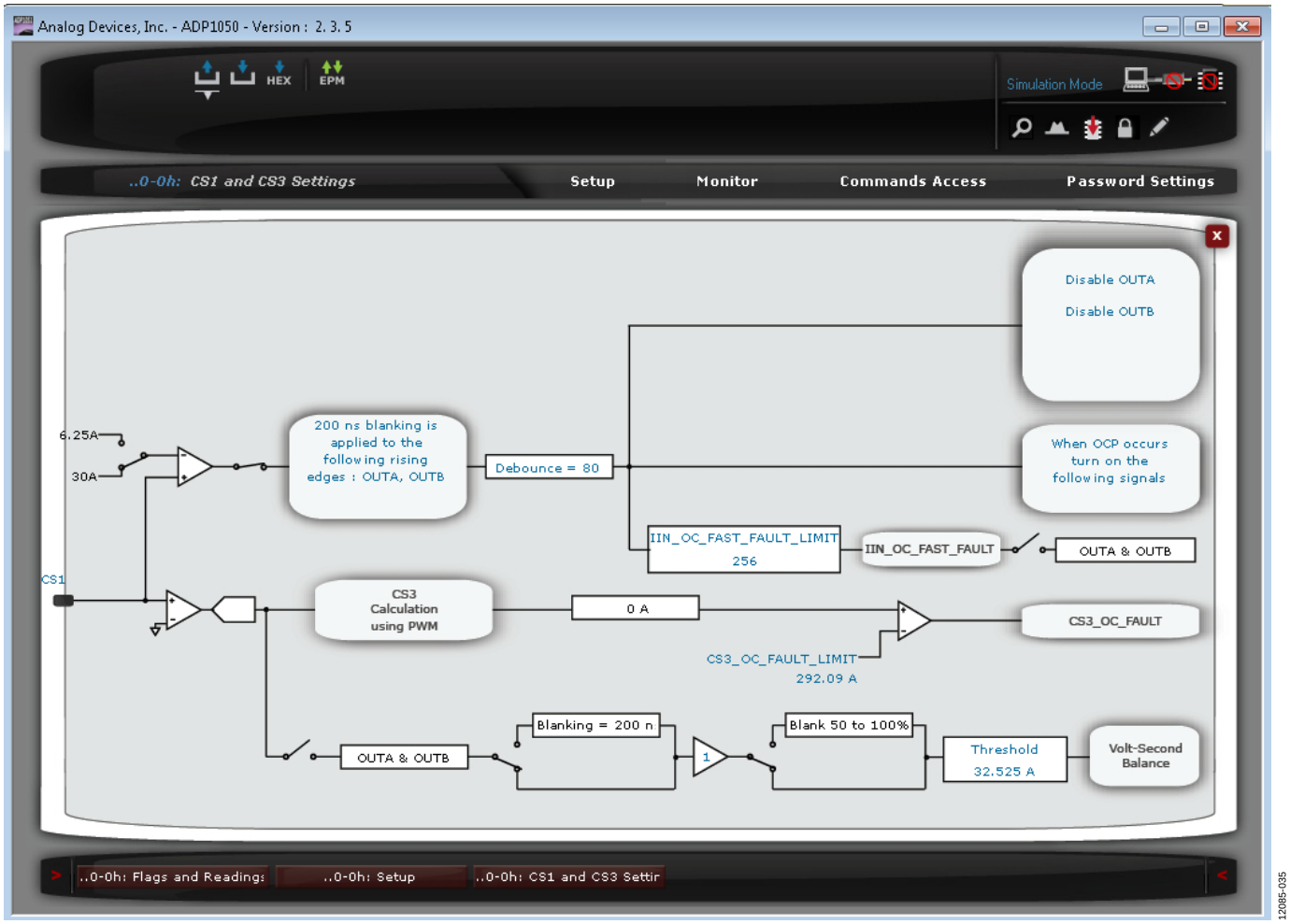


Figure 35. CS1 and CS3 Settings Window

TEMPERATURE SETTINGS

This test can be conducted by enclosing the evaluation board in a thermal chamber at the desired ambient temperature to simulate the operating condition. The user can program the overtemperature fault limit and overtemperature warning limit through the **Temperature Settings** window (see Figure 36). The overtemperature hysteresis is the difference between the values of the overtemperature fault limit and the overtemperature warning limit.

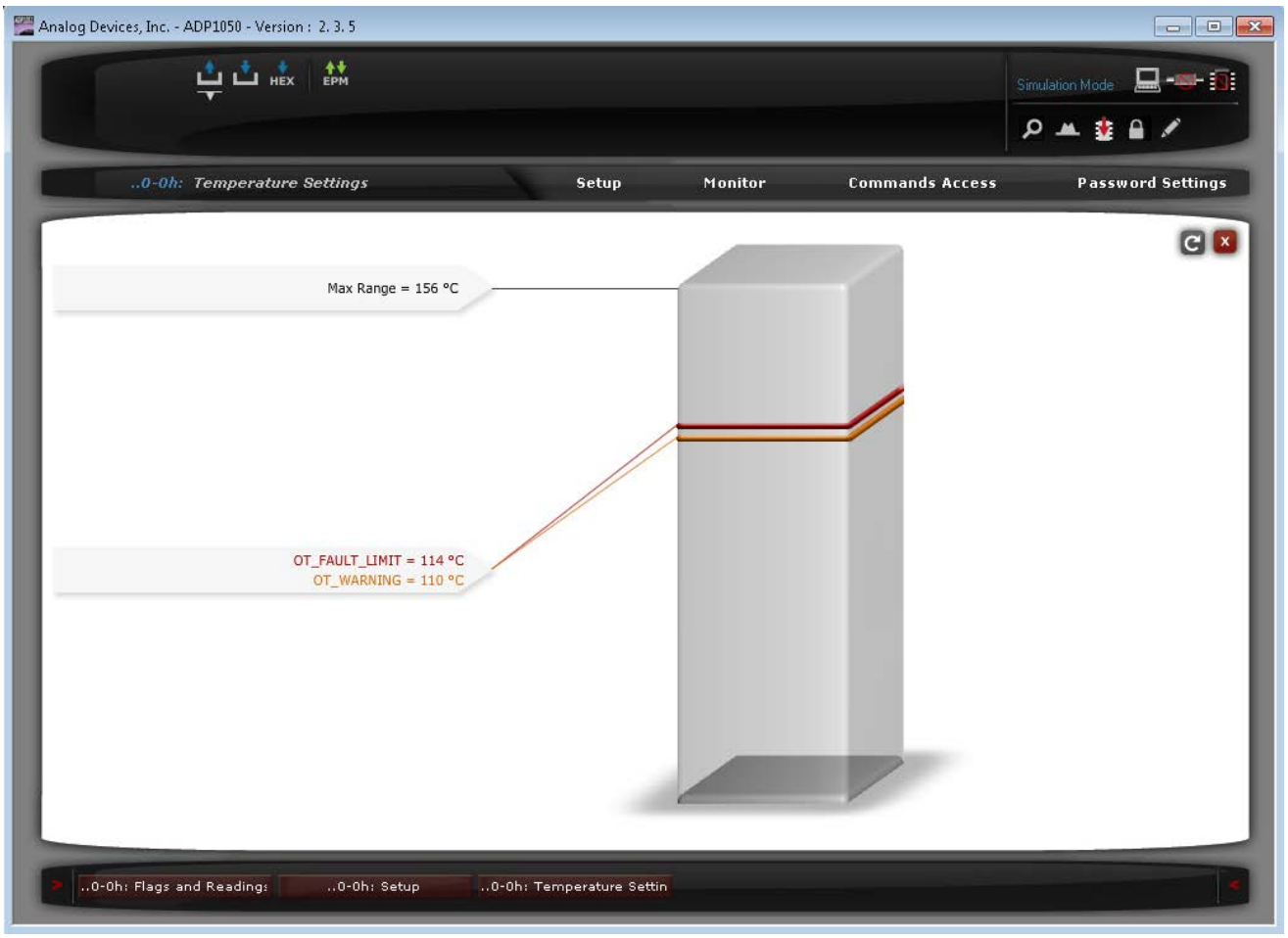


Figure 36. Temperature Settings Window

FLAGS AND FAULT RESPONSE CONFIGURATIONS

The fault responses can be programmed in the **Fault Response** window (see Figure 37), accessed via **Setup** tab. The state of each fault can be monitored in the **Monitor** tab, as shown in Figure 10. There are two groups of fault responses:

- PMBus fault responses, including the V_{OUT} overvoltage fault response (VOUT_OV_FAULT_RESPONSE), the V_{OUT} undervoltage fault response (VOUT_UV_FAULT_RESPONSE), and the overtemperature fault response (OT_FAULT_RESPONSE).
- Manufacturer specific fault responses, including the I_{IN} overcurrent fast fault response (IIN_OC_FAST_FAULT_RESPONSE), the CS3 overcurrent fault response (CS3_OC_FAULT_RESPONSE), the V_{IN} undervoltage fault response (VIN_UV_FAULT_RESPONSE), the flag input fault response (FLAGIN_RESPONSE), and the VDD overvoltage fault response (VDD_OV_RESPONSE). There is a global reenabling timing for all manufacturer specific fault responses.

The user can test these responses by applying a fault condition. By changing the settings of the debounce timing, delay timings, and responses and reenable timings, the user can alter the protection performance.

If there is a fault causing the power supply to be shut down and a soft start is required because the PWM outputs are reenabled, the first fault ID information is displayed in the **Monitor** tab. The first flag ID register provides the user with more information than a simple flag would and, therefore, helps facilitate fault diagnoses.

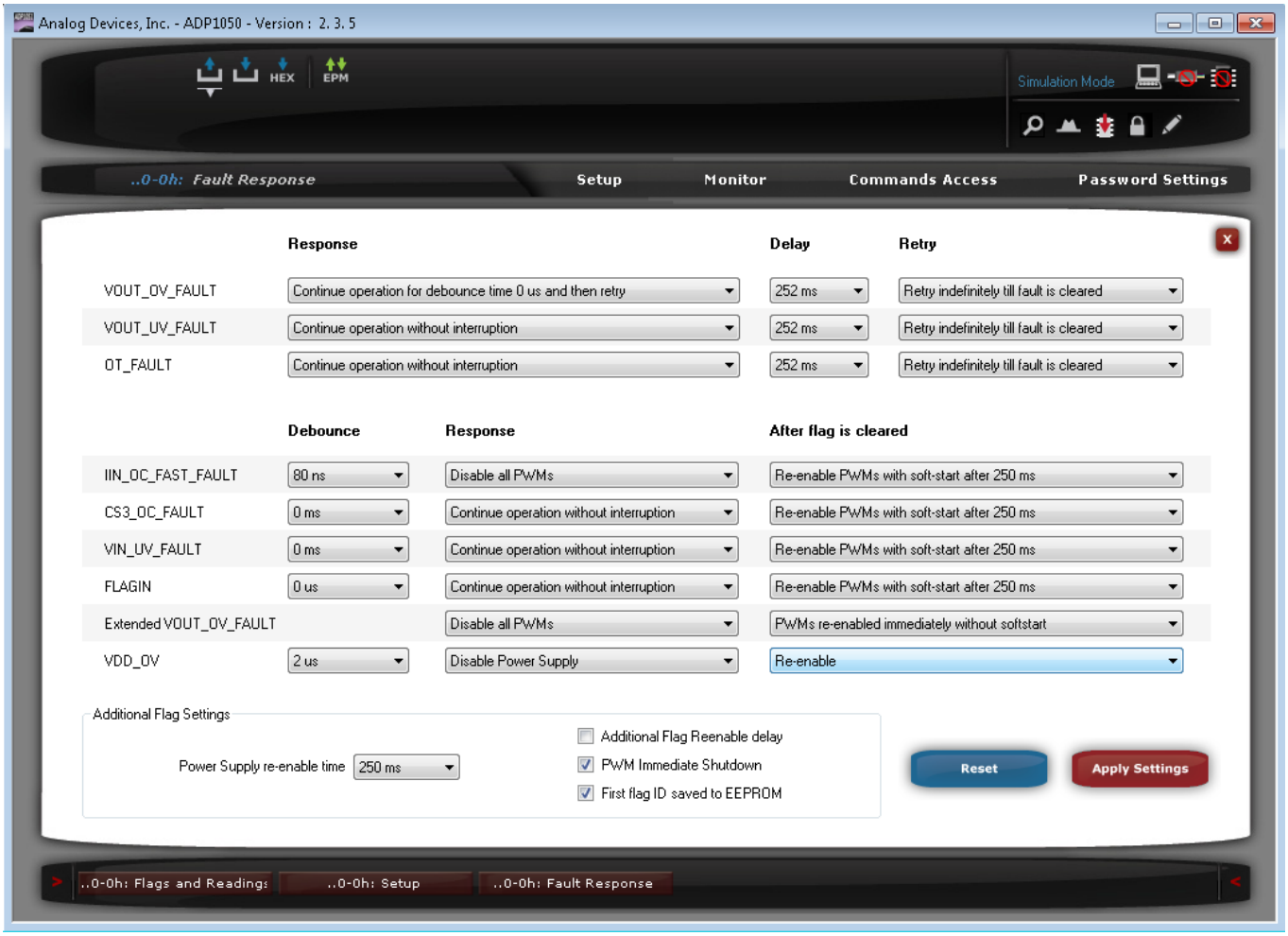


Figure 37. Fault Response Window

TRIMMING

This test allows the entire power supply to be calibrated and trimmed digitally through the ADP1050 in the production environment.

All the ADP1050 parts are factory calibrated. The trimming is not needed if the voltage and current sense resistors have a high enough accuracy (see the ADP1050 data sheet for details). However, the ADP1050 can be retrimmed by the user to compensate for errors introduced by external components. All trimming can be initiated from the **Trim Settings** window (see Figure 38), accessed via the **Setup** tab.

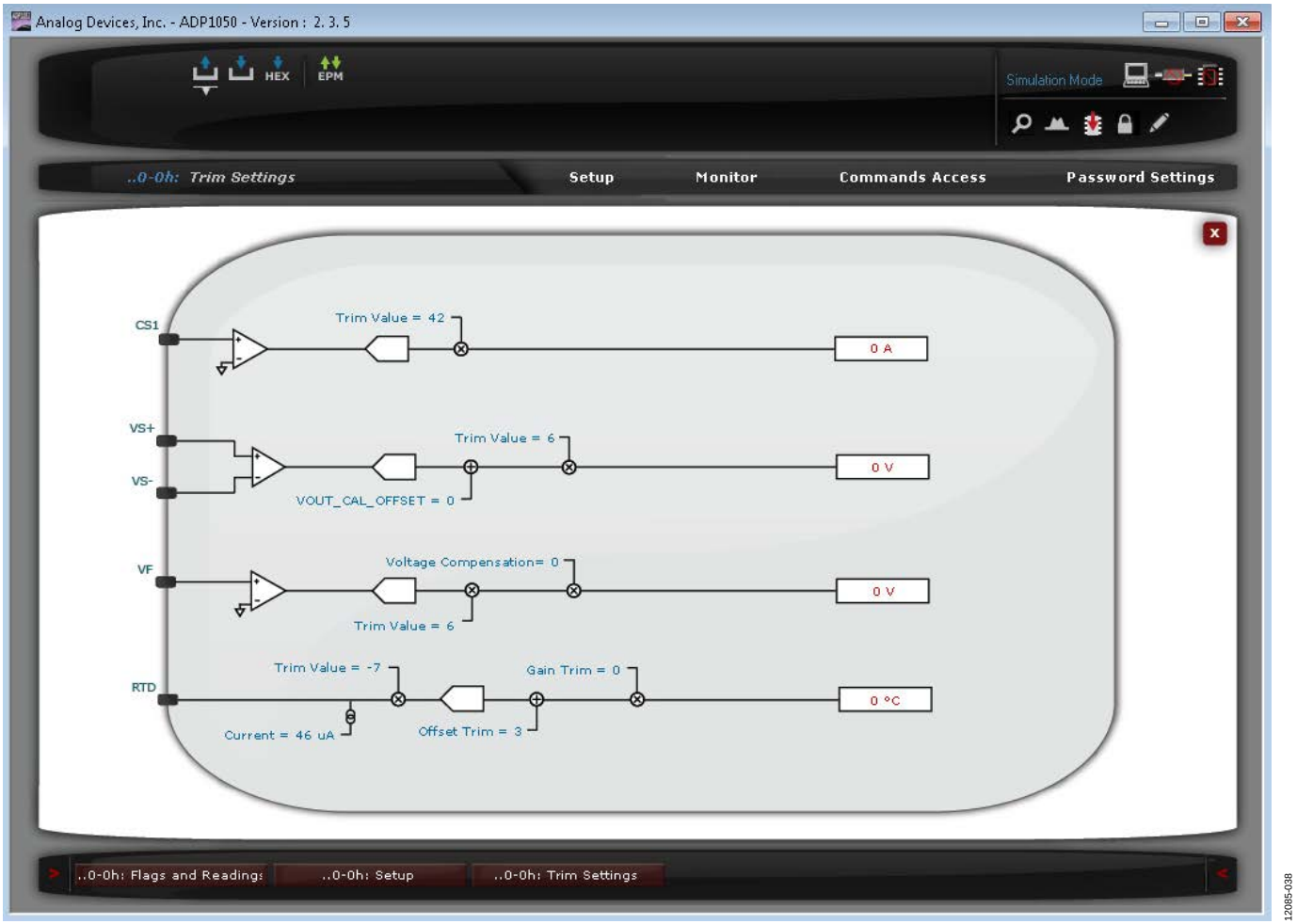


Figure 38. Trimming Settings Window

SYNCHRONIZATION

Synchronization as a Slave Device

This test can be done by applying an external clock signal to the TP25 test point. Alternatively, an external clock signal (such as an SYNO signal from the master device) can be applied to the SYNC pin of the J17 or J18 connector. The synchronization settings can be programmed in the **Sync Settings** window (see Figure 39).

To view the synchronization performance,

- Enable and disable synchronization.
- Set different delays to see the phase shift between master device and slave device.
- Program a different phase capture range.
- If the external clock signal is generated by a signal generator, program the clock signal in sweep mode or burst mode to see the synchronization locking or unlocking.

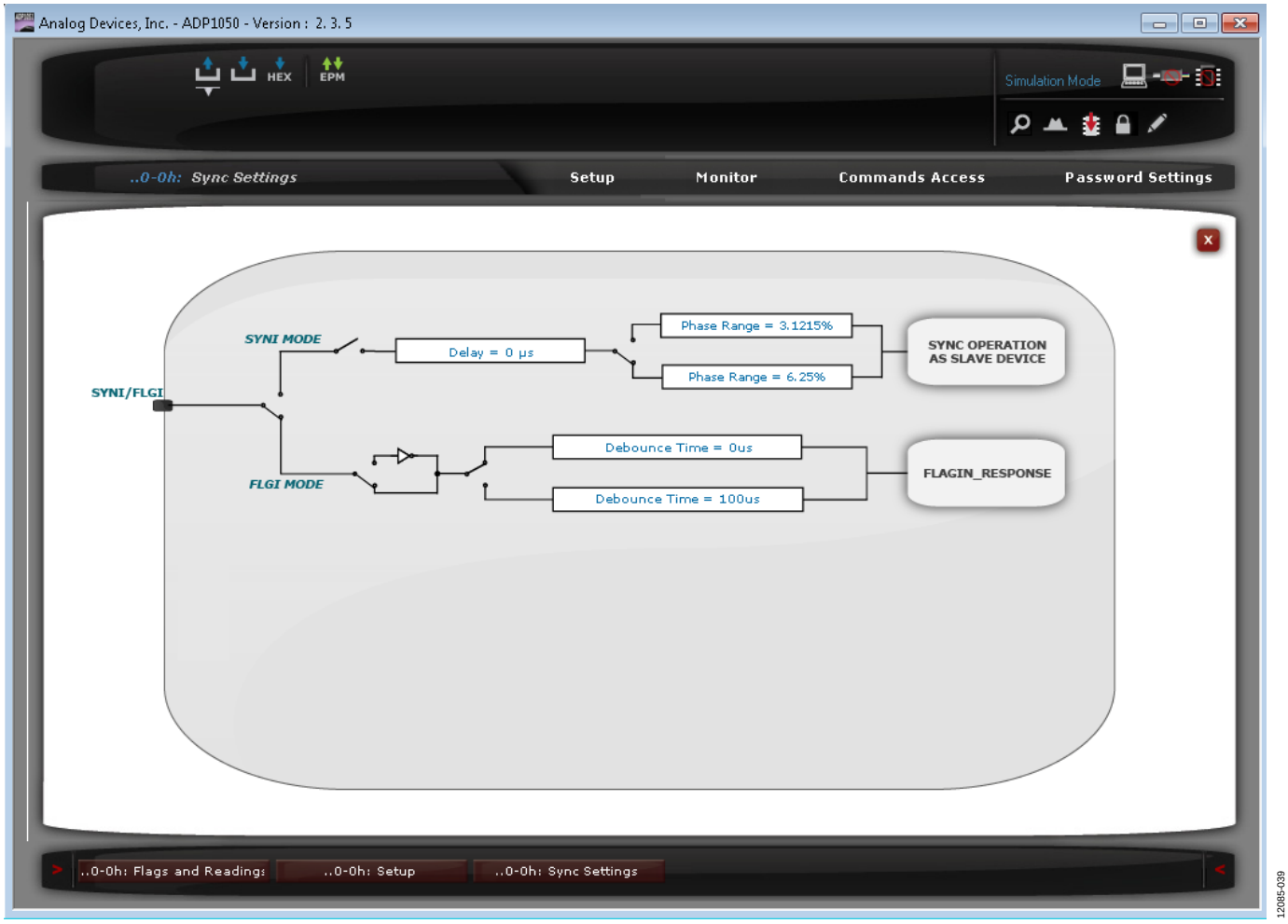


Figure 39. Sync Settings Window

POWER GOOD SIGNAL

This test can be conducted by setting a fault condition, which is used to trigger a PGOOD flag and to pull down the PG/ALT pin. In the **PGOOD Settings** window (see Figure 41), program which fault signal asserts the PGOOD flag. When a fault triggers the PGOOD flag, the D17 LED turns off, indicating that the power supply is not good. Figure 40 shows an example of a VOUT_UV_FAULT flag triggering the PGOOD output (PG/ALT pin).

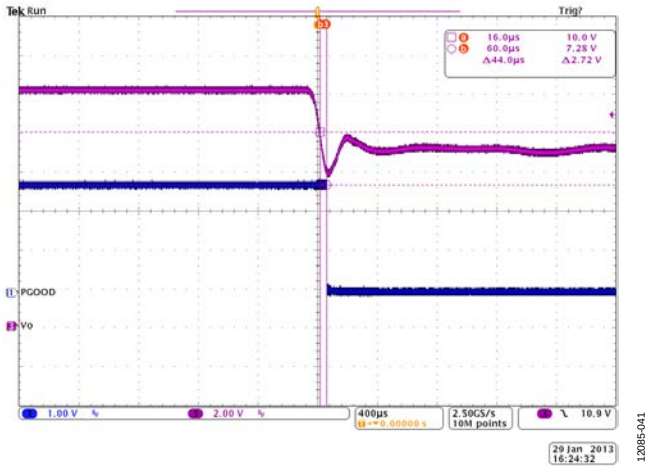


Figure 40. A VOUT_UV_FAULT Flag to Trigger PGOOD Output

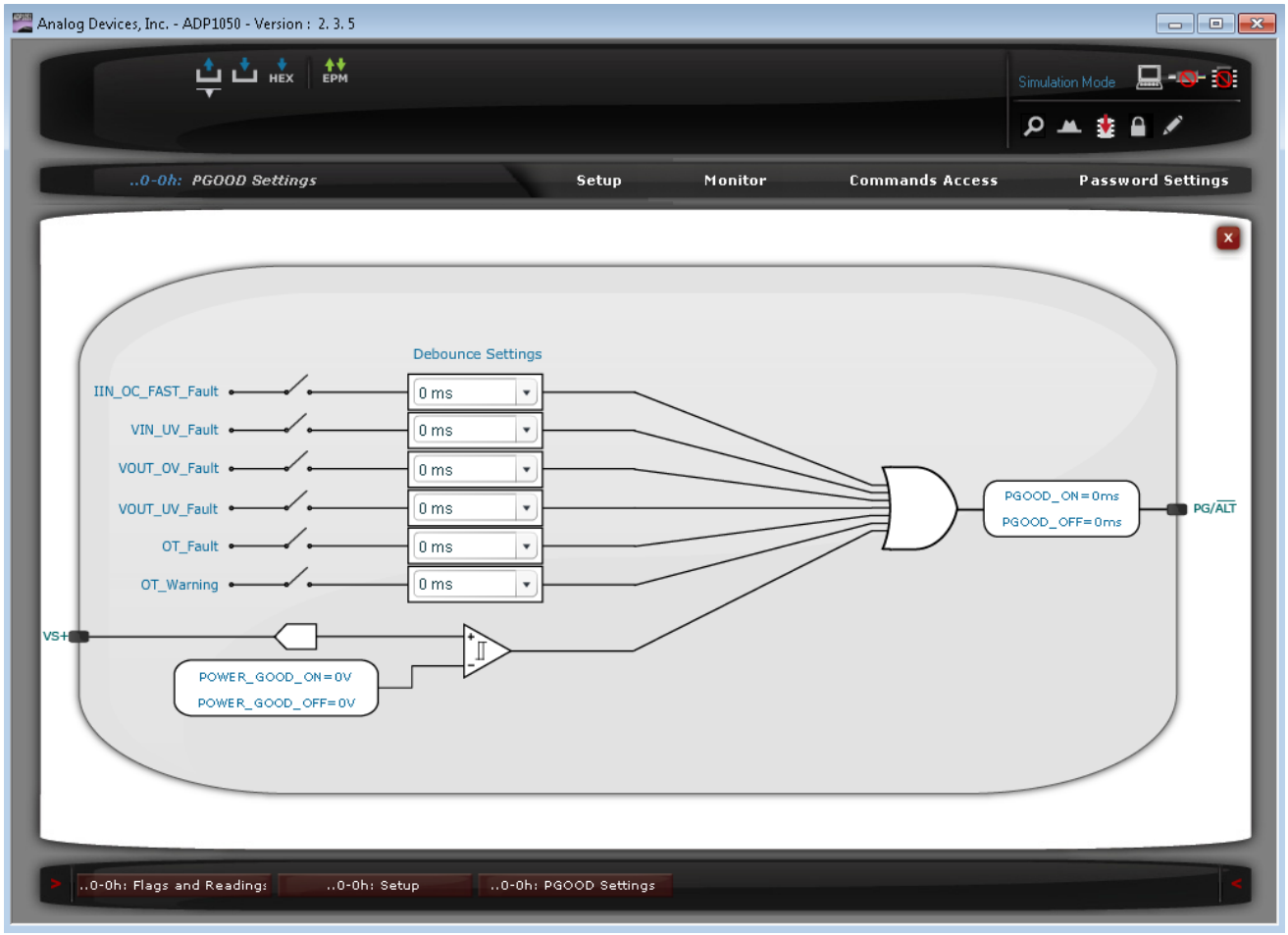


Figure 41. PGOOD Settings Window

ADDITIONAL GRAPHS

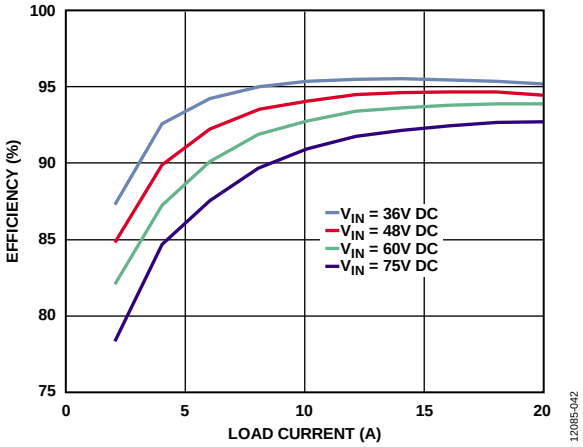


Figure 42. Efficiency Curve at 36 V DC, 48 V DC, 60 V DC, and 75 V DC Input

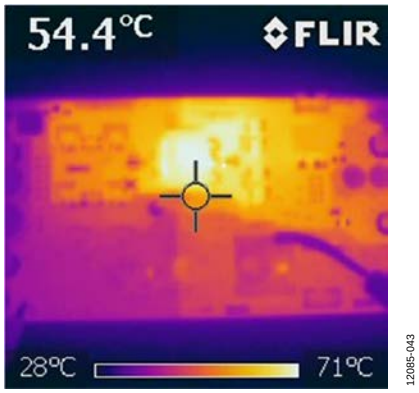


Figure 43. Thermal Image at 36 V DC Input, 20 A load, No Airflow

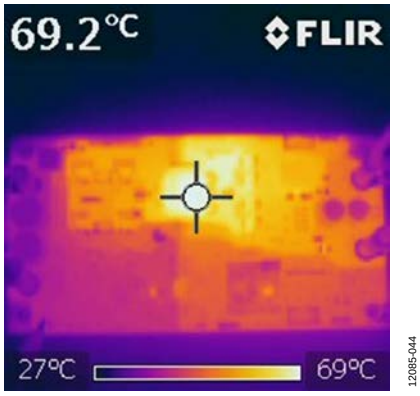


Figure 44. Thermal Image at 48 V DC Input, 20 A Load, No Airflow

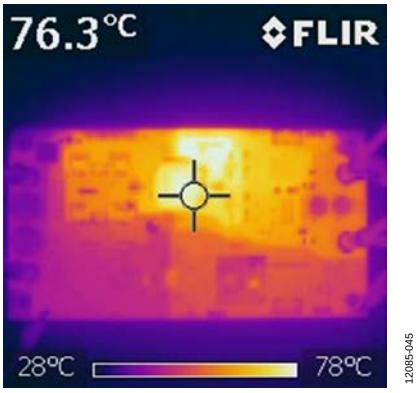


Figure 45. Thermal Image at 60 V DC Input, 20 A Load, No Airflow

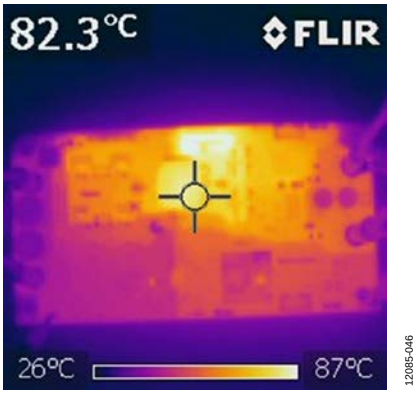


Figure 46. Thermal Image at 75 V DC Input, 20 A Load, No Airflow

SCHEMATICS AND ARTWORK

ADP1051-240-EVALZ

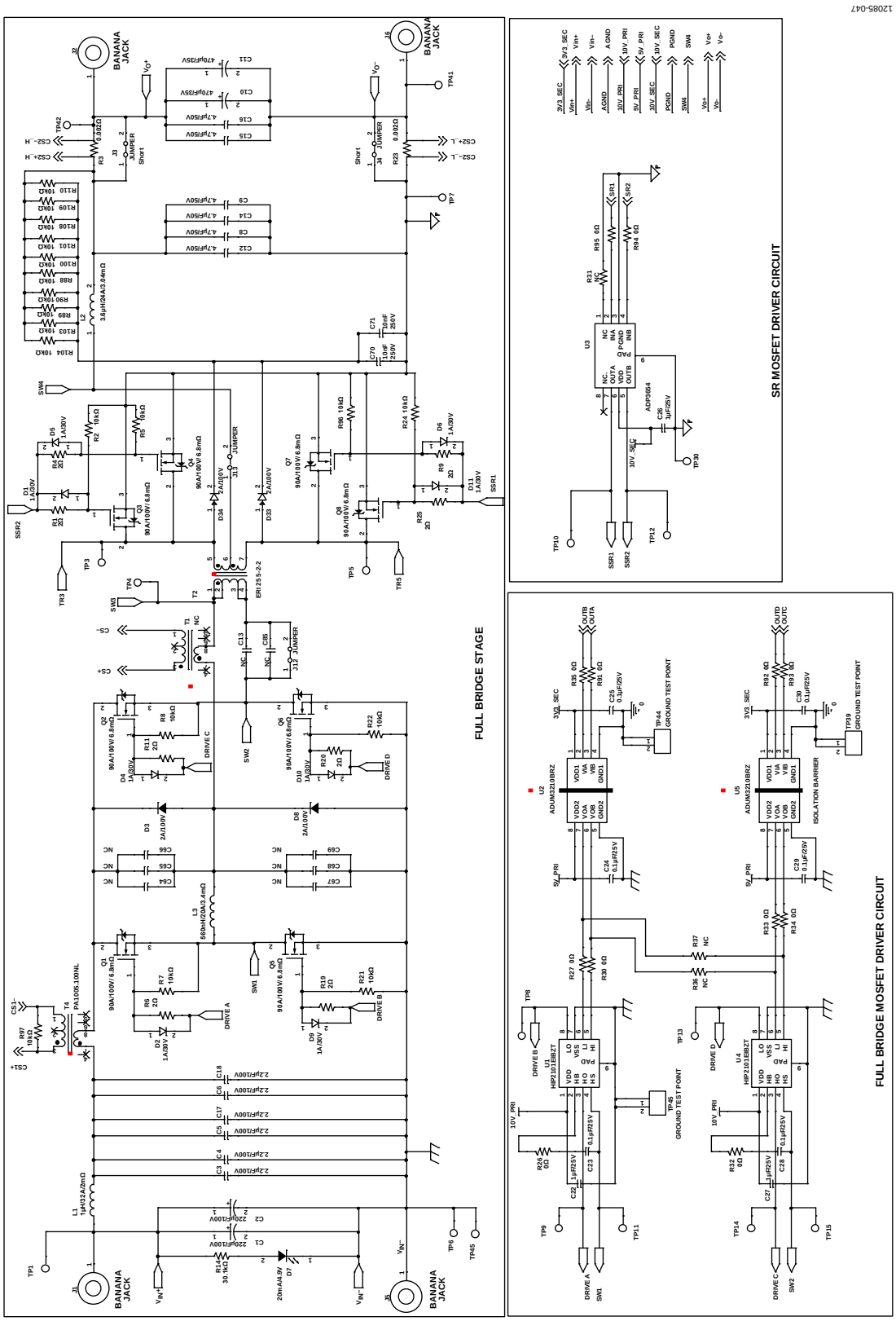


Figure 47. ADP1051-240-EVALZ Evaluation Board Schematic—Part I

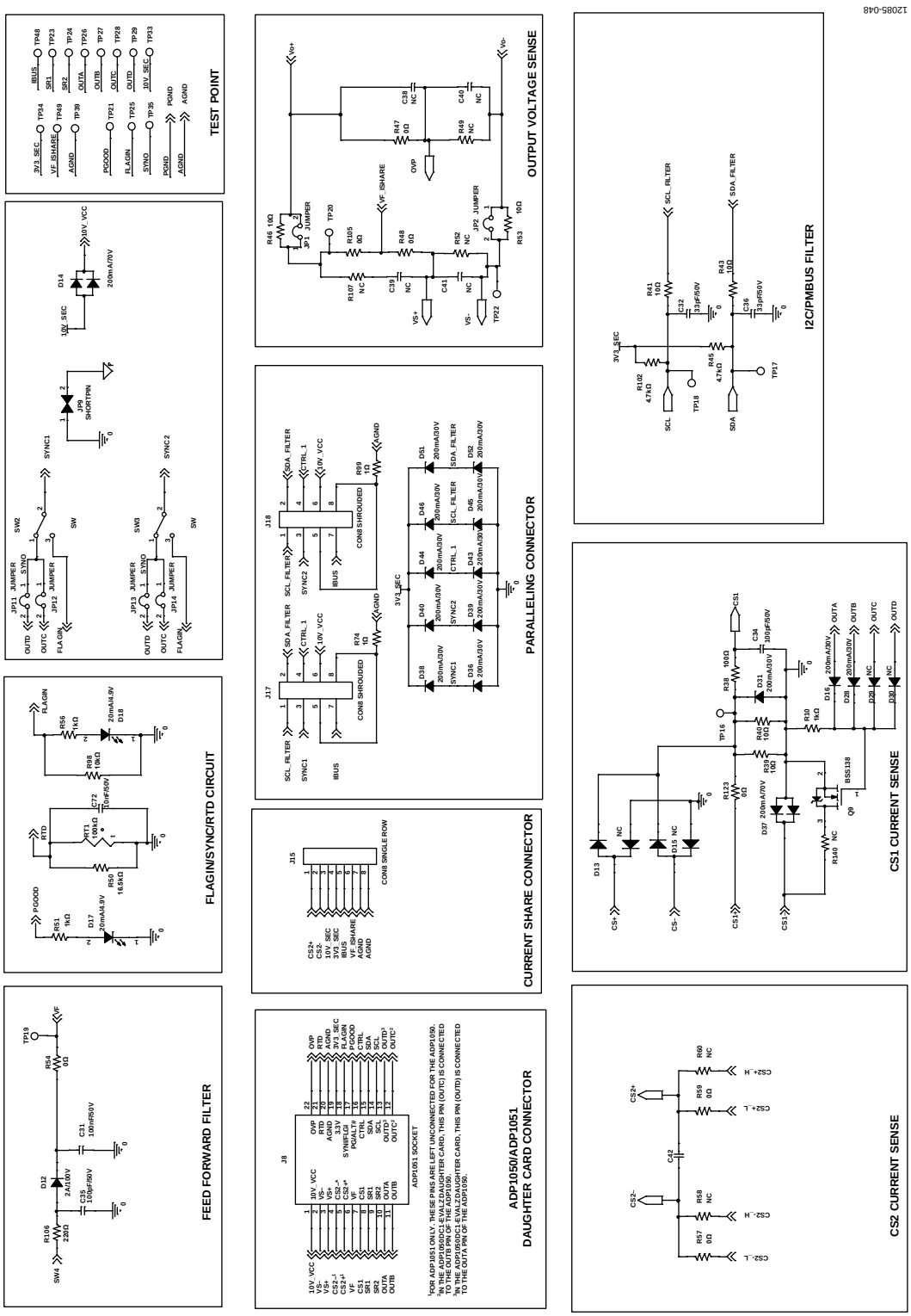


Figure 48. ADP1051-240-EVALZ Evaluation Board Schematic—Part II

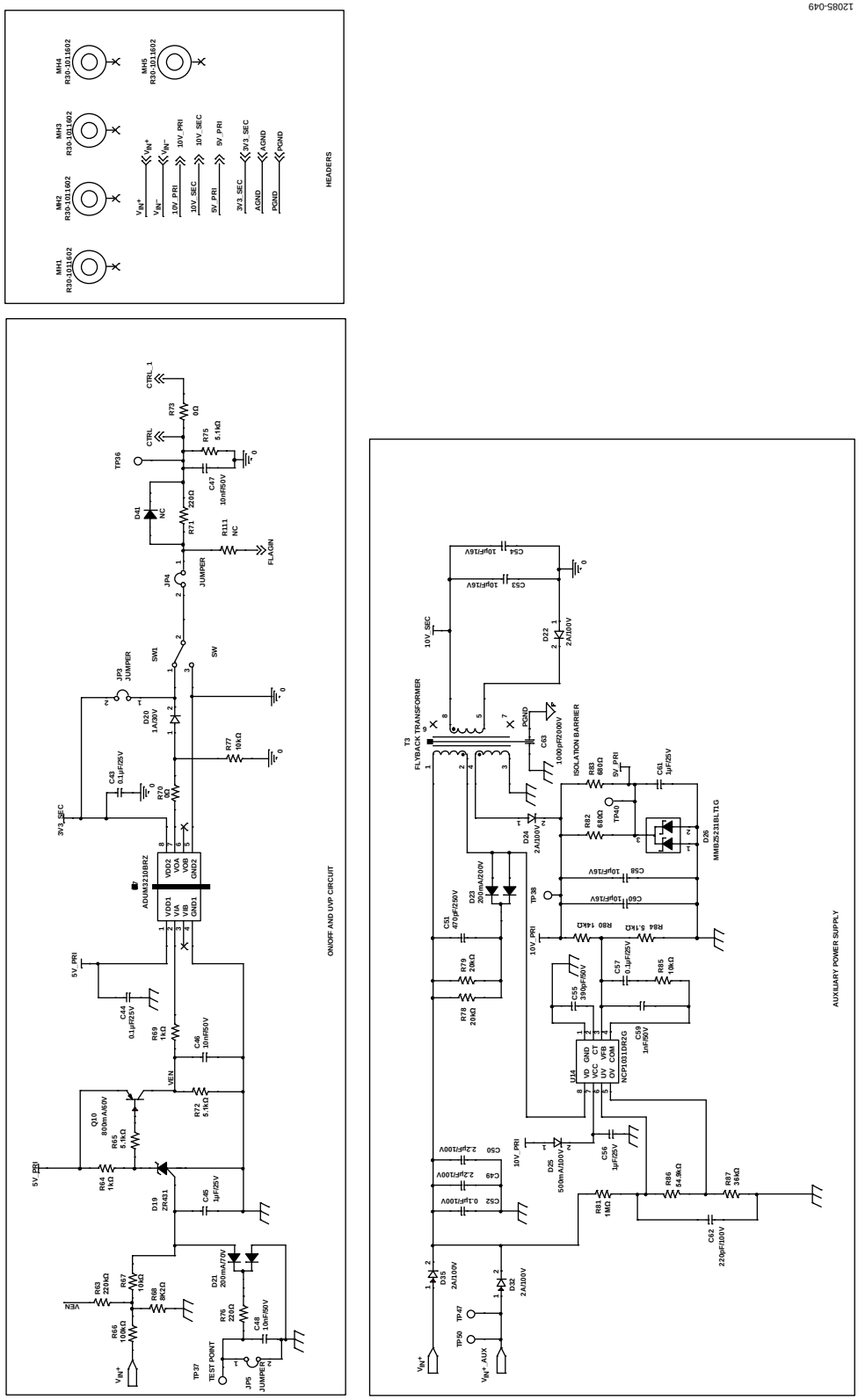


Figure 49. ADP1051-240-EVALZ Evaluation Board Schematic—Part III

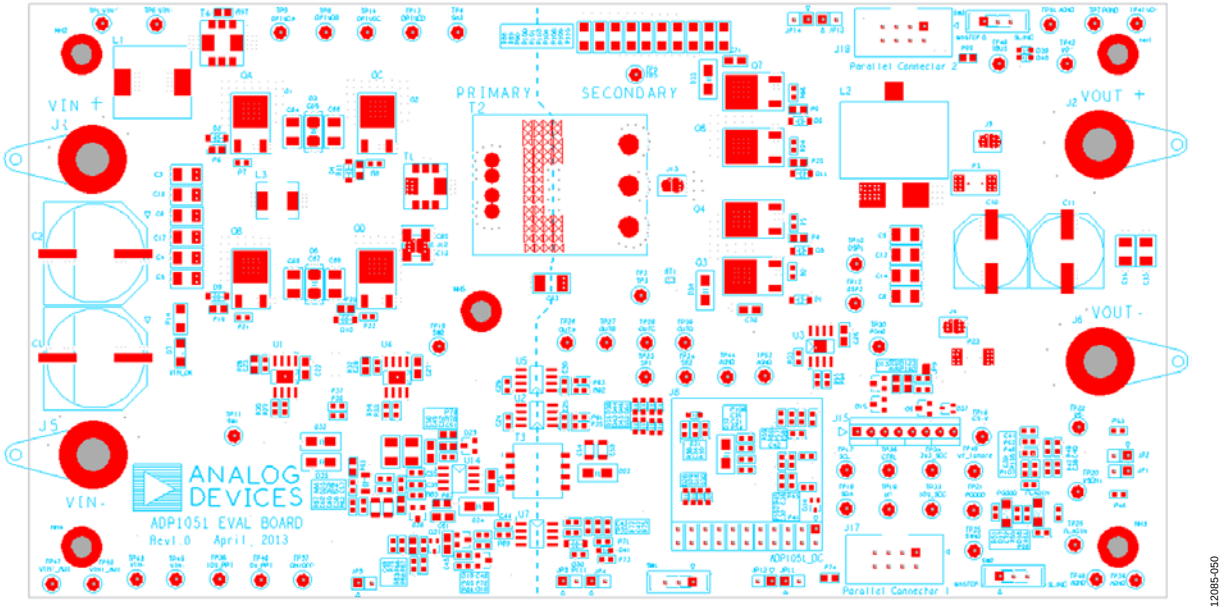


Figure 50. PCB Layout, Silkscreen Layer

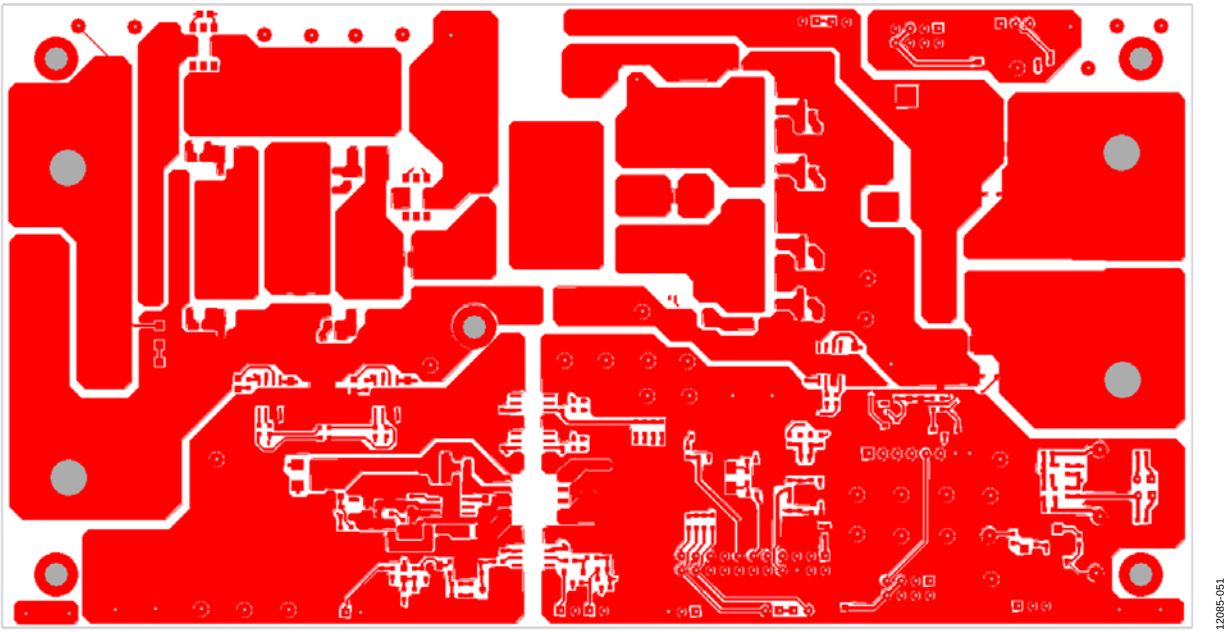


Figure 51. PCB Layout, Top Layer

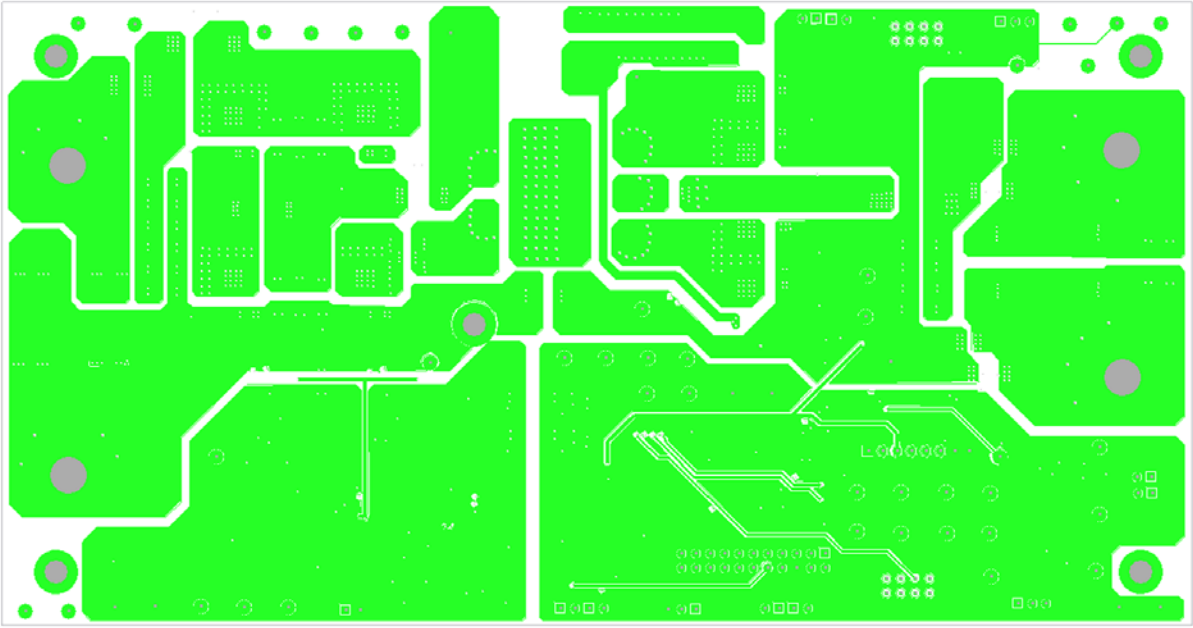


Figure 52. PCB Layout, Layer 2

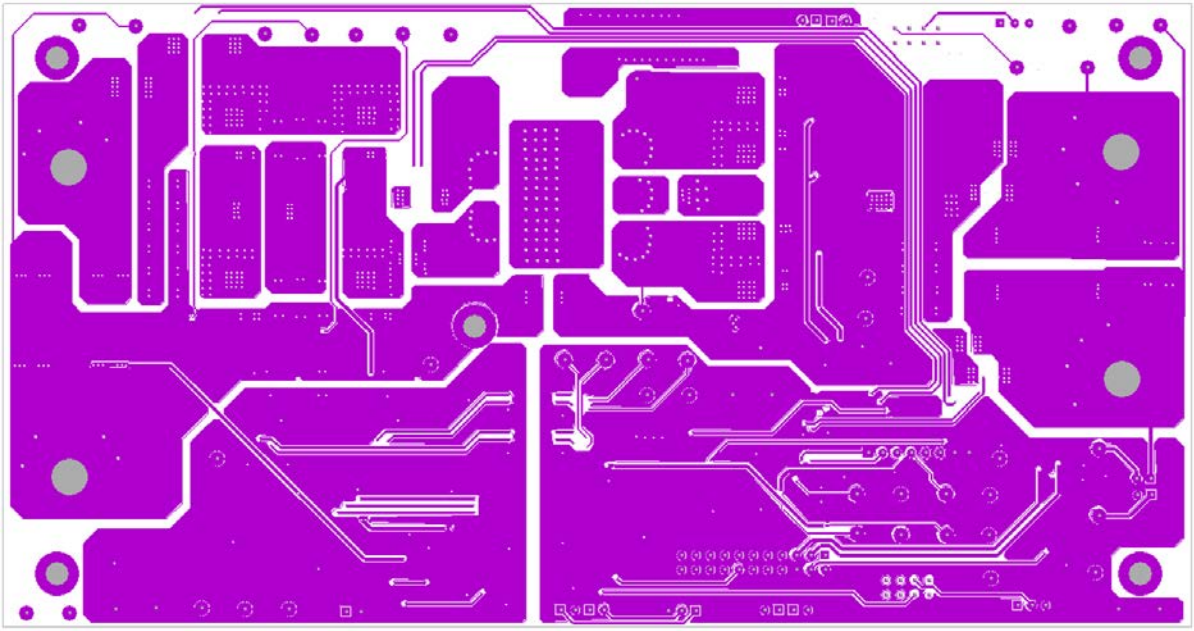


Figure 53. PCB Layout, Layer 3

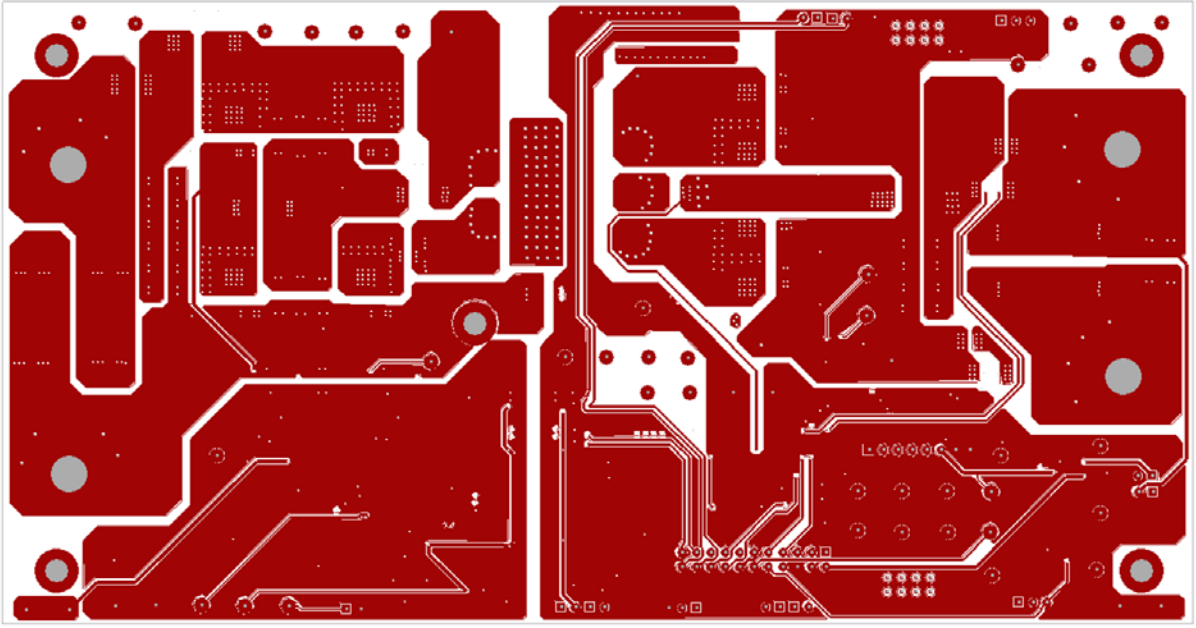


Figure 54. PCB Layout, Layer 4

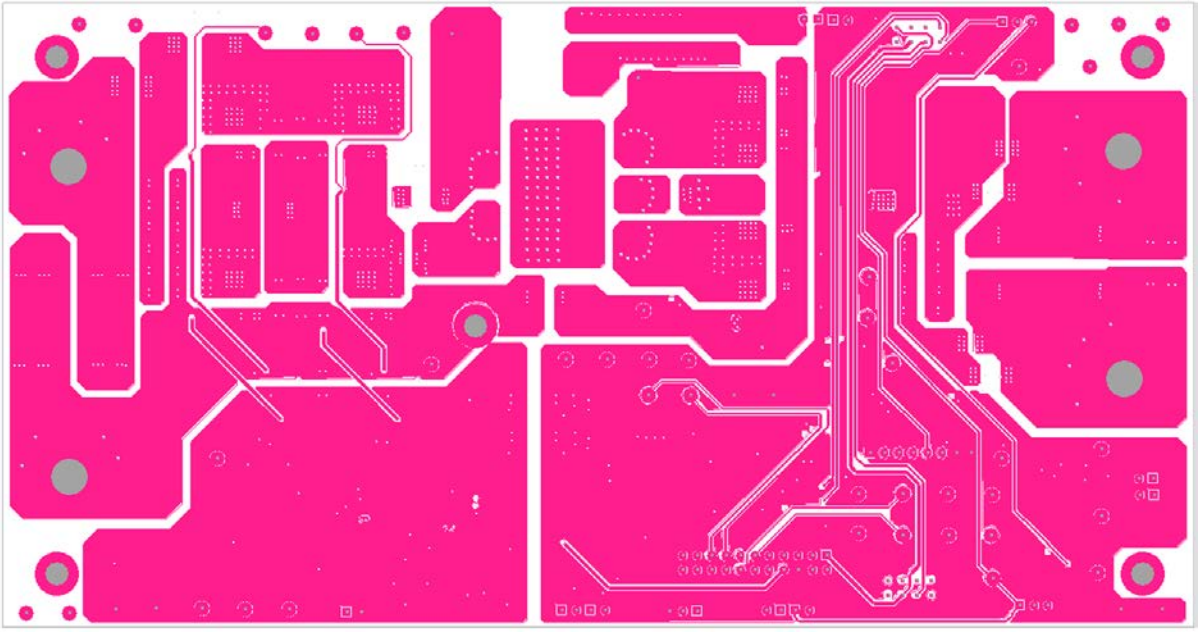


Figure 55. PCB Layout, Layer 5

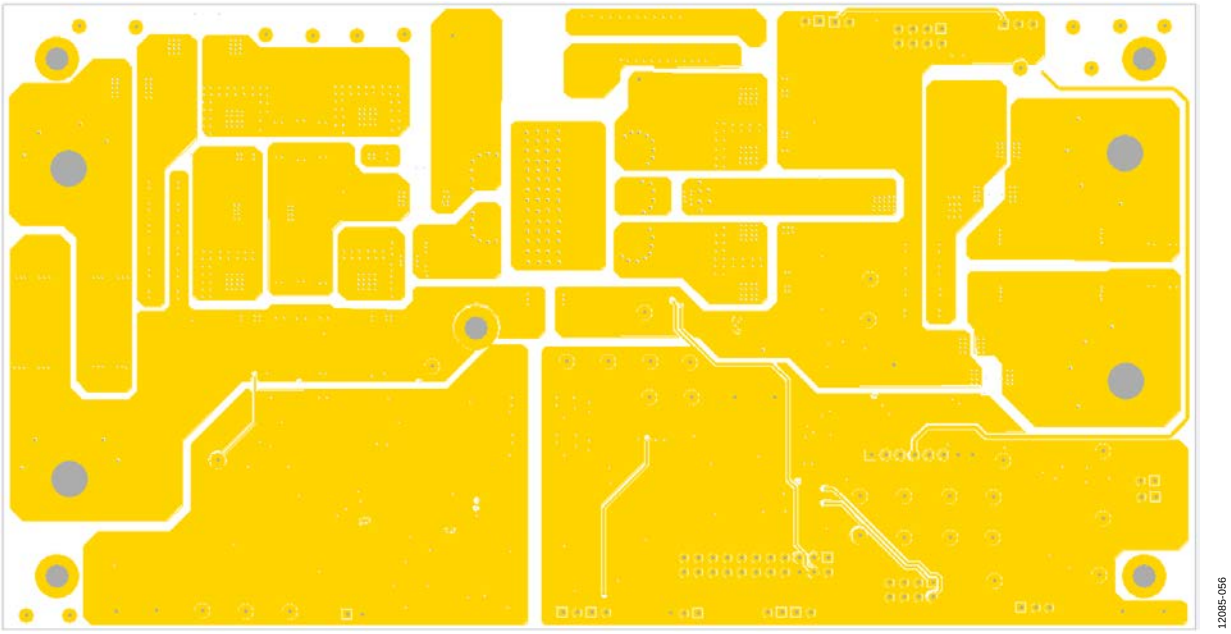


Figure 56. PCB Layout, Bottom Layout

ADP1050DC1-EVALZ

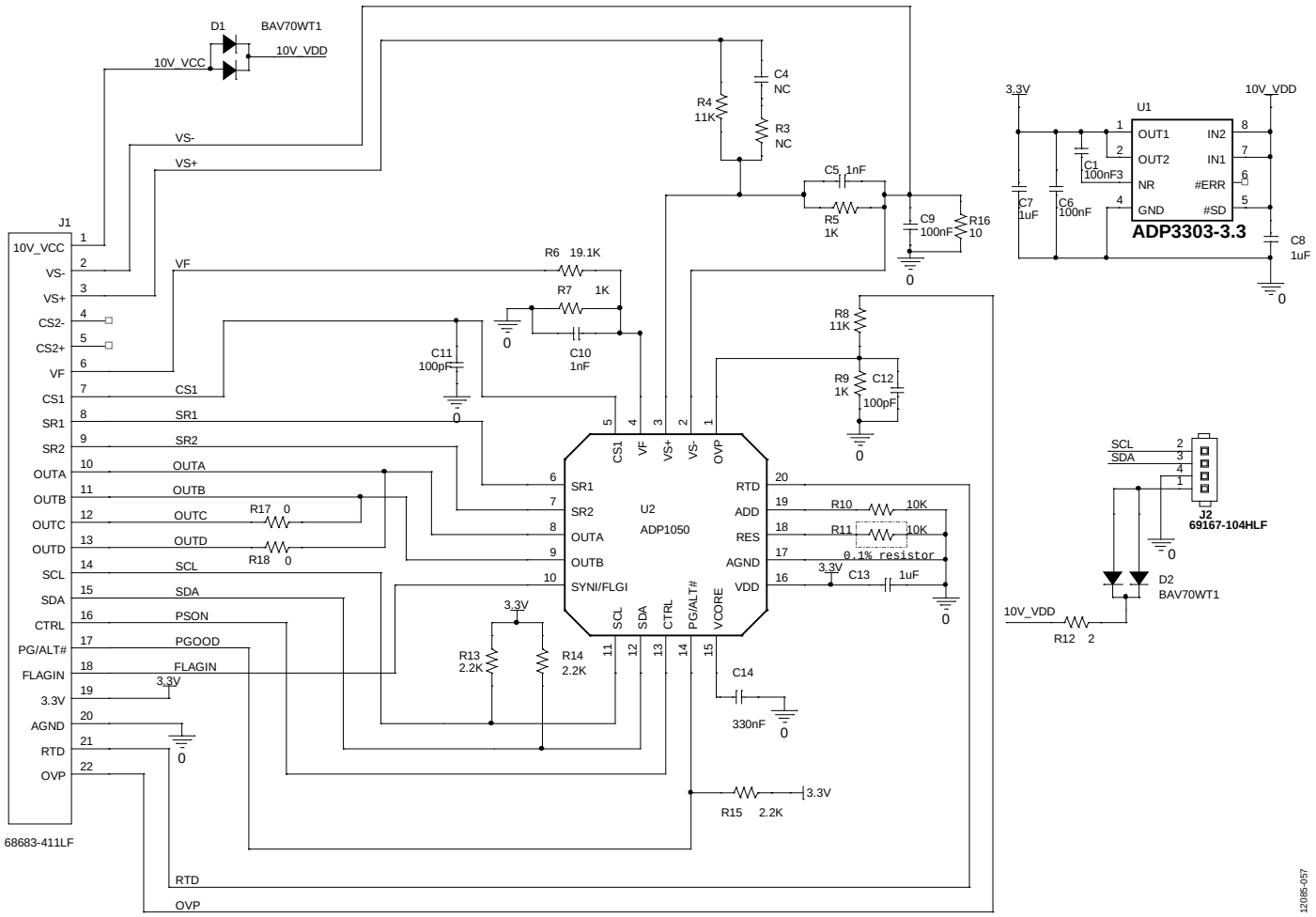
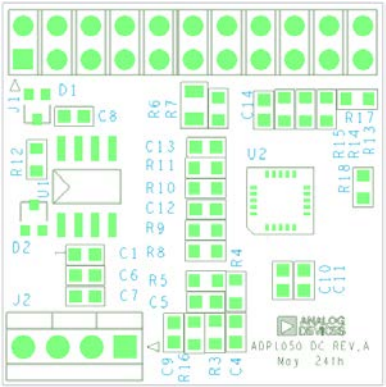
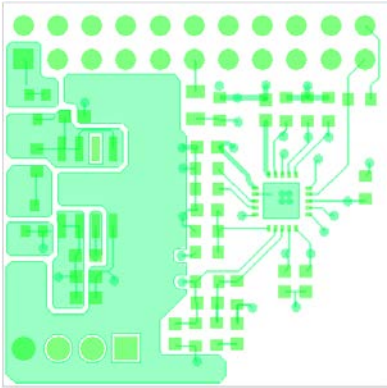


Figure 57. ADP1050DC1-EVALZ Daughter Card Schematic



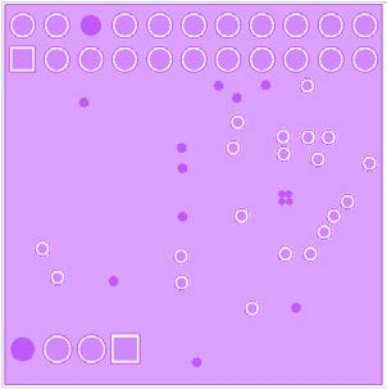
12085-058

Figure 58. PCB Layout, Silkscreen Layer



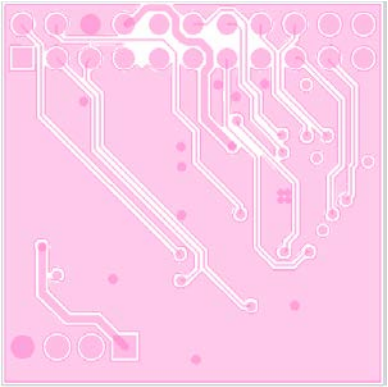
12085-059

Figure 59. PCB Layout, Top Layer



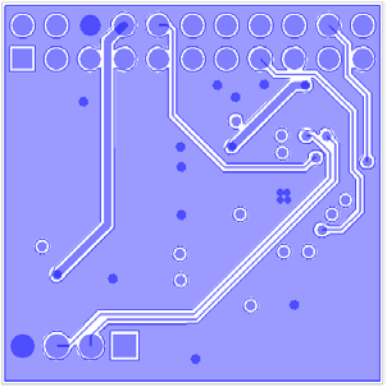
12085-060

Figure 60. PCB Layout, Layer 2



12085-061

Figure 61. PCB Layout, Layer 3



12085-062

Figure 62. PCB Layout, Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 7. ADP1051-240-EVALZ Evaluation Board

Qty	Reference Designator	Part Number[1] Manufacturer	Part Number[1] Digi-Key	Footprint	Description
2	C1, C2	EEEFK2A221AM	PCE4866TR-ND	SMC-AEC-TG-K16	Capacitor aluminum 220 µF 100 V 20% SMD
8	C3, C4, C5, C6, C17, C18, C49, C50	C3225X7R2A225K	445-4497-2-ND	C1210	Capacitor 2.2 µF/100 V X7R 1210
6	C8, C9, C12, C14, C15, C16	GRM32ER71H475KA88	490-1864-2-ND	C1210	Capacitor ceramic 4.7 µF 50 V 10% X7R 1210
2	C10, C11	EEEFK1V471AQ	PCE4862TR-ND	AL_CAP_H13	Capacitor aluminum 470 µF 35 V 20% SMD
2	C13, C85	C3225X7R2A225K	445-4497-2-ND	C1210	Capacitor ceramic 2.2 µF 100 V 10% X7R 1210
6	C22, C26, C27, C45, C56, C61	C2012X7R1E105K	445-1354-2-ND	C0805	Capacitor ceramic 1 µF 25 V 10% X7R 0805
9	C23, C24, C25, C28, C29, C30, C43, C44, C57	C1608X7R1E104K	445-1316-2-ND	C0603	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603
1	C31	C1608X7R1H104K	445-1314-2-ND	C0603	Capacitor ceramic 0.1 µF 50 V 10% X7R 0603
2	C32, C36	C1608COG1H330J	445-1257-2-ND	C0603	Capacitor ceramic 33 pF 50 V 5% NP0 0603
2	C34, C35	C1608COG1H101J	445-1281-2-ND	C0603	Capacitor ceramic 100 pF 50 V 5% NP0 0603
4	C38, C39, C40, C41	C1608COG1H102J	445-1293-2-ND	C0603	Capacitor ceramic 1000 pF 50 V 5% NP0 0603
1	C42	C1608X7R1H104K	445-1314-2-ND	C0603	Capacitor ceramic 0.1 µF 50 V 10% X7R 0603
4	C46, C47, C48, C72	C1608X7R1H103J	445-5089-2-ND	C0603	Capacitor ceramic 10 nF 50 V 5% X7R 0603
1	C51	C1608C0G2E471J	445-2318-2-ND	C0603	Capacitor ceramic 470 pF 250 V 5% NP0 0603
1	C52	C2012X7R2A104K	445-1418-2-ND	C0805	Capacitor ceramic 0.1 µF 100 V 10% X7R 0805
4	C53, C54, C58, C60	C3216X7R1C106K	445-4042-2-ND	C1206	Capacitor ceramic 10 µF 16 V 10% X7R 1206
1	C55	C1608C0G1H391J	445-1288-2-ND	C0603	Capacitor ceramic 390 pF 50 V 5% NP0 0603
1	C59	C1608COG1H102J	445-1293-2-ND	C0603	Capacitor ceramic 1 nF 50 V 5% NP0 0603
1	C62	C1608COG2A221J	445-2308-2-ND	C0603	Capacitor ceramic 220 pF 100 V 5% NP0 0603
1	C63	202S43W102KV4E	709-1053-2-ND	C1812	Capacitor ceramic 1 nF 2 kV 10% X7R 1812
6	C64, C65, C66, C67, C68, C69	C3225X7R1H335K	445-3936-2-ND	C1210	Capacitor ceramic 3.3 µF 50 V 10% X7R 1210
2	C70, C71	C2012X7R2E103K	445-2280-2-ND	C0805	Capacitor ceramic 10 nF 250 V X7R 0805
9	D1, D2, D4, D5, D6, D9, D10, D11, D20	MBR130LSFT1G	MBR130LSFT1GOSTR-ND	SOD123	Schottky diode 1 A 30 V SOD-123FL
9	D3, D8, D12, D22, D24, D32, D33, D34, D35	MURA110T3G	MURA110T3GOSTR-ND	SMA	Diode ultrafast 2 A 100 V SMA
3	D7, D17, D18	CMD15-21UBC/TR8	L62206CT-ND	D1206	LED blue clear 1206 SMD
2	D13, D15	BAV99	BAV99FSTR-ND	SOT23	Diode ultrafast HI COND 70 V SOT-23
3	D14, D21, D37	BAV70WT1G	BAV70WT1GOSTR-ND	SOT323	Diode switch dual CC 70 V SOT323
13	D16, D28, D31, D36, D38, D39, D40, D43, D44, D45, D46, D51, D52	BAT42WS-7	BAT42WSDITR-ND	SOD323	Schottky diode 30 V 200 MW SOD-323
1	D19	ZR431F01TA	ZR431F01TR-ND	SOT23-IC	IC VREF shunt PREC ADJ SOT-23
1	D23	MMBD1504A	MMBD1504ATR-ND	SOT23	Diode SS 200 V 200 MA SOT23
1	D25	EGL34B-E3/83	EGL34B-E3/83-ND	DO-213AA	Diode 0.5 A 100 V 50 NS MELF
1	D26	MMBZ5231BLT1G	MMBZ5231BLT1GOSTR-ND	SOT23	Diode Zener 5.1 V 225 MW SOT-23
3	D29, D30, D41	BAT42WS-7	BAT42WSDITR-ND	SOD323	Schottky diode 30 V 200 MW SOD-323
9	JP1, JP2, JP3, JP4, JP5, JP11, JP12, JP13, JP14	STC02SYAN	S9000-ND	HEADER-SR-2	Connector jumper shorting tin
1	JP9	N/A	N/A	Short pin	Single connect point of AGND and PGND
4	J1, J2, J5, J6	108-0740-001	J147-ND	B-JACK	Connector jack banana
4	J3, J4, J12, J13	N/A	N/A	PADJUMPER	Power connector jumper on PCB
1	J8	TSW-111-14-T-D	SAM1058-11-ND	HEADER-DR-22	Connector header 22 POS 0.100 dual tin 22 male pin 2.54
1	J15	PPC081LFBN-RC	S4108-ND	HEADER-I-SR-8	Single row 8 female pin 2.54 mm
2	J17, J18	75869-132LF	609-3530-ND	313-208-s2	Connector header 8 POS dual vertical PCB
1	L1	IHLP5050FDER1R0M01	541-1032-2-ND	IND-IHLP-5050FD	Power inductor 1.0 µH 32 A SMD
1	L2	#7443630420	N/A	LER-20-63	Power inductor 4.2 µH 24 A 3.04 mΩ SMD
		LER-20-63	N/A		Power Inductor 3.6 µH 30 A 2.3 mΩ SMD
1	L3	IHLP2525EZERR56M01	IHLP2525EZERR56M01-ND	2525ez	Power Inductor 0.56 µH 20 A SMD

Qty	Reference Designator	Part Number[1]		Footprint	Description
		Manufacturer	Digi-Key		
5	MH1, MH2, MH3, MH4, MH5	R30-1011602	952-1492-ND	MH	Standoff HEX M3 THR Brass 16 mm
8	QA, QB, QC, QD, Q3, Q4, Q7, Q8	IPD068N10N3 G	IPD068N10N3 G-ND	DPAK	MOSFET N-CH 100 V 90 A TO252-3
1	Q9	BSS138	BSS138TR-ND	SOT23	MOSFET N-CH 50 V 220 MA SOT-23
1	Q10	MMBT2907A	MMBT2907AFSTR-ND	SOT23	Transistor GP PNP AMP SOT-23
1	RT1	NCP15WF104F03RC	490-4803-2-ND	R0402	Thermistor 100 kΩ NTC 0402 SMD resistance 1% beta
12	R2, R5, R7, R8, R21, R22, R24, R67, R77, R85, R96, R98	CRCW060310K0JNTA	CRCW060310K0JNTA-ND	R0603	Resistor 10 kΩ 5% 1/10 W 0603 SMD
2	R3, R23	ERJ-M1WTF2M0U	P2.0NDTR-ND	R2512	Resistor 0.002 Ω 1 W 1% 2512
8	R1, R4, R6, R9, R11, R19, R20, R25	CRCW08052R00JNEA	541-2.0ATR-ND	R0805	Resistor 2 Ω 5% 1/8 W 0805 SMD
1	R10	CRCW060310K0JNTA	CRCW060310K0JNTA-ND	R0603	Resistor 10 kΩ 5% 1/10 W 0603 SMD
1	R14	CRCW120630K1FKEA	541-30.1KFTR-ND	R1206	Resistor 30.1 kΩ 1/4 W 1% 1206 SMD
2	R26, R32	CRCW08050000Z0EA	541-0.0ATR-ND	R0805	Resistor 0.0 Ω 1/8 W 0805 SMD
19	R27, R30, R33, R34, R35, R47, R48, R54, R57, R59, R70, R73, R91, R92, R93, R94, R95, R105, R123	CRCW06030000Z0EA	541-0.0GTR-ND	R0603	Resistor 0.0 Ω 1/10 W 0603 SMD
9	R31, R36, R37, R49, R58, R60, R107, R111, R140	CRCW06030000Z0EA	541-0.0GTR-ND	R0603	Resistor 0.0 Ω 1/10 W 0603 SMD
1	R38	CRCW0603100RFKEA	541-100HCT-ND	R0603	Resistor 100 Ω 1/10 W 1% 0603 SMD
2	R39, R40	CRCW080510R0FKEA	541-10.0CTR-ND	R0805	Resistor 10.0 Ω 1/8 W 1% 0805 SMD
4	R41, R43, R46, R53	CRCW060310R0FKEA	541-10.0HTR-ND	R0603	Resistor 10.0 Ω 1/10 W 1% 0603 SMD
2	R45, R102	CRCW06034K10JNEA	541-4.7KGCT-ND	R0603	Resistor 4.7 kΩ 1/10 W 5% 0603 SMD
1	R50	CRCW060316K5FKTA	CRCW060316K5FKTA-ND	R0603	Resistor 16.5 kΩ 1% 1/10 W 0603 SMD
4	R51, R56, R64, R69	CRCW06031K00FKEA	541-1.00KHCT-ND	R0603	Resistor 1.00 kΩ 1/10 W 1% 0603 SMD
1	R52	CRCW06031K00FKEA	541-1.00KHCT-ND	R0603	Resistor 1.00 kΩ 1/10 W 1% 0603 SMD
1	R63	CRCW0603220KFKEA	541-220KHTR-ND	R0603	Resistor 220 kΩ 1/10 W 1% 0603 SMD
3	R65, R72, R75	CRCW06035K10JNEA	541-5.1KGCT-ND	R0603	Resistor 5.1 kΩ 1/10 W 5% 0603 SMD
1	R66	CRCW0805100KJNEA	541-100KATR-ND	R0805	Resistor 100 kΩ 1/8 W 5% 0805 SMD
1	R68	CRCW06038K20FKEA	541-8.20KHCT-ND	R0603	Resistor 8.20 kΩ 1/10 W 1% 0603 SMD
3	R71, R76, R106	CRCW0603220RJNEA	541-220GCT-ND	R0603	Resistor 220 Ω 1/10 W 5% 0603 SMD
2	R74, R99	CRCW08051R00JNEA	541-1.0ATR-ND	R0805	Resistor 1 Ω 5% 1/8 W 0805
2	R78, R79	CRCW080520R0JNEA	541-20ACT-ND	R0805	Resistor 20 Ω 1/8 W 5% 0805 SMD
1	R80	CRCW060314K0FKEA	541-14.0KHTR-ND	R0603	Resistor 14.0 kΩ 1/10 W 1% 0603 SMD
1	R81	CRCW08051M00FKEA	541-1.00MCTR-ND	R0805	Resistor 1.00 MΩ 1/8 W 1% 0805 SMD
2	R82, R83	CRCW0805680RJNEA	541-680ACT-ND	R0805	Resistor 680 Ω 1/8 W 5% 0805 SMD
1	R84	CRCW06035K10FKEA	541-5.10KHTR-ND	R0603	Resistor 5.10 kΩ 1/10 W 1% 0603 SMD
1	R86	CRCW060354K9FKEA	541-54.9KHTR-ND	R0603	Resistor 54.9 kΩ 1/10 W 1% 0603 SMD
1	R87	CRCW060336K0FKEA	541-36.0KHTR-ND	R0603	Resistor 36.0 kΩ 1/10 W 1% 0603 SMD
10	R88, R89, R90, R100, R101, R103, R104, R108, R109, R110	CRCW120620K0JNEA	541-20KETR-ND	R1206	Resistor 20 kΩ 1/4 W 5% 1206 SMD
1	R97	CRCW080510K0JNEA	541-10KATR-ND	R0805	Resistor 10 kΩ 1/8 W 5% 0805 SMD
3	SW1, SW2, SW3	EG1218	EG1903-ND	SPDT-SLSW	Switch slide SPDT 30 V 2 A PC MNT

Qty	Reference Designator	Part Number[1] Manufacturer	Part Number[1] Digi-Key	Footprint	Description
43	TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP33, TP34, TP35, TP36, TP37, TP38, TP40, TP41, TP42, TP47, TP48, TP49, TP50, TP51	5010	5010K-ND	TP-70	Test point PC
3	TP39, TP44, TP45	GTP002	N/A	TP-70 dual	Ground test point
1	T1	PA1005.100NL	553-1529-2-ND	P820X	Transformer current sense 2.0 MH 1:100 SMD
1	T2	#750341378	N/A	BDC_2512	Transformer ER25 5:2:2
		BDC-25-69	N/A		Transformer ER25 5:2:2
1	T3	#750341379	N/A	PBSER9-77	36 V to 75 V input, 12 V 0.25 A pri output, 12 V, 0.25 A sec output, ER9.5 22:8:8
		BSER9-77	N/A		36 V to 75 V input, 12 V pri output, 12 V sec output, ER9.5 22:8:8
1	T4	PA1005.100NL	553-1529-2-ND	P820X	Transformer current sense 2.0 MH 1:100 SMD
2	U1, U4	HIP2101EIBZT	HIP2101EIBZTTR-ND	8-SOIC-EP	IC driver half bridge 100 V 8EPSOIC
3	U2, U5, U7	ADUM3210BRZ-RL7	ADUM3210BRZ-RL7TR-ND	8-SOIC	*i*Coupler 2-CH 8-lead SOIC
1	U3	ADP3654ARDZ-R7	ADP3654ARDZ-R7-ND	8-SOIC_N_EP	IC MOSFET DVR 4 A dual HS SOIC_N_EP
1	U14	NCP1031DR2G	NCP1031DR2GOSTR-ND	8-SOIC	IC CTRLR PWM OTP OVD HV 8SOIC

[1] N/A = not applicable.

Table 8. ADP1050DC1-EVALZ Daughter Card

Qty	Reference Designator	Part Number[1, 2] Manufacturer	Part Number[1, 2] Digi-Key	Footprint	Description
3	C1, C6, C9	C1608X7R1H104K	445-1316-2-ND	C0603	Capacitor ceramic 0.1 µF 25 V 10% X7R 0603
1	C4	N/C	N/C	C0603	Capacitor ceramic 1 nF 50 V 5% COG 0603
2	C5, C10	C1608COG1H102J	445-1293-2-ND	C0603	Capacitor ceramic 1 nF 50 V 5% COG 0603
3	C7, C8, C13	C1608X7R1C105K	445-1604-2-ND	C0603	Capacitor ceramic 1 µF 16 V 10% X7R 0603
2	C11, C12	C1608COG1H101J	445-1281-2-ND	C0603	Capacitor ceramic 100 pF 50 V 5% NP0 0603
1	C14	C1608X7R1H334K	445-5950-2-ND	C0603	Capacitor ceramic 330 nF 50 V 10% X7R 0603
1	D2	BAV70WT1G	BAV70WT1GOSTR-ND	SOT323	Diode switch dual CC 70 V SOT323
1	J1	PPPC112LFBN-RC	S7114-ND	Header-dr-22	Connector header FMAL 22 POS 0.1" DL gold
1	J2	69167-104HLF	609-2411-ND	HEADER-L-SR-4	Connector header 4 POS SGL PCB 30 gold
1	R3	N/C	N/C	R0603	Resistor 200 Ω 1/10 W 1% 0603 SMD
2	R4, R8	TNPW060311K0BEEA	TNP11.0KAATR-ND	R0603	Resistor 11 kΩ 1/10 W 0.1% 0603 SMD
3	R5, R7, R9	TNPW06031K00BEEA	TNP1.00KAATR-ND	R0603	Resistor 1.00 kΩ 1/10 W 0.1% 0603 SMD
1	R6	CRCW080519K1FKEA	541-19.1KCTR-ND	R0805	Resistor 19.1 kΩ 1/8 W 1% 0805 SMD
1	R10	CRCW060310K0FKEA	541-10.0KHTR-ND	R0603	Resistor 10 kΩ 1/10 W 1% 0603 SMD
1	R11	TNPW060310K0BEEA	TNP10.0KAATR-ND	R0603	Resistor 10 kΩ 1/10 W 0.1% 0603 SMD
1	R12	CRCW06032R00FKEA	541-2.00HHTR-ND	R0603	Resistor 2 Ω 1/10 W 1% 0603 SMD
3	R13, R14, R15	CRCW06032K20FKEA	541-2.20KHTR-ND	R0603	Resistor 2.2 kΩ 1/10 W 1% 0603 SMD
1	R16	CRCW060310R0FKEA	541-10.0HTR-ND	R0603	Resistor 10 Ω 1/10 W 1% 0603 SMD
2	R17, R18	RC0603JR-070RL	311-0.0GRTR-ND	R0603	Resistor 0 Ω 1/10 W 5% 0603 SMD
1	U1	ADP3303ARZ-3.3	ADP3303ARZ-3.3-ND	SO8	IC regulator LDO 200 mA 3.3 V 8-lead SOIC
1	U2	ADP1050ACPZ	N/A	CP-20-10	Digital controller

[1] N/A = not applicable.
[2] N/C = no connection.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

UG12085-0-1/14(0)

ANALOG DEVICES

www.analog.com