

Quick Start Guide for Testing the **AD9250/AD6673** Analog-to-Digital Converters (ADCs) Evaluation Boards Using the **HSC-ADC-EVALDZ** FPGA-Based Capture Board

FEATURES

Evaluation boards for the **AD9250/AD6673** high speed analog-to-digital converters (ADCs) using the **HSC-ADC-EVALDZ** capture board

EQUIPMENT NEEDED

- An analog signal source and antialiasing filter
- An analog clock source
- A PC with a USB 2.0 port, recommended (USB 1.1-compatible)
- The **AD9250** or the **AD6673** ADC evaluation board
- The **HSC-ADC-EVALDZ** FPGA-based data capture board

DOCUMENTS NEEDED

- AD9250** data sheet
- AD6673** data sheet
- AN-905** Application Note, *VisualAnalog Converter Evaluation Tool User Manual* (Analog Devices, Inc., 2007)
- High Speed Converter Division, **AN-878** Application Note, *High Speed ADC SPI Control Software User Manual* (Analog Devices, 2006–2007)
- High Speed Converter Division, **AN-877** Application Note, *Interfacing to High Speed ADCs via SPI* (Analog Devices, 2005–2007)

SOFTWARE NEEDED

- VisualAnalog
- SPIController

GENERAL DESCRIPTION

This user guide describes the **AD9250/AD6673** evaluation boards that can be used to evaluate Analog Devices, Inc., high speed **AD9250-250**, **AD9250-170**, or the **AD6673-250** ADCs.

Full performance details are provided in the **AD9250/AD6673** data sheets and should be consulted in conjunction with this user guide. All documents and software are available at www.analog.com/fifo. For more information, email highspeed.converters@analog.com.

EVALUATION BOARD CONNECTION DIAGRAM

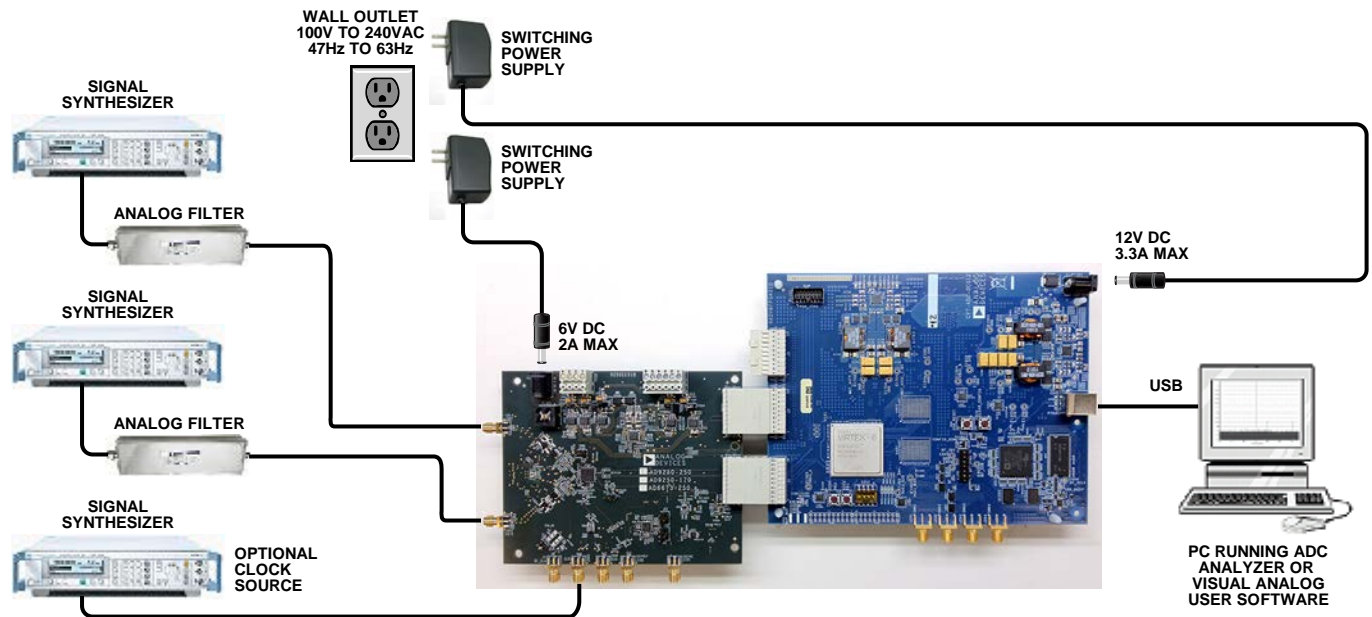


Figure 1.

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REVISION HISTORY

11/12—Revision 0: Initial Version

EVALUATION BOARD SOFTWARE/HARDWARE QUICK START PROCEDURES

INSTALLING THE SOFTWARE

To install the software, go to www.analog.com/fifo, and download and install the following:

- VisualAnalog, Rev 1.9.20.21 or later.
- SPI Control Software, Rev 1.0.91.3 or later.

SETTING UP THE HARDWARE AND THE SOFTWARE

1. Connect the [AD9250](#) or the [AD6673](#) evaluation board and the [HSC-ADC-EVALDZ](#) board together, as shown in Figure 1.
2. Connect one 6 V, 2 A switching power supply (such as the CUI EPS060250UH-PHP-SZ supplied) to the [AD9250](#) or the [AD6673](#) board. Ensure that the 6 V power supply is used.
3. Connect one 12 V, 3.3 A switching power supply (such as the V-Infinity ETSA120330UDC-P5P-SZ supplied) to the [HSC-ADC-EVALDZ](#) board. Ensure that a 12 V power supply is used.
4. Connect the [HSC-ADC-EVALDZ](#) board to the PC with a USB cable. (Connect to P702.)
5. On the [AD9250](#) or the [AD6673](#) evaluation board, ensure that the jumpers are installed on the P205, P206, and P204 headers for default setup.
6. On the [AD9250](#) or the [AD6673](#) evaluation board, provide a clean, low jitter clock source to Connector J505 at the desired ADC conversion rate. If the [AD9250](#) or the [AD6673](#) input clock divider is used, provide a clock into the J505 connector at the appropriate rate. The input clock level must be between 10 dBm and 14 dBm.
7. On the [AD9250](#) or the [AD6673](#) evaluation board, use a clean signal generator with low phase noise to provide an input signal to the analog input at Connector J301 (Channel A) and/or Connector J303 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band, band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.) For the input level to be near the full-scale of the ADC, the generator level must be set to 8 dBm to 12 dBm, and this level depends on the input frequency and any losses in band-pass filters.

8. Open the **VisualAnalog** software on the PC. The [AD9250](#) or the [AD6673](#) should be listed in the status bar of the **New Canvas** window (see Figure 2).

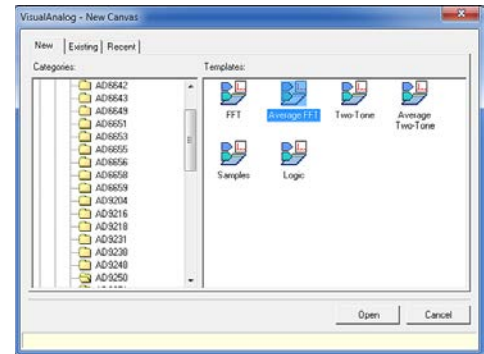


Figure 2. New Canvas Window

9. Select the template that corresponds to the type of testing that needs to be performed.
10. Select the **ADC Data Capture Settings** window and click the **Capture Board** tab (see the red box in Figure 3).
11. In the FPGA box, select the [AD9250_12_04_11_1225.mcs](#) program or the [AD6673_12_04_11_1225.mcs](#) program to configure the FPGA.
12. Click **Program** to download the file to the FPGA. The **CONFIG_DONE** LED should illuminate on the [HSC-ADC-EVALDZ](#) board indicating that the FPGA has been correctly programmed.

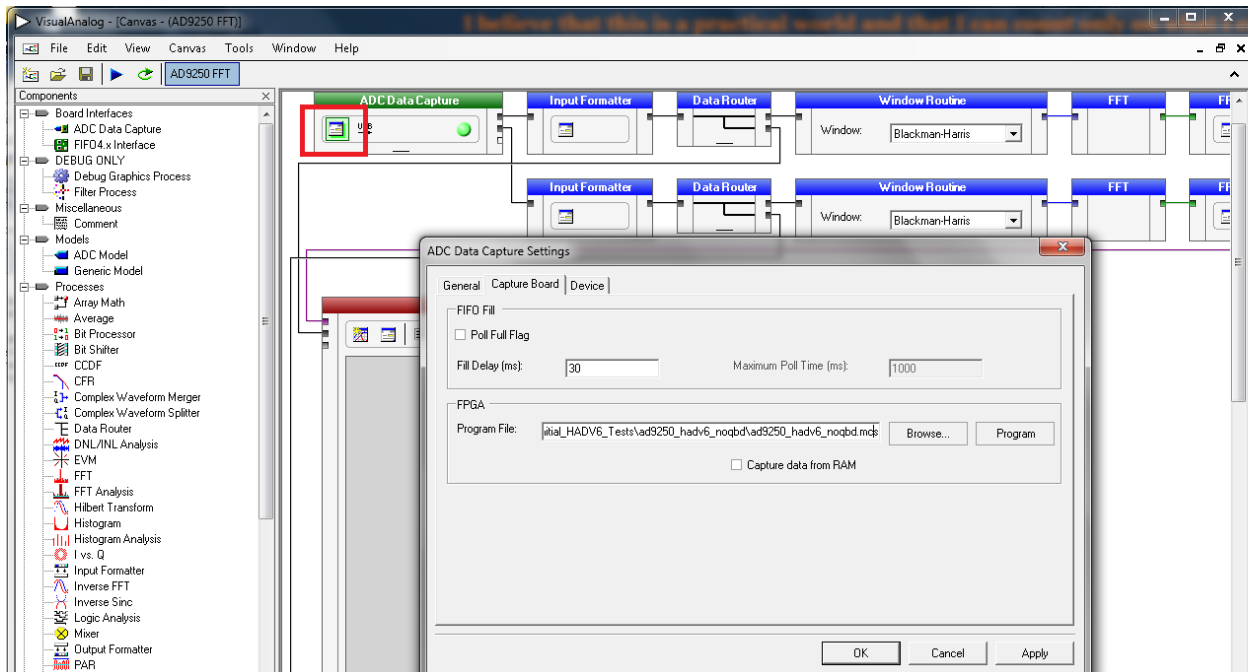


Figure 3. VisualAnalog, ADC Data Capture Settings Window

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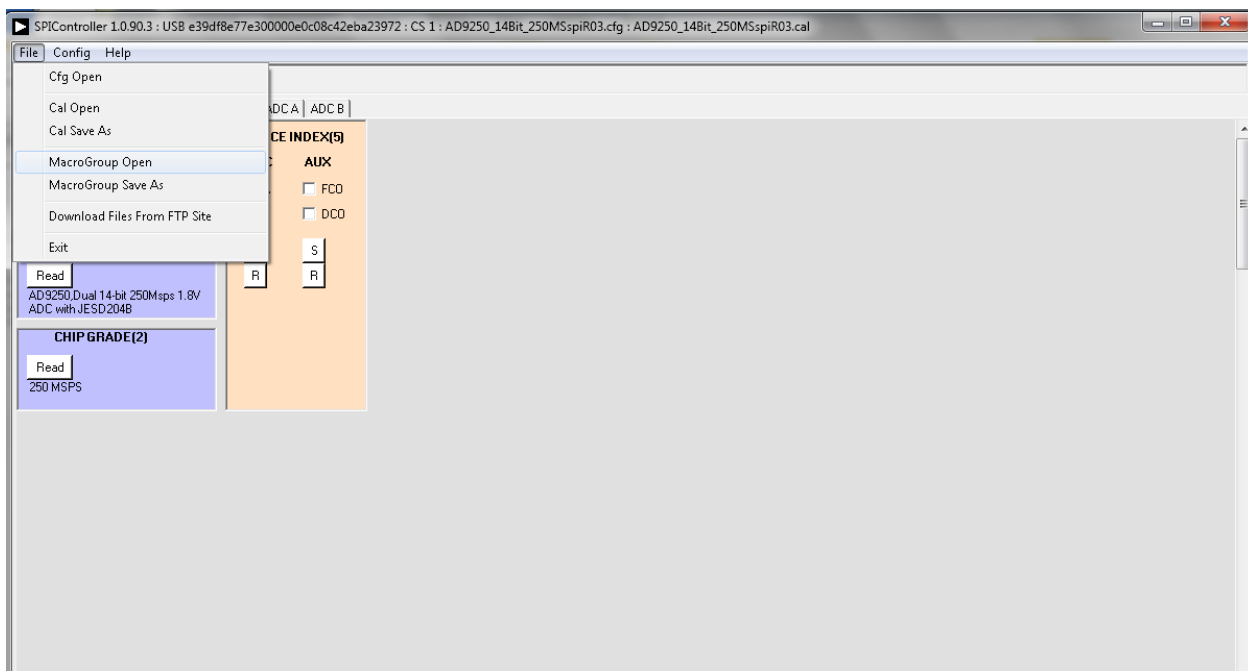


Figure 4. SPIController Software, MacroGroup Open

11140-004

13. Open the **SPIController** software. If prompted for a configuration file, select the **AD9250_14Bit_250MSspiR03.cfg** or **AD6673_14Bit_250MSspiR03.cfg**. If not, check the title bar of the window to see which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the correct configuration file. Note that the **CHIP ID(1)** field may be filled whether the correct SPIController configuration file is loaded or not.
14. In the **SPIController** software, click **File > MacroGroup Open** (see Figure 4).
15. Select the **AD9250_M2L2_SPI.mgp** or the **AD6673_M2L2_SPI.mgp** file and click **Open**.
16. Select **Config > Launch Macro Editor** (see Figure 5). The **MarcoEditor** window opens (see Figure 6).



Figure 5. SPIController Software, Launch Macro Editor

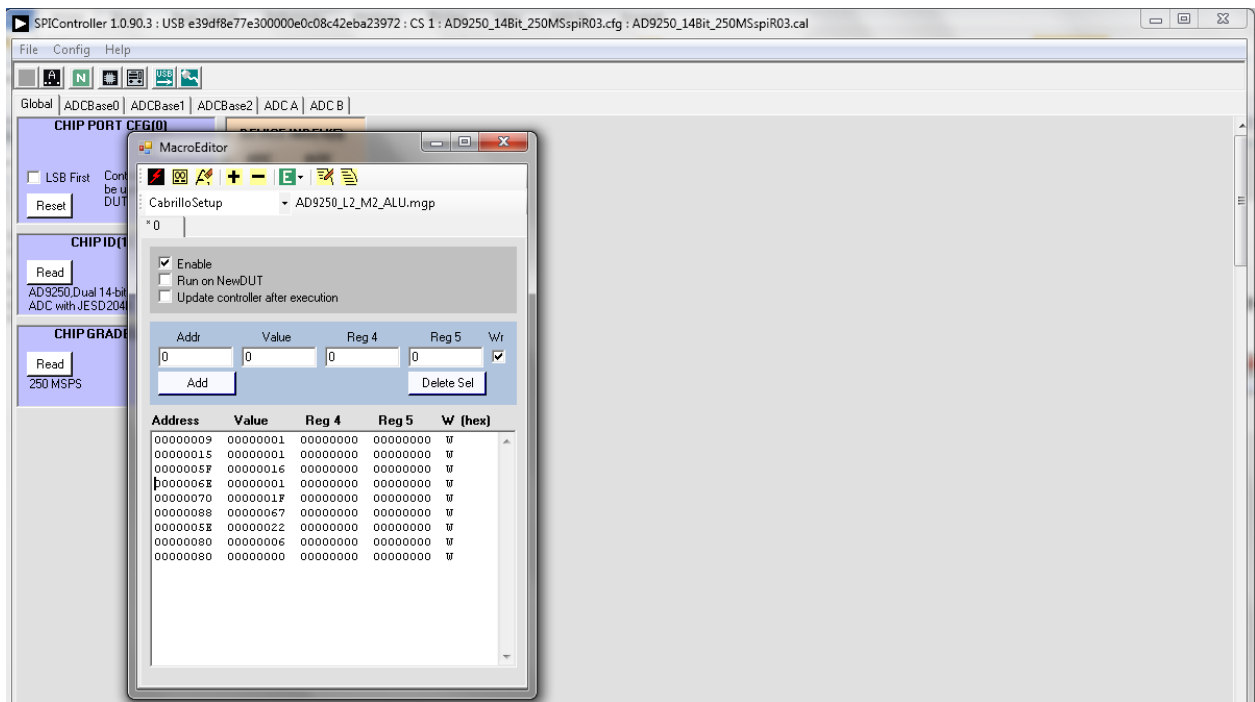


Figure 6. SPIController Software, MacroEditor

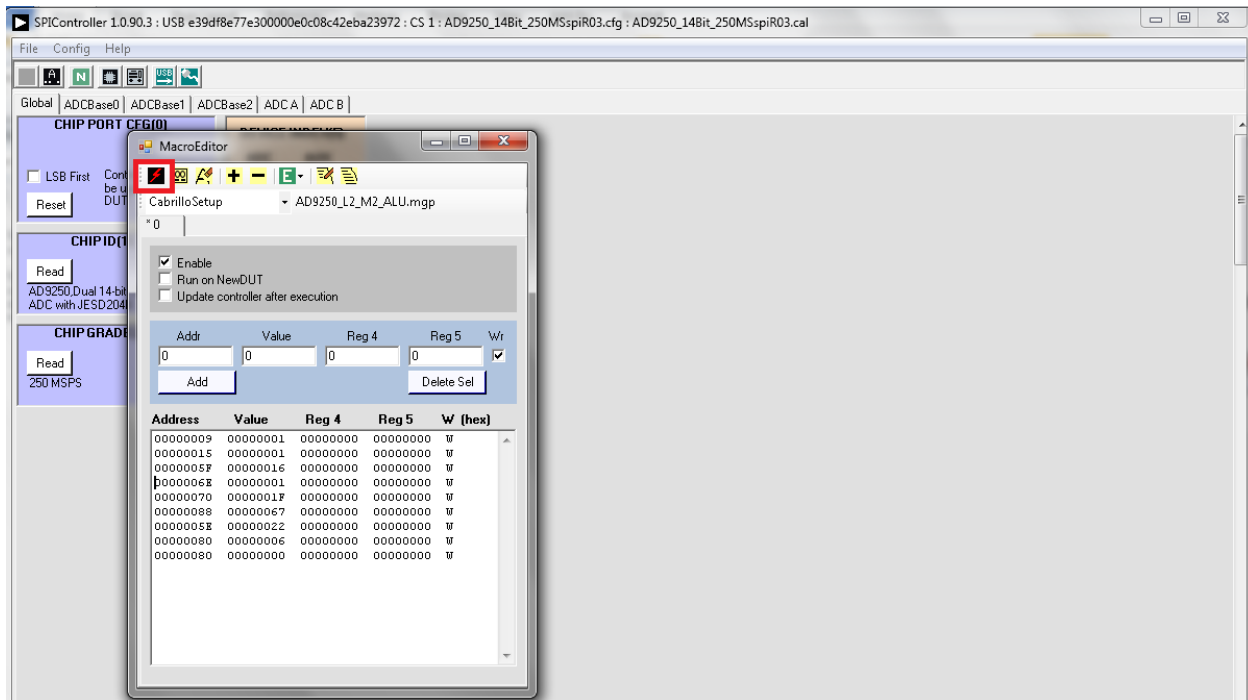


Figure 7. SPIController Software, Run Macro

17. Before running the macro, unplug the power connector to the [AD9250](#) or the [AD6673](#) evaluation board and reconnect it.
18. Click **Run Macro** to configure the [AD9250](#) or the [AD6673](#) (see highlighted red in Figure 7).
19. Click **Run** (🎮) in the **VisualAnalog** software.
20. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the **Fund** **Power** reading in the left panel of the **VisualAnalog FFT** window.)
21. If desired, click **File > Save Form as** in the FFT window to save the FFT plot

TROUBLESHOOTING

Four troubleshooting issues include the following:

- FFT plot appears abnormal
- FFT plot appears normal, but the performance is poor
- FFT window remains blank after clicking **Run**
- VisualAnalog indicates **FIFO capture timed out**

FFT Plot Appears Abnormal

Take the following steps if the FFT plot appears abnormal:

- If a normal noise floor is seen when the signal generator is disconnected from the analog input, ensure that the ADC is not being overdriven. Reduce input level, if necessary.
- In **VisualAnalog**, click **Settings** in the **Input Formatter** block. Ensure that **Number Format** is set to the correct encoding (twos complement by default).

FFT Plot Appears Normal, but the Performance Is Poor

Take the following steps if the FFT plot appears normal but the performance is poor:

- Ensure that the appropriate filter is being used on the analog input.
- Ensure that the signal generators for the clock and the analog input are clean (low phase noise).
- If noncoherent sampling is being used, change the analog input frequency slightly.
- Ensure that the SPI configuration file matches the product being evaluated.

FFT Window Remains Blank After Run Is Clicked

Take the following steps if the FFT window remains blank after **Run** is clicked:

- Ensure that the [AD9250](#) or the [AD6673](#) evaluation board is securely connected to the [HSC-ADC-EVALDZ](#) board.
- Disconnect power from both the [AD9250](#) or the [AD6673](#) evaluation board and the [HSC-ADC-EVALDZ](#) board, disconnect the USB cable from the [HSC-ADC-EVALDZ](#) board, and begin again at Step 1.
- Ensure that the FPGA has been programmed by verifying that the **CONFIG_DONE** LED is illuminated on the [HSC-ADC-EVALDZ](#) board.
- Ensure that the correct FPGA program was installed.

VisualAnalog Indicates FIFO Capture Timed Out

Take the following steps if the VisualAnalog indicates that the **FIFO Capture Timed Out**:

- Ensure that all power and USB connections are secure.
- Confirm that the encode clock source is present at Connector J505.

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.