ANALOG DEVICES

Evaluation Board User Guide

UG-070

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Setting Up the Evaluation Board for the ADCLK854

PACKAGE LIST

Evaluation board with components installed
Applicable documents (schematic and layout)

GENERAL DESCRIPTION

This user guide describes how to set up and use the evaluation board for the ADCLK854. The ADCLK854 data sheet contains full technical details about the specifications and operation of this device and should be consulted when using the evaluation board.

The ADCLK854 is a high performance clock fanout buffer. The evaluation board is fabricated using a high quality Rogers® dielectric material. Transmission line paths are kept as close to 100 Ω differentially as possible.

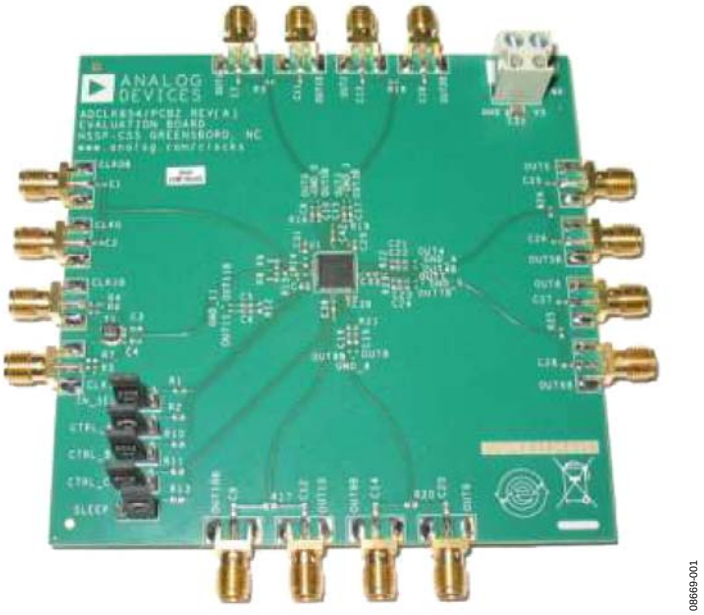

Figure 1. Evaluation Board

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REVISION HISTORY

12/09—Revision 0: Initial Version

RECOMMENDED BOARD SETUP

The recommended setup for the ADCLK854 evaluation board is shown in Figure 2. V_S is set to 1.8 V. The IN_SEL jumper provides the desired input configuration. Logic 0 on the IN_SEL pin selects the CLK0 and $\overline{\text{CLK0}}$ inputs, and Logic 1 on the IN_SEL pin selects the CLK1 and $\overline{\text{CLK1}}$ inputs.

On the evaluation board, the CLK0 and $\overline{\text{CLK0}}$ inputs are set up for ac-coupled, differential operation to the ADCLK854. This input configuration requires the user to provide the appropriate ac swing to both inputs. Refer to the ADCLK854 data sheet and the schematic (see Figure 4) for the input specifications.

CLK1 is set up to evaluate with a single-ended source via the balun on the evaluation board. In addition, series capacitors in the path provide ac-coupled inputs to the ADCLK854.

The range of the peak-to-peak input voltage swing at CLK1 is 0.15 V to 1.8 V. Output jitter performance is degraded by input slew rate, as shown in the ADCLK854 data sheet.

Table 1. Basic Equipment Required

Quantity	Description
1	Single power supply
1	Signal source
1	High bandwidth oscilloscope
1	High bandwidth differential probe
2	Matched high speed cables

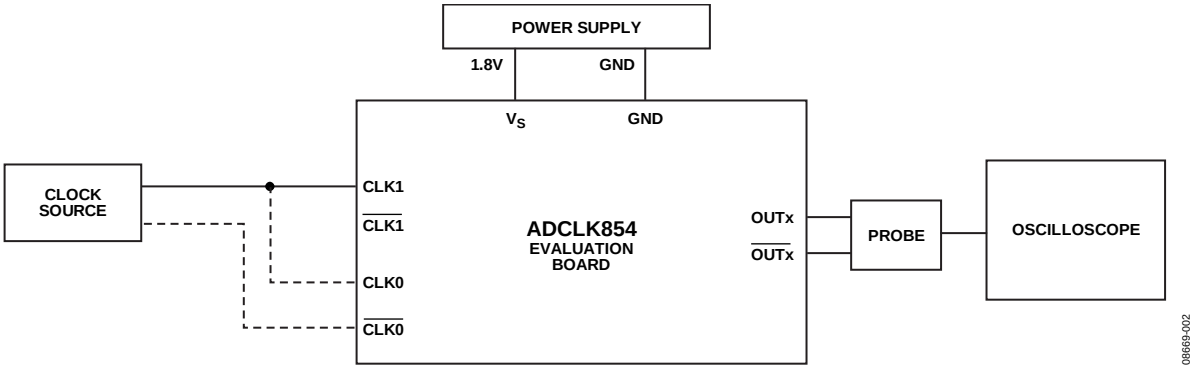

Figure 2. Recommended Setup for ADCLK854 Evaluation

CLOCK OUTPUTS

The ADCLK854 outputs are pin programmable up to 12 differential LVDS outputs or 24 single-ended 1.8 V CMOS outputs. Jumpers CTRL_A, CTRL_B, CTRL_C, and SLEEP are used to configure the outputs. See Table 2 and Figure 3 for jumper assignments.

For high precision measurements, it is recommended to evaluate the nonlaunched outputs on the evaluation board. The nonlaunched outputs do not go to the SMA connectors. In this case, the ADCLK854 is physically close to the output load and avoids the issues of driving a 50 Ω cable. Note that CMOS is not designed to operate in a 50 Ω environment.

The nonlaunched outputs have a full output swing with 100 Ω differential trace impedance into a 100 Ω resistor to minimize reflections. These outputs are set up to evaluate using a high bandwidth differential probe and oscilloscope. See the evaluation board schematic in Figure 4 for more details.

The outputs that go to the SMA connector may not have a full output swing, and reflections may be observed.

Table 2. Output Pin Assignment

Jumper Name	Jumper Setting	Affected Outputs
CTRL_A	Logic 0 = LVDS; Logic 1 = CMOS	Output 0 to Output 3
CTRL_B	Logic 0 = LVDS; Logic 1 = CMOS	Output 4 to Output 7
CTRL_C	Logic 0 = LVDS; Logic 1 = CMOS	Output 8 to Output 11
SLEEP	Logic 1 = sleep	Output 0 to Output 11

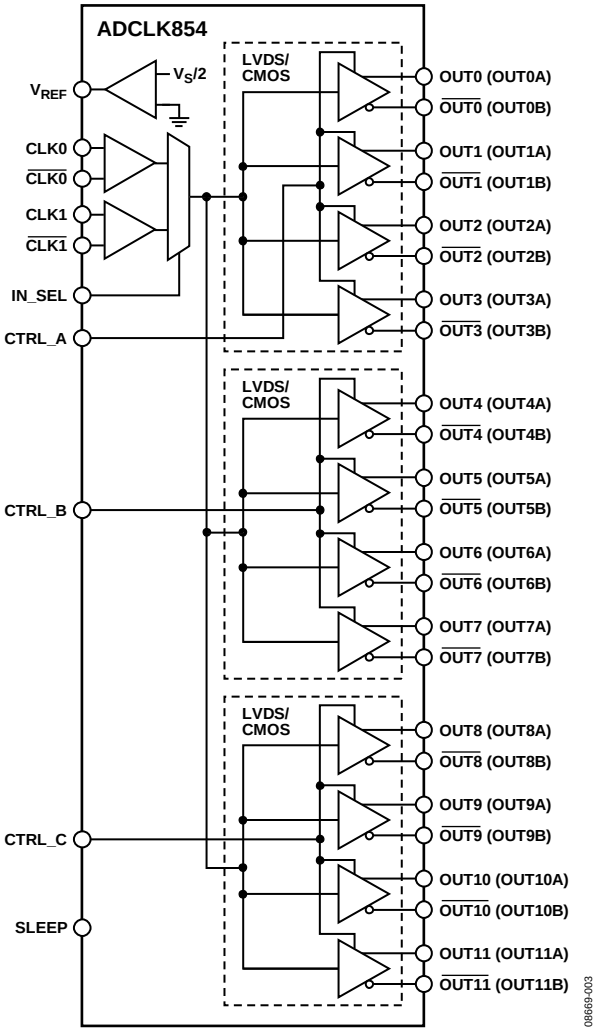

Figure 3. 1:12 Clock/Data Buffer Block Diagram

EVALUATION BOARD SCHEMATIC AND ARTWORK

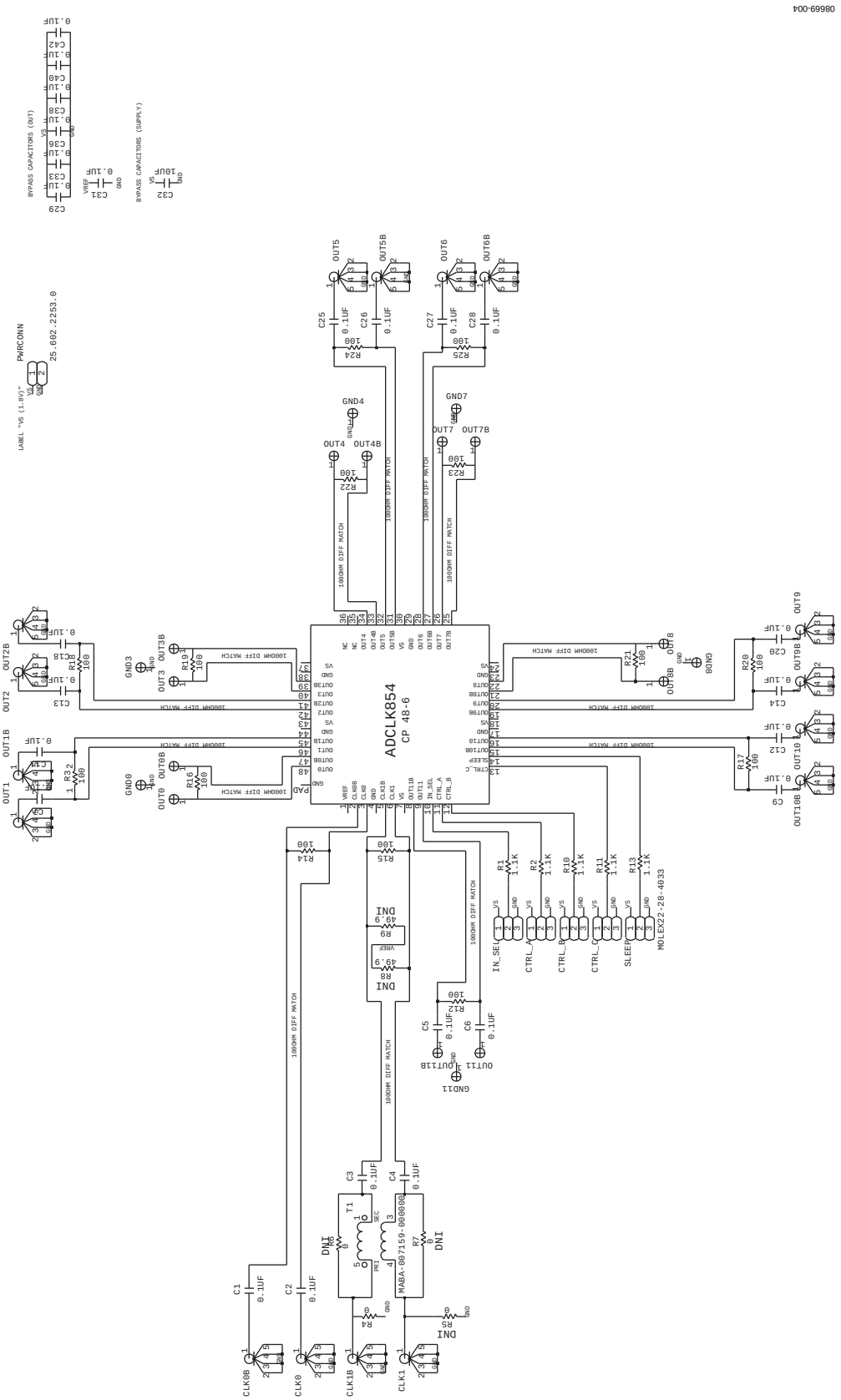

Figure 4. ADCLK854 Evaluation Board Schematic

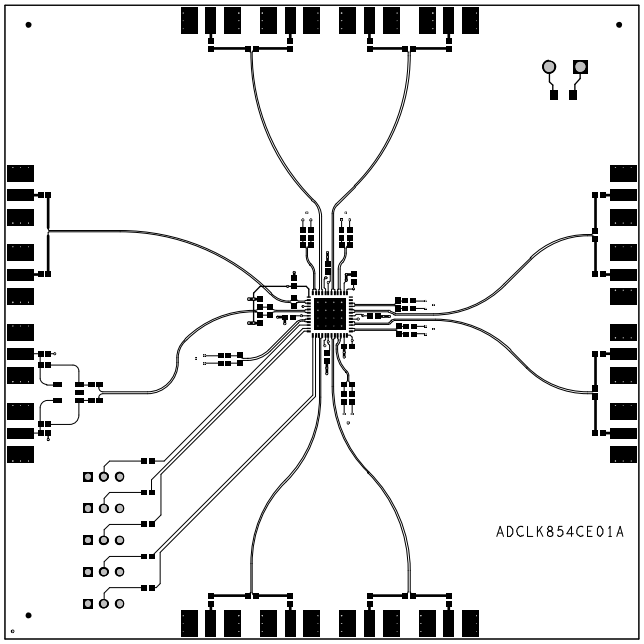

Figure 5. Top Trace Layer

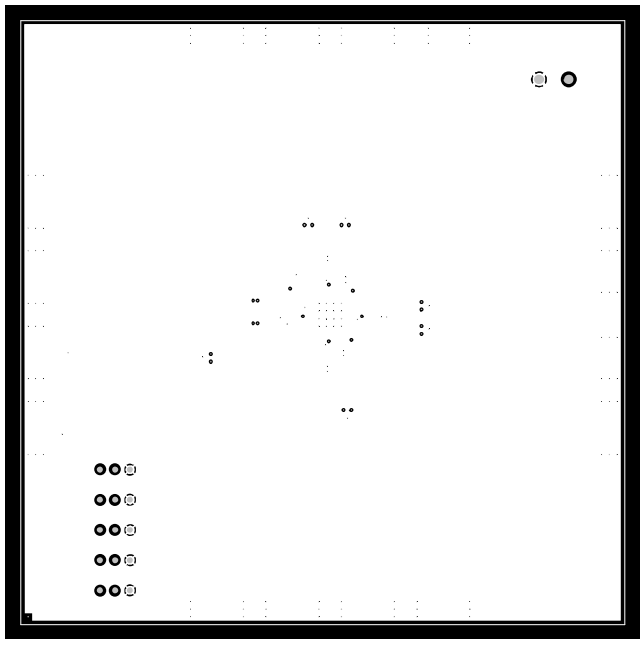

Figure 6. Ground Plane Layer

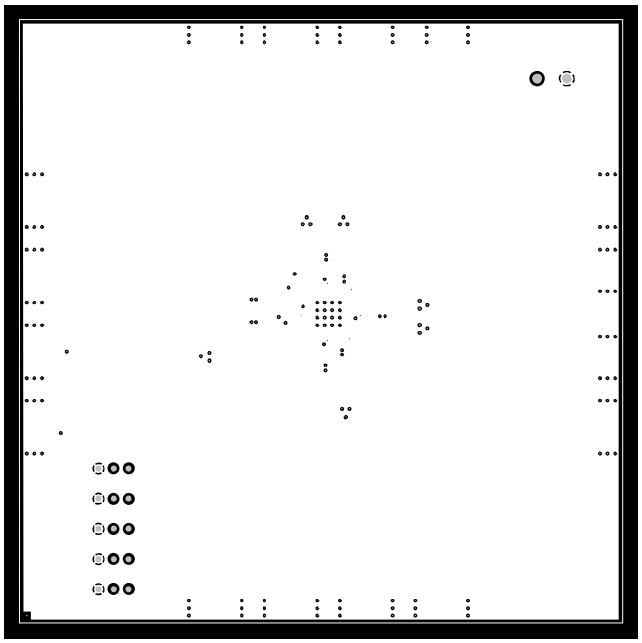

Figure 7. V_S Power Plane Layer

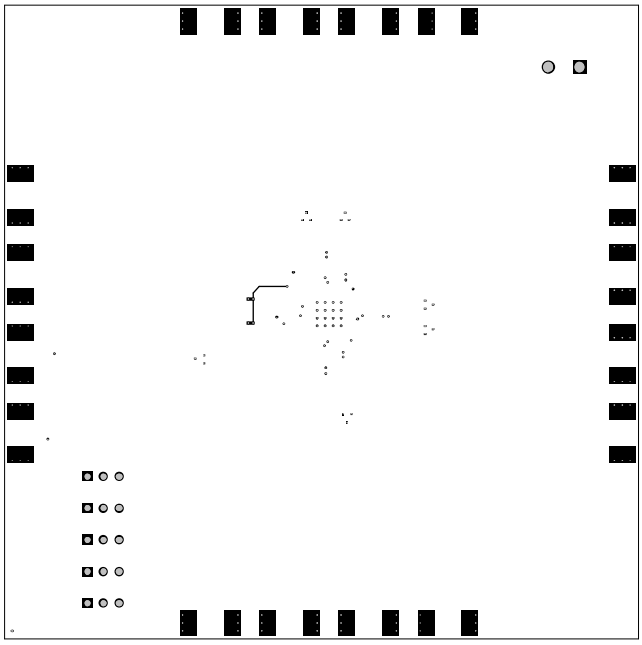

Figure 8. Bottom Trace Layer

NOTES

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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