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Evaluation Board for the AD7291
8-Channel, I²C, 12-Bit SAR ADC with Temperature Sensor

FEATURES

Full-featured evaluation board for the AD7291
Link options
On-board analog bias-up circuit
PC control in conjunction with system demonstration platform (SDP)
PC software for control

EVALUATION BOARD DESCRIPTION

The EVAL-AD7291SDZ is a full-featured evaluation board, designed to allow the user to easily evaluate all features of the AD7291. The evaluation board can be controlled via the system demonstration platform (SDP) connector (J1). The SDP board allows the evaluation board to be controlled through the USB port of a PC using the AD7291 evaluation software.

On-board components include the ADP1706 low dropout CMOS linear regulator; the AD8022 high speed, low noise amp; and the AD8066 high performance 145 MHz FastFET™ amp.

The evaluation board features analog bias-up circuitry. Bipolar signals are input via the VIN SMB connector and are biased up by the on-board bias-up buffer circuit. The biased up signal is available at the BIASED_VIN2 SMB and can be applied to any one of the eight VINx SMB connectors using an SMB-SMB cable.

Various link options are described in the Evaluation Board Hardware section. The Link Options section of this user guide should be consulted when configuring the board for standalone operation.

DEVICE DESCRIPTION

The AD7291 is a 12-bit, 8-channel successive approximation ADC with an internal temperature sensor. The part operates from a single 3.3 V power supply and features an I²C®-compatible interface. Each AD7291 provides a 2-wire serial interface compatible with I²C interfaces.

The AD7291 offers a programmable sequencer, which enables the selection of a preprogrammable sequence of channels for conversion. The device has an on-chip 2.5 V reference that can be disabled to allow the use of an external reference.

The AD7291 includes a high accuracy band-gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C.

Complete specifications for the AD7291 are provided in the AD7291 data sheet, available from Analog Devices, Inc., which should be consulted in conjunction with this data sheet when using the evaluation board.

FUNCTIONAL BLOCK DIAGRAM

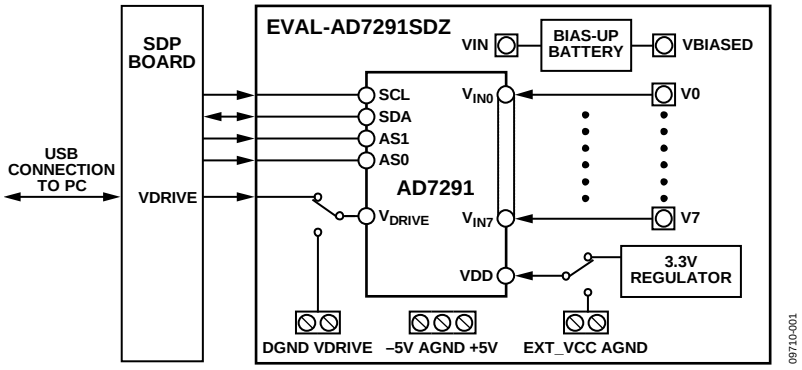

Figure 1.

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3/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode.

When using this evaluation board with the SDP board, apply +5 V, −5 V, and GND to Connector J2. V_{DRIVE} is supplied by the SDP board, and V_{DD} is supplied by an on-board regulator. Each supply is decoupled on the EVAL-AD7291SDZ using 10 µF and 0.1 µF capacitors. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

LINK OPTIONS

Table 1 shows the position in which all the links are set when the evaluation board is packaged. The links are set so that control signals and V_{DRIVE} are supplied by the SDP board.

Multiple link (LKx) and solder link (SLx) options must be set correctly to select the appropriate operating setup before using the evaluation board. The default link positions are shown in Table 1 and the functions of these options are outlined in Table 2.

Table 1. Link Options

Link No.	Position	Function
LK1	Inserted	This link option pulls the AD7291 V_{IN0} input to GND via a 10 kΩ resistor.
LK2	Inserted	This link option pulls the AD7291 V_{IN1} input to GND via a 10 kΩ resistor.
LK3	Inserted	This link option pulls the AD7291 V_{IN6} input to GND via a 10 kΩ resistor.
LK4	Inserted	This link option pulls the AD7291 V_{IN7} input to GND via a 10 kΩ resistor.
LK5	Position A	Connects the $\overline{PD}/\overline{RST}$ pin to V_{DRIVE} voltage.
LK6	Position A	When in Position A, the 3.3 V V_{CC} supply is supplied by the on-board regulator, ADP1706.
LK7	Position A	When in Position A, the V_{DRIVE} supply is taken from the SDP board via VIO_CONNECTOR.
LK8	Inserted	When inserted, the V_{REF} signal is connected to the V_{REF} test point.
LK9	Inserted	When inserted, the buffered internal reference voltage is divided by a factor of 3 and used as the bias input for U10.
LK10	Inserted	This link option pulls the AD7291 V_{IN2} input to GND via a 10 kΩ resistor.
LK11	Inserted	This link option pulls the AD7291 V_{IN3} input to GND via a 10 kΩ resistor.
LK12	Inserted	This link option pulls the AD7291 V_{IN4} input to GND via a 10 kΩ resistor.
LK13	Inserted	This link option pulls the AD7291 V_{IN5} input to GND via a 10 kΩ resistor.
LK14	Inserted	This link option connects +5 V to Pin 1 of J1.
LK20	Position A	In Position A, the buffered internal reference is used as the bias input for U10.
SL1	Position B	Buffered output from SMA Connector V7 is routed to SMB Connector BUFF_V7.
SL2	Position A	In Position A, there is no amplifier included in the Analog Input Channel V_{IN1} path.
SL3	Position B	Buffered output from SMA Connector V0 is routed to SMB Connector BUFF_V0.
SL4	Position B	In Position B, there is an amplifier included on the Analog Input Channel V_{IN0} path.

SOCKETS/CONNECTORS

There are 16 SMB input sockets relevant to the operation of the AD7291 on this evaluation board. The functions of these sockets are outlined in Table 2.

Table 2. Socket/Connector Functions

Socket	Function
BIASED_VIN2	SMB socket for the output of the bias up circuit
BUFF_V0	SMB socket for the buffered V0 input (SL3 must be in Position A and SL4 must be in Position B)
BUFF_V7	SMB socket for the buffered V7 input (SL1 must be in Position A)
EXT_OFFSET	SMB socket for an external bias input, which is applied to U10
J3	V0 SMB socket for a single-ended input that is applied to the V_{IN0} pin of the AD7291
J4	V1 SMB socket for a single-ended input that is applied to the V_{IN1} pin of the AD7291
J5	V6 SMB socket for a single-ended input that is applied to the V_{IN6} pin of the AD7291
J6	V7 SMB socket for a single-ended input that is applied to the V_{IN7} pin of the AD7291
J8	V2 SMB socket for a single-ended input that is applied to the V_{IN2} pin of the AD7291
J9	V3 SMB socket for a single-ended input that is applied to the V_{IN3} pin of the AD7291
J10	V4 SMB socket for a single-ended input that is applied to the V_{IN4} pin of the AD7291
J11	V5 SMB socket for a single-ended input that is applied to the V_{IN5} pin of the AD7291
J12	SMB socket connected to the V_{REF} pin of the AD7291 (by default the internal reference is used)
J13	SMB socket connected to the $\overline{PD}/\overline{RST}$ pin of the AD7291
VIN	SMB socket to connect input to the bias-up circuit
VREF_BUFF	SMB socket for the output of the buffered reference

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The AD7291 evaluation kit includes self-installing software on a CD. The software is compatible with Windows® XP (SP2) and Windows Vista® (32-bit). If the setup file does not run automatically, you can run **setup.exe** from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

1. After installation from the CD is complete, power up the AD7291 evaluation board as described in the Power Supplies section. Connect the SDP board (Connector A) to the AD7291 evaluation board (Connector J1) and then to the USB port of your PC using the supplied cable.
2. When the evaluation system is detected, proceed through any dialog boxes that appear. This completes the installation.

SOFTWARE OPERATION

To launch the software, complete the following steps:

1. From the **Start** menu, select **Analog Devices** – AD7291 > AD7291 **Evaluation Software.** The main window of the software is displayed (see Figure 3).
2. If the evaluation system is not connected to the USB port when the software is launched, a connectivity error is displayed (see Figure 2). Connect the evaluation board to the USB port of the PC, wait a number of seconds, and click **Rescan.** Follow the instructions.

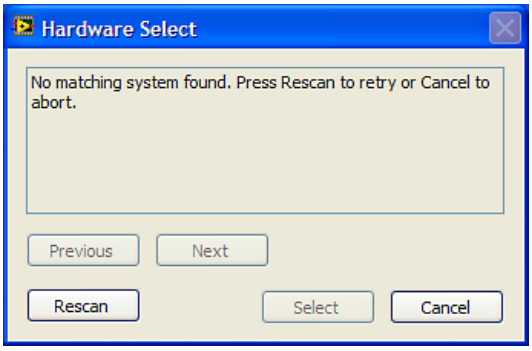

Figure 2. Connectivity Error Alert

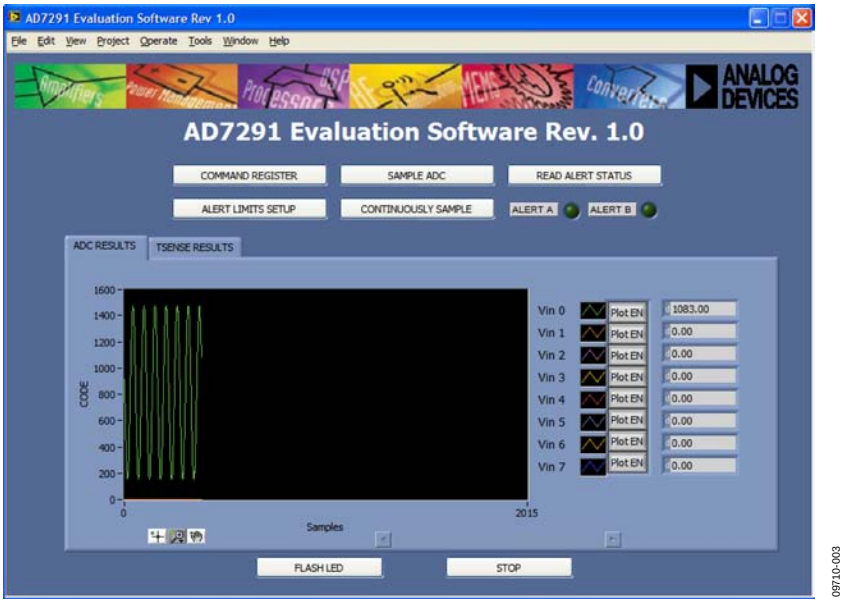

Figure 3. Main Window

MAIN WINDOW

Figure 4 shows the main window of the AD7291 evaluation software. The device is configured via the **COMMAND REGISTER** button.

Samples can be taken continuously or one at a time, depending on whether **CONTINUOUSLY SAMPLE** or **SAMPLE ADC** is selected.

The AD7291 has nine pairs of limit registers. Each pair stores high and low conversion limits for each analog input channel and the internal temperature sensor, which can be programmed via the **ALERT LIMITS SETUP** button. If a limit is violated, the ALERT A or ALERT B indicator turns red. Further details on the alert limits can be ascertained at any time by clicking **READ ALERT STATUS**.

The lower section of the window graphically displays AD7291 data. The tab setting in the data display window allows the user to swap between displaying the ADC analog input channel conversion results and the internal temperature sensor results. Figure 4 depicts continuous analog input channel conversion results for V_{IN0}. Figure 4 shows the main panel with the TSENSE RESULTS tab selected.

Enabling the **FLASH LED** button on this window causes the orange LED1A on the SDP board to flash, which is a useful debug tool.

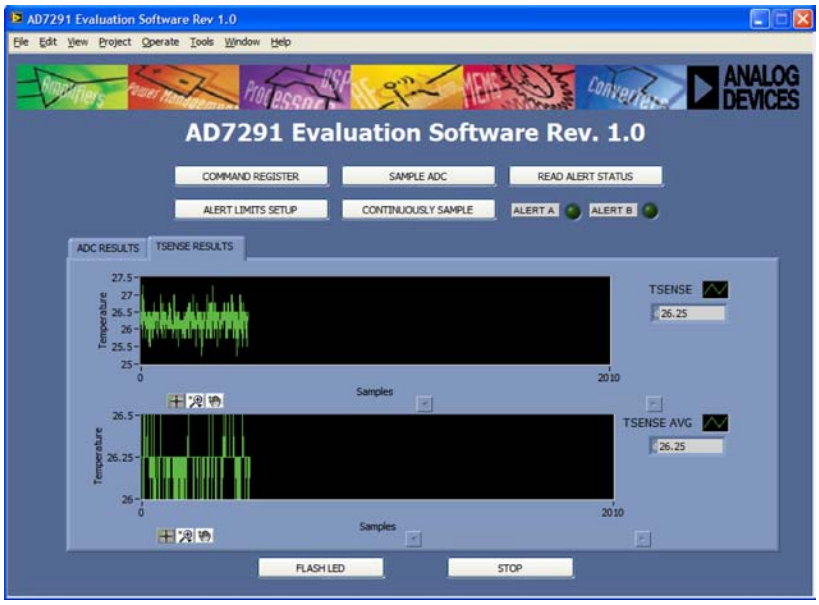

Figure 4. AD7291 Main Window Displaying TSENSE and TSENSE Average Results

COMMAND REGISTER

The Command Register section of the AD7291 data sheet should be consulted before configuring the control register settings. To configure the command register, click **COMMAND REGISTER** (see Figure 4).

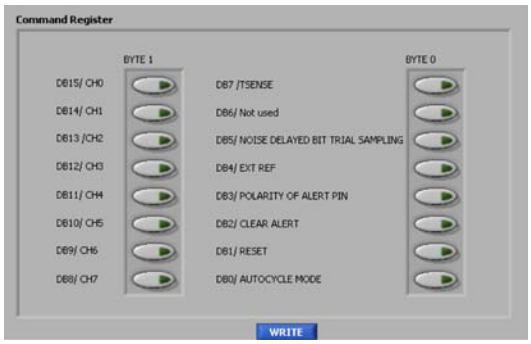

Figure 5. Command Register

Select the ADC channels required for conversion in the sequence. To enable the internal temperature sensor, select **DB7/TSENSE**.

When **DB5/NOISE DELAYED BIT TRIAL SAMPLING** is enabled, critical sampling intervals and bit trials are delayed when there is activity on the I^2C bus, thus ensuring improved dc performance of the AD7291.

The active polarity of the ALERT pin is configured as active low if the **DB3/POLARITY OF ALERT PIN** is enabled. Conversely, it is set to active high operation if this bit is disabled.

DB2/CLEAR ALERT clears the content of the alert status register. Once the content of the alert status register is cleared, this bit should be reprogrammed to Logic 0 to ensure future alerts are detected.

Enabling the DB1/RESET bit in the command register resets the content of all internal registers in the AD7291 to their default values, including the command register itself. Disable this bit once the reset is complete to allow the internal registers to be reprogrammed.

The **DB0/AUTOCYCLE MODE** enables autocycle mode. In autocycle mode, the AD7291 is configured to convert continuously on the selected sequence of channels (both analog input channels and the temperature sensor channel), making it the ideal mode of operation for system monitoring. While in this mode, the conversion results from the analog input channels are not displayed on the user interface.

Click **WRITE** to update the control register.

ALERT LIMITS

The AD7291 has nine pairs of limit registers. Each pair stores high and low conversion limits for each analog input channel and the internal temperature sensor. Each pair of limit registers has one associated hysteresis register. To program the alert limits and associated hysteresis register, click **ALERT LIMITS SETUP** on the main window.

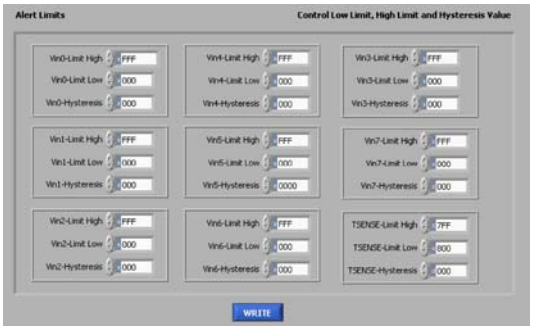

Figure 6. Alert Limits Setup

The AD7291 signals an alert in hardware if the conversion result moves outside the upper or lower limit set by the limit registers. **ALERTA** and **ALERTB** indicators on the main window turn red if a limit is violated, as shown in Figure 7. Alert Register A stores alerts for the analog voltage conversion channels, and Alert Register B stores alerts for the internal temperature sensor.

For further information on the status of the alerts, click **READ ALERT STATUS** on the front panel. For example, Figure 8 depicts an example where the V_{IN0} low limit, TSENSE AVG high limit, and TSENSE high limit have been violated.

SAMPLE ADC/CONTINUOUSLY SAMPLE

To gather sample data on the selected channels, click SAMPLE ADC or CONTINUOUSLY SAMPLE. Both buttons are located on the upper middle area of the main window. To stop sampling, click CONTINOUSLY SAMPLE a second time.

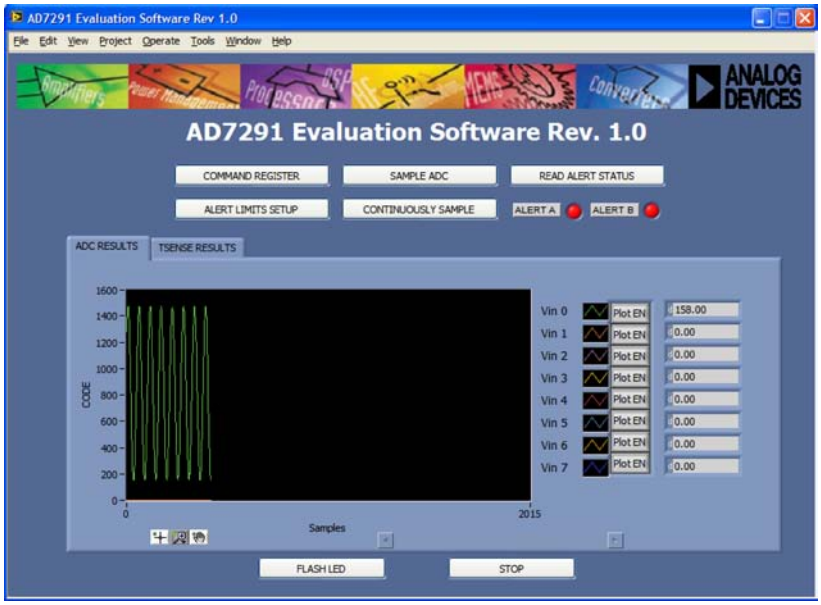

Figure 7. AD7291 Main Window Showing Triggered ALERT A and ALERT B Indicators

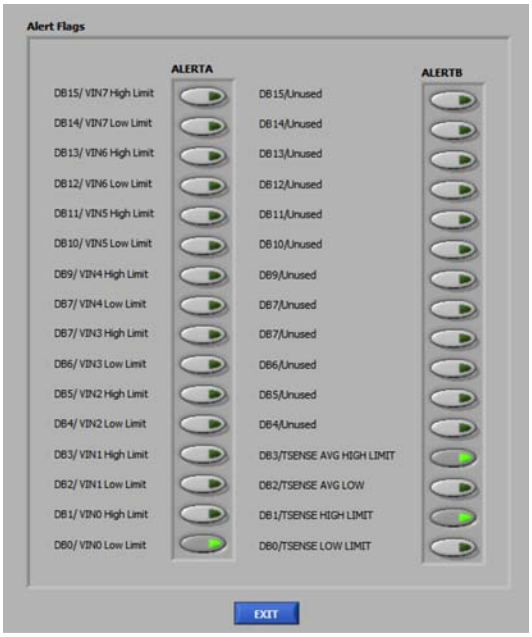

Figure 8. Read Alert Status

EVALUATION BOARD SCHEMATICS AND ARTWORK

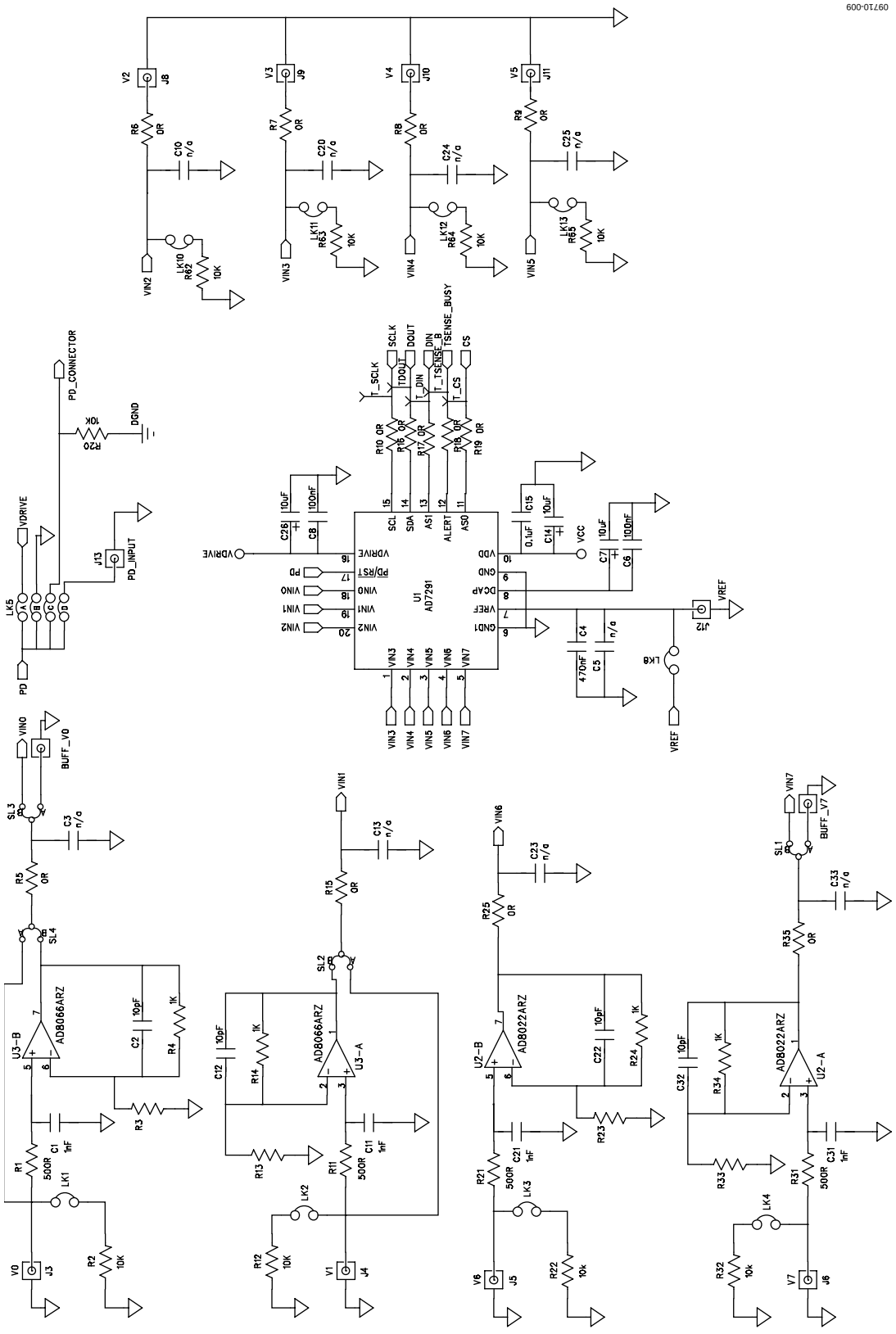

Figure 9. EVAL-AD7291SDZ Schematic 1 of 3

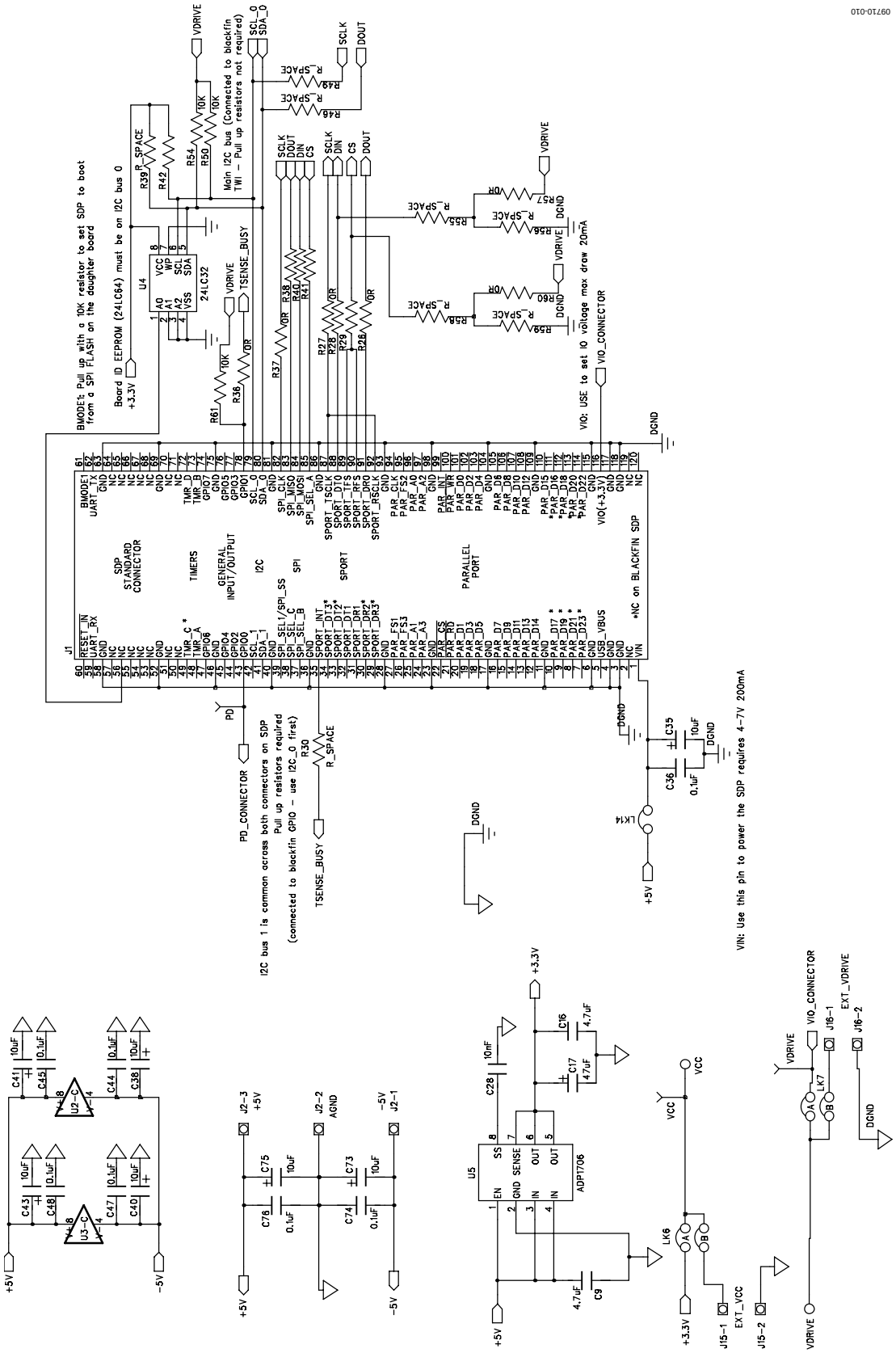

Figure 10. EVAL-AD7291SDZ Schematic 2 of 3

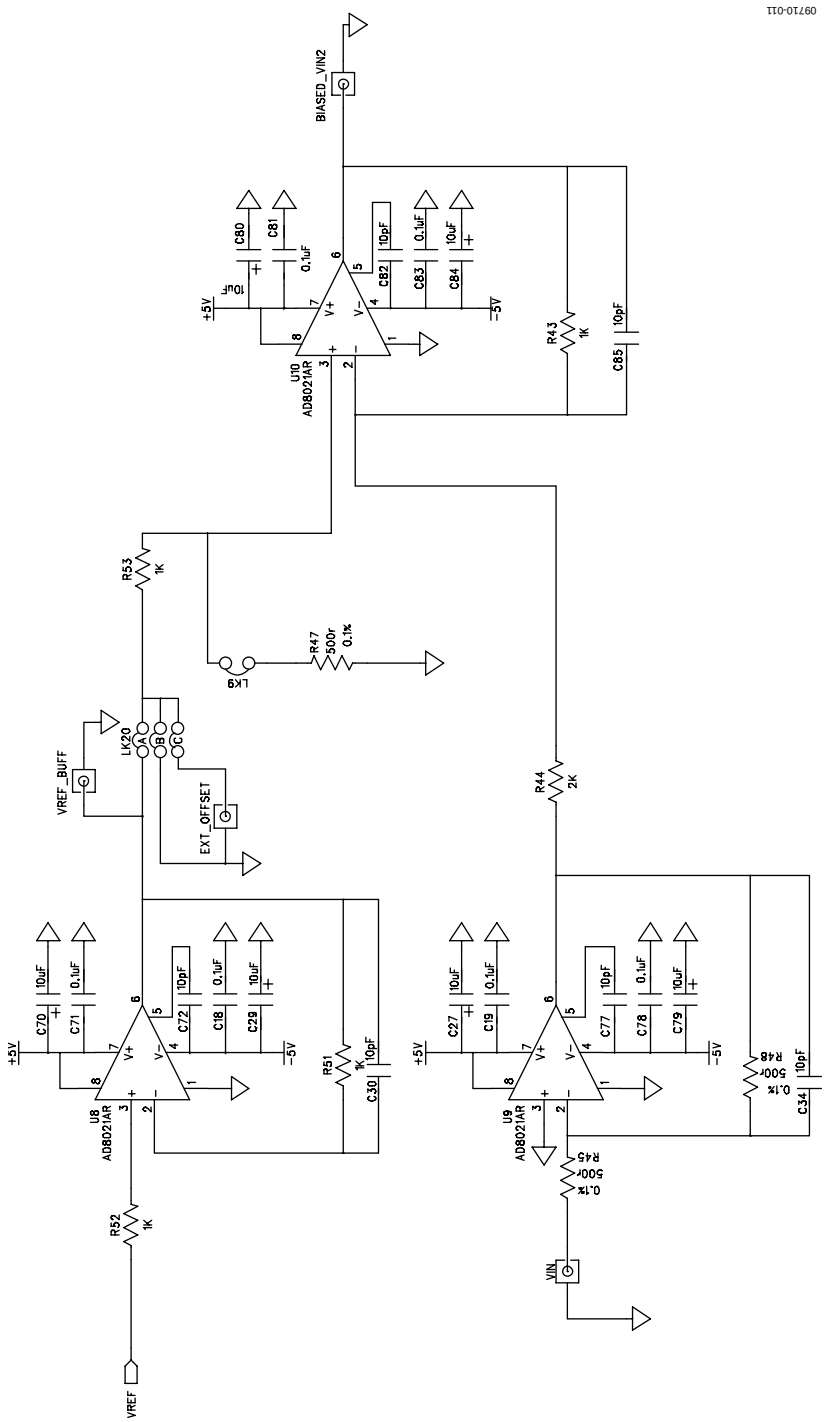

Figure 11. EVAL-AD7291SDZ Schematic 3 of 3

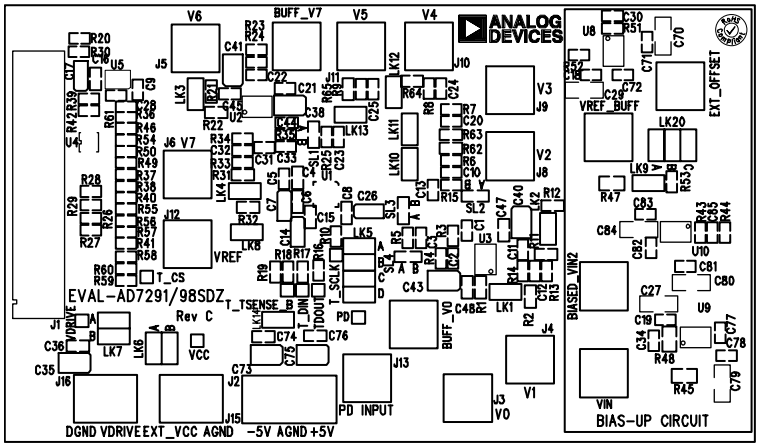

Figure 12. Component Side Artwork

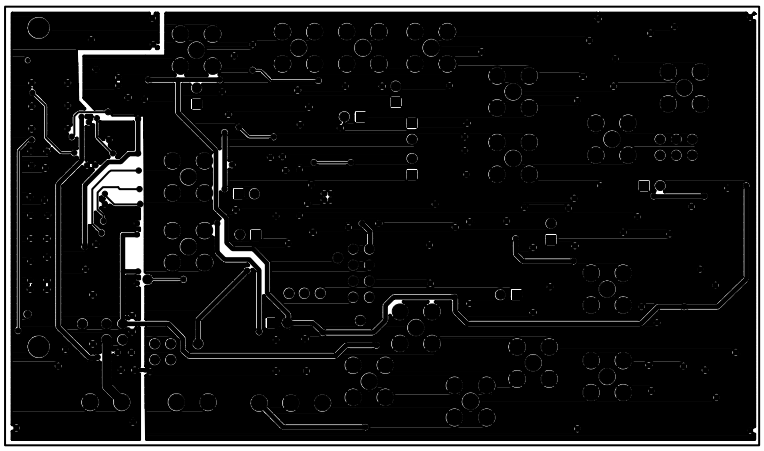

Figure 12. Solder Side Artwork

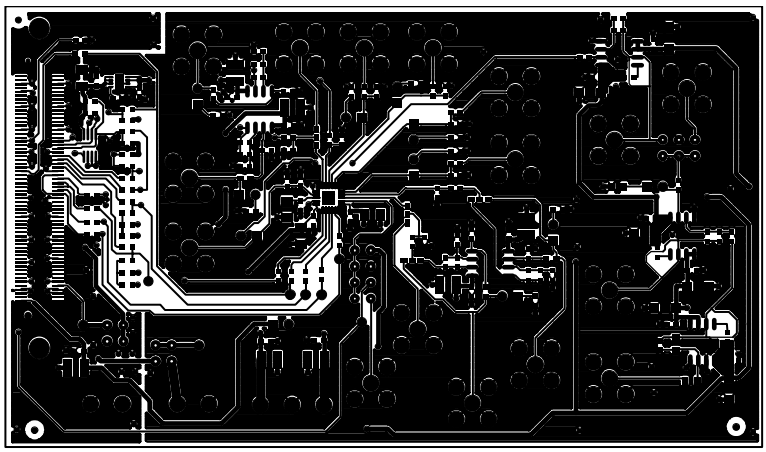

Figure 13. Component Side Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Part Type	Value	Tolerance	Part Description	Part Number	Stock Code
C1, C11, C21, C31	Capacitor	1 nF	0.1	50 V X7R multilayer ceramic capacitor	U0603R102KCT	FEC 9406174
C2, C12, C22, C30, C32, C34, C72, C77,C82, C 85,	Capacitor	10 pF	0.05	50 V NPO multilayer ceramic capacitor	06035A100JAT2A	FEC 499110
C3, C5, C7, C10, C13, C20, C23, C24, C25, C33	Not inserted	N/A	N/A	0603 capacitor spacing	N/A	N/A
C4	Capacitor	10 µF	0.2	6.3 V X5R ceramic capacitor	C0603C106M9PACTU	FEC 1288201
C6, C8, C15, C36, C44, C45,C47, C48, C74, C76	Capacitor	100 nF	0.05	16 V X7R ceramic capacitor	0603YC104JAT2A	FEC 432210
C9, C16	Capacitor	4.7 µF	0.1	10 V X7R multilayer ceramic capacitor 603	C0603C475K8PAC 7867	FEC 1572625
C14, C26	Capacitor	10 µF	0.1	10 V SMD tantalum capacitor	TAJA106K010R	FEC 197130
C17	Capacitor	47 µF	0.2	SMD tantalum capacitor	TAKA106010R	FEC 1658411
C18, C19, C71, C78, C81, C83	Capacitor	0.1 µF	0.1	16 V X7R multilayer ceramic capacitor	B0603R104KCT	FEC 9406140
C27, C29, C70, C79, C80, C84	Capacitor	10 µF	0.2	16 V X5R multilayer ceramic capacitor 1206	ECJ-HVB1C106M	Digi-Key PCC2417CT-ND
C28	Capacitor	10 nF	0.1	50 V NPO multilayer ceramic capacitor	06035C103KAZ2A	FEC 7569548
C35, C38, C40, C41,C43,C73,C75	Capacitor	10 µF	0.1	16 V SMD tantalum capacitor	AVX TAJB106K016R	FEC 498737
J1	CON-120/ FX8-120S-SV			120-way connector, 0.6 mm pitch	FX8-120S-SV(21)	FEC 1324660
J2	CON/POWER3			3-pin terminal block, 5 mm pitch	CTB5000/3	FEC 151790
J3 to J6,J8 to J13, BUFF_V0, BUFF_V7	SMB			50 W gold plated PCB SMB jack	1-1337482-0	FEC 1206013
J15, J16	CON/POWER			2-pin terminal block, 5 mm pitch	CTB5000/2	FEC 151789
LK1 to LK4, LK8 TO LK14	Jumper			2-pin header and shorting shunt	M20-9990206	FEC 1022247 and 150411
LK5	Jumper			8-pin (4x2) header and shorting shunt	M20-9990206	FEC 1022231 & 150411
LK6, LK7	Jumper			4-pin (2x2) header and shorting shunt	M20-9990206	FEC 1022233 & 150411
LK20	Jumper			6-pin (3x2) header and shorting shunt	M20-9983646	FEC 1022244 % 150411
R1, R11, R21, R31	Resistor	500 Ω	0.01	0603 SMD resistor	MC0.063W06031%499R	FEC 1170758
R2, R12, R20, R22, R32, R50, R54, R61, R62, R63, R64, R65	Resistor	10 kΩ	0.01	0603 SMD resistor	MC0.063W06031%10K	FEC 9330399
R3, R13, R23, R26 to R29, R30, R33, R37, R38, R39, R40, R41, R42, R55, R56, R58, R59	Not inserted	N/A	N/A	0603 resistor space	N/A	N/A
R4, R14, R24, R34, R43, R51, R52, R53	Resistor	1 kΩ	0.01	0603 SMD resistor	MC0.063W06031%1K	FEC 9330380

Reference Designator	Part Type	Value	Tolerance	Part Description	Part Number	Stock Code
R5 to R10, R15 to R19, R25, R35, R36, R46, R49, R57, R60	Resistor	0 Ω	0.01	0603 SMD resistor	MC0.063W06030R	FEC 9331662
R44	Resistor	2k	0.01	0603 SMD resistor	MC0.063W06031%2K	FEC 9330763
R45, R47, R48	Resistor	500 Ω	0.001	0805 SMD resistor	CRCW0805499RFKEA	FEC 1152405
SL1 to SL4	Solder link			two-way solder bridge	N/A	N/A
U1	AD7291			Main device	AD7291BCPZ	AD7291BCPZ
U2	AD8022			Dual op amp	AD8022ARZ	AD8022ARZ
U3	AD8066			Dual op amp	AD8066ARZ	AD8066ARZ
U4	EEPROM			32 kΩ I^2C serial EEPROM	24LC32A-1/MS	FEC 1331330
U5	ADP1706			Linear regulator	ADP1706ACPZ-3.3V-R7	ADP1706ACPZ-3.3V-R7
U8, U9, U10	AD8021			Op amp	AD8021ARZ	AD8021ARZ
T_SCLK, PD, T_CS, T_DIN, T_TENSE_B, TDOUT, VCC, VDRIVE	Test point			Black test point	20-2137	FEC 8731128
BIASED_VIN2, EXT_OFFSET, VIN, VREF_BUFF	SMB			50Ω SMB jack	SMB1251B1-3GT30G-50	FEC 1111349

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG09710-0-6/11(A)

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