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Evaluation Board for the ADuM3223/ADuM4223 *i*Coupler, 4 A, Isolated Precision Half-Bridge Drivers

FEATURES

4 A peak output current
High frequency operation: 1 MHz maximum
CMOS input logic levels
4.5 V to 18 V output drive
Supports TO-263 or TO-252 IGBT/MOSFETs
Bootstrap option

SUPPORTED *i*Coupler MODELS

ADuM3223
ADuM4223

GENERAL DESCRIPTION

The EVAL-ADuM3223AEBZ and EVAL-ADuM4223AEBZ support the ADuM3223 and ADuM4223 isolated precision half-bridge drivers, respectively. Because the evaluation boards have footprints for IGBTs and MOSFETs in TO-263 or TO-252 packages, the ADuM3223 and ADuM4223 can be evaluated with many different power devices. The evaluation boards also allow the high-side supply to be bootstrapped to the low-side supply.

The ADuM3223A model represents a superset of the ADuM3223 models because it has the lowest minimum output voltage (4.5 V). The ADuM3223B and ADuM3223C models have minimum output voltages of 7.5 V and 11.5 V, respectively. In the same way, the ADuM4223A model represents a superset of the ADuM4223 models.

Complete information about the ADuM3223 and ADuM4223 is available in the ADuM3223/ADuM4223 data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD

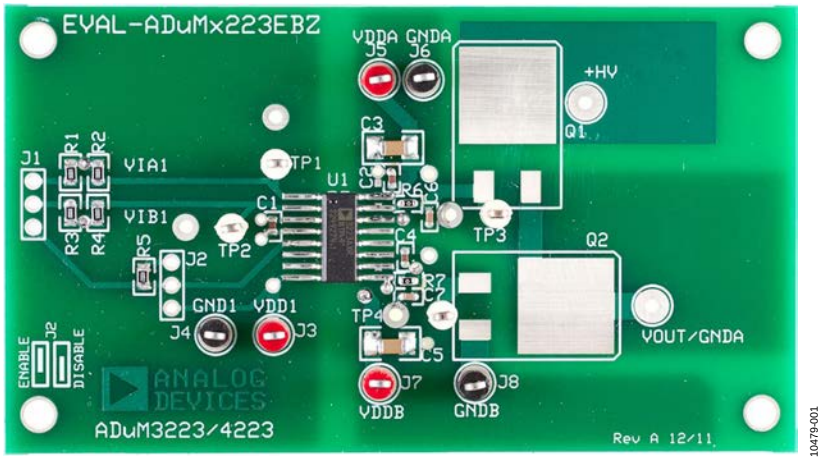

Figure 1. ADuM3223/ADuM4223 Evaluation Board

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REVISION HISTORY

5/12—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

PAD LAYOUT FOR THE DUT

Figure 5 shows the top layer artwork for the dual gate driver circuit.

- U1 is the footprint for the ADuM3223 or ADuM4223.
- C1, C2, and C4 are 0.1 µF bypass capacitors; C3 and C5 are 10 µF bypass capacitors.
- Q1 and Q2 can be populated with TO-263 or TO-252 MOSFETs or IGBTs with the pinout shown in Figure 2.
- C6 and C7 are 2.2 nF loads for the gate driver outputs. Remove C6 and C7 if MOSFETs or IGBTs are added to Q1 and Q2.

R6 and R7 are for gate resistors to control the edges of the outputs. By default, 0 Ω resistors are installed, but these resistors may need to be replaced with low value 0603 resistors if the outputs have loads lighter than 2 nF.

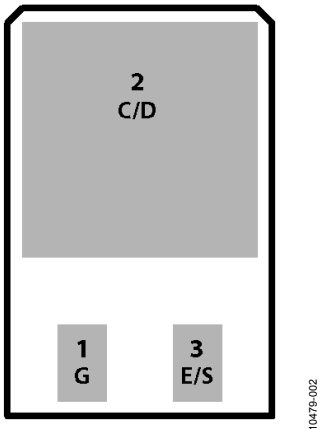

Figure 2. IGBT/MOSFET Footprint

POWER CONNECTIONS

To connect the evaluation board to the power supply, follow these steps:

1. Connect the 5 V or 3.3 V input supply to J3 and its return to J4.
2. Connect the ADuM3223/ADuM4223 V_{DDB} supply voltage (4.5 V to 18 V) to J7 and its return to J8.
3. Connect the V_{DDA} supply voltage (4.5 V to 18 V) to J5 and its return to J6.

GNDA and GNDB are functionally isolated. The emitter/source of Q1 is tied to GNDA, and the emitter/source of Q2 is tied to GNDB. GNDB also has a wire pad directly below the emitter/source pad of Q2. Connect the bridge supply to the +HV wire pad, which is connected to the collector/drain of Q1.

INPUT/OUTPUT CONNECTIONS

Connect Logic Input A (V_{IA}) to TP1 or to Pin 1 of J1; connect Logic Input B (V_{IB}) to TP2 or to Pin 2 of J1. Both inputs have 50 Ω terminations. Resistor R5 enables the outputs of the ADuM3223 or ADuM4223 by pulling the DISABLE pin low. The disable function can also be externally controlled from J1 or set by J2 (not installed).

The half-bridge output is the Q1 emitter/source and Q2 collector/drain node. A wire pad labeled VOUT/GNDA is the output of this circuit.

BOOTSTRAPPING V_{DDB} TO V_{DDA}

To bootstrap V_{DDB} to V_{DDA}, a through-hole diode can be connected from V_{DDB} to V_{DDA}, as shown in Figure 3. In this way, both outputs of the ADuM3223/ADuM4223 can be powered by the V_{DDB} supply when a half bridge is configured with Q1 and Q2.

When the switch node (GNDA) is low, C2 and C3 are charged through the forward biased bootstrapping diode. When the switch node rises to the bridge voltage, the diode becomes reverse biased, and $V_{DDA} = GNDA + V_{DDB} - GNDB$ because of the charge on C2 and C3. For bootstrapping to work, Q1 and Q2 must be populated instead of the load capacitors, C6 and C7. The switching frequency must be sufficiently high to supply C2 and C3 with the charge required to drive the Q1 gate.

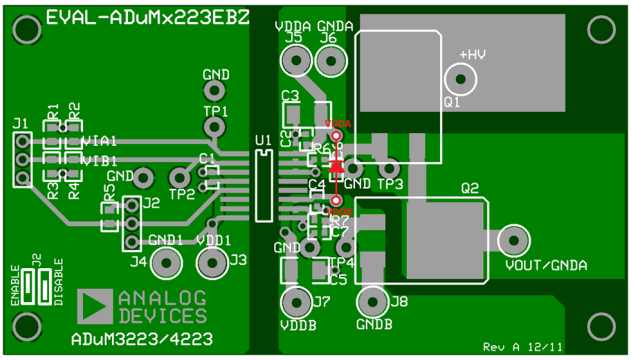

Figure 3. Bootstrapping V_{DDB} to V_{DDA}

EVALUATION BOARD SCHEMATIC

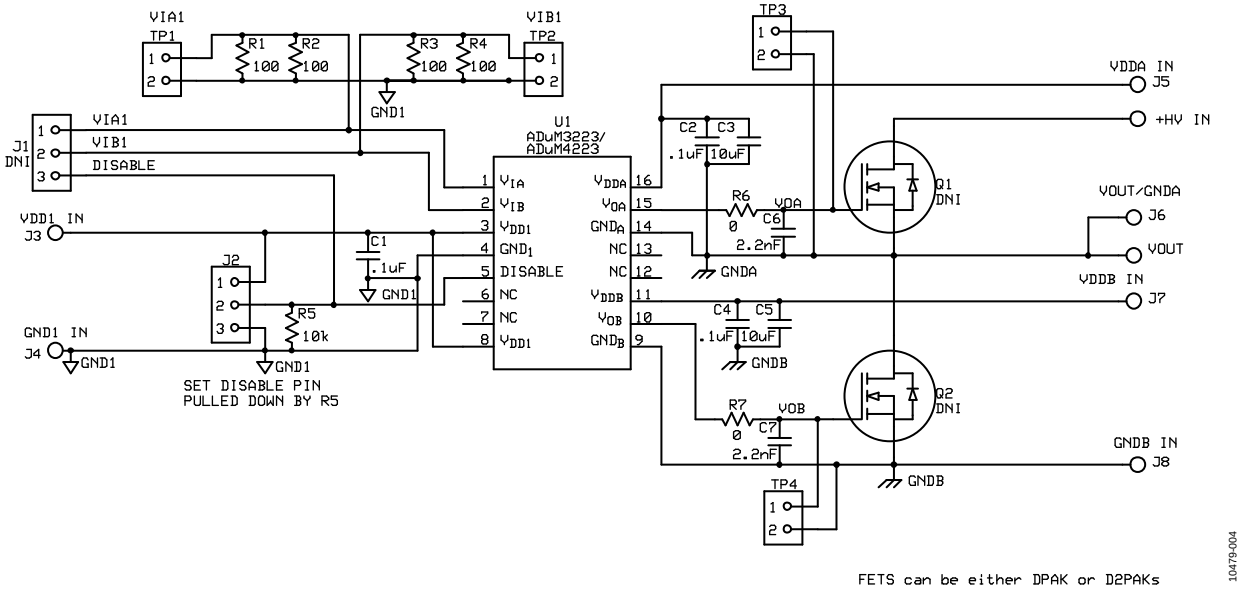

Figure 4. Half-Bridge Driver Schematic

EVALUATION BOARD LAYOUT

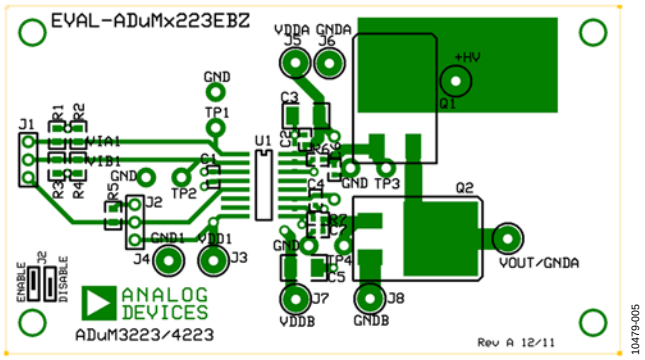

Figure 5. Top Layer

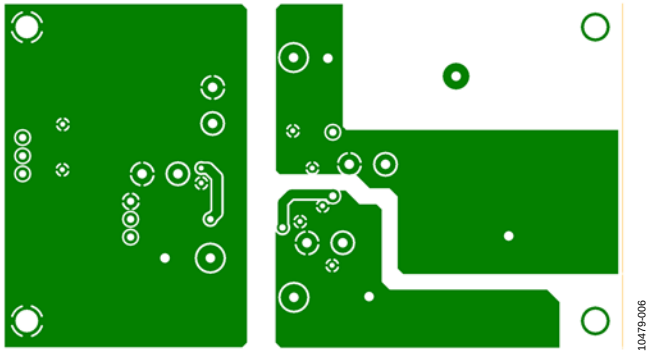

Figure 6. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description
1	U1	ADuM3223ARZ or ADuM4223ARWZ IC
3	C1, C2, C4	Capacitor, 0.1 µF, 25 V, 10%, 0603
2	C3, C5	Capacitor, 10 µF, 25 V, 10%, 1206
2	C6, C7	Capacitor, 2200 pF, 50 V, 5%, 0603
3	J3, J5, J7	Test point, TP-104 series, red
3	J4, J6, J8	Test point, TP-104 series, black
4	R1, R2, R3, R4	Resistor, 100 Ω, 1/4 W, 1%, 0805
1	R5	Resistor, 10 kΩ, 1/4 W, 1%, 0805
2	R6, R7	Resistor, 0 Ω, 1/10 W, 0603
4	TP1, TP2, TP3, TP4	Test point, TP-104 series, white
4	J1, J2, Q1, Q2	Not installed

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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