ADM1270CP-EVALZ/ ADM1270RQ-EVALZ User Guide

UG-760

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Evaluating the ADM1270 High Voltage Input Protection Device

FEATURES

Controls supply voltages from 4 V to 60 V
Gate drive for low voltage drop reverse supply protection
Gate drive for P-channel field effect transistors (FETs)
Inrush current limiting control
Adjustable current limit
Foldback current limiting
Automatic retry or latch-off on current fault
Programmable current-limit timer for safe operating area (SOA)
Power-good and fault outputs
Analog undervoltage (UV) and overvoltage (OV) protection
16-lead, 3 mm × 3 mm LFCSP
16-lead QSOP

EVALUATION KIT CONTENTS

ADM1270CP-EVALZ or ADM1270RQ-EVALZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

DC power supply
Multimeters for voltage and current measurements
Electronic or resistive loads

GENERAL DESCRIPTION

The ADM1270CP-EVALZ and ADM1270RQ-EVALZ evaluation boards are used to demonstrate the functionality of the ADM1270 high voltage input protection device.

Full specifications on the ADM1270 are available in the product data sheet, which should be consulted in conjunction with this user guide when using these evaluation boards.

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REVISION HISTORY

4/16—Rev. 0 to Rev. A

Change to Setting the Current Limit (ISET) Section 5

12/14—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

EVALUATION BOARD CONFIGURATIONS

The ADM1270CP-EVALZ and ADM1270RQ-EVALZ evaluation boards arrive supplied with different components depending on which version is ordered.

Table 1. Evaluation Board Hardware Components

Component	Function	Description
U1[1]	High voltage protection device	ADM1270CP or ADM1270RQ high voltage protection device
C1	VCAP bypass capacitor	1 µF, VCAP bypass capacitor
C2	TIMER capacitor	100 nF, C_{TIMER}, sets an SOA overcurrent (OC) fault delay, nominally 100 ms
C3	TIMER_OFF capacitor	100 nF, C_{TIMER_OFF}, sets an initial timing cycle delay and the SOA off time delay, nominally 200 ms
R1	OVLO/UVLO resistor divider	332 kΩ, sets UV threshold, nominally 8.7 V
R2	OVLO/UVLO resistor divider	33.2 kΩ, sets OV/UV thresholds with R1 and R3
R3	OVLO/UVLO resistor divider	10 kΩ, sets OV threshold, nominally 37.5 V
R4	OC current-limit threshold	100 kΩ, sets OC threshold with R5, nominally 450 mA when R6 = 100 mΩ
R5	OC current-limit threshold	100 kΩ, sets OC threshold with R4, nominally 450 mA when R6 = 100 mΩ
R6	Current sense resistor	100 mΩ, current sense resistor for OC protection
R7	OC foldback divider	4.75 kΩ, sets foldback threshold with R8, nominally 13.2 V
R8	OC foldback divider	332 kΩ, sets foldback threshold with R7, nominally 13.2 V
R9	Power-good (PG) threshold	20 kΩ, sets power-good threshold, nominally 18 V
R10	$\overline{\text{FAULT}}$ pull up	332 kΩ, $\overline{\text{FAULT}}$ pin pull up
R11	PWRGD pull up	332 kΩ, PWRGD pin pull up
R12	ENABLE pull down	332 kΩ, ENABLE pin pull down
Q1A, Q1B	Protection FET	FDS9958 dual P-channel metal-oxide semiconductor field effect transistor (MOSFET), −60 V/−2.9 A, 105 mΩ
Q2, Q4	Protection FET	DPAK FET (optional)
Q3, Q5	Protection FET	D^2PAK FET (optional)
J1	Jumper	Connects ENABLE to VIN for automatic startup
J2	Jumper	Connect this pin directly to the ENABLE pin for automatic retry after shutdown

[1] Component varies depending on the evaluation board ordered.

CONFIGURING THE ADM1270

POWERING THE ADM1270

A supply voltage from 4 V to 60 V is required to power the ADM1270 via the VCC/SENSE+ pin. The VCC/SENSE+ pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and to best regulate the gate to source voltage (V_{GS}) is supplied by the SENSE− pin.

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external current sense resistor, R_{SENSE} (see Figure 1). An internal current sense amplifier provides a gain of 40 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and is used by the hot swap control logic to detect an overcurrent condition.

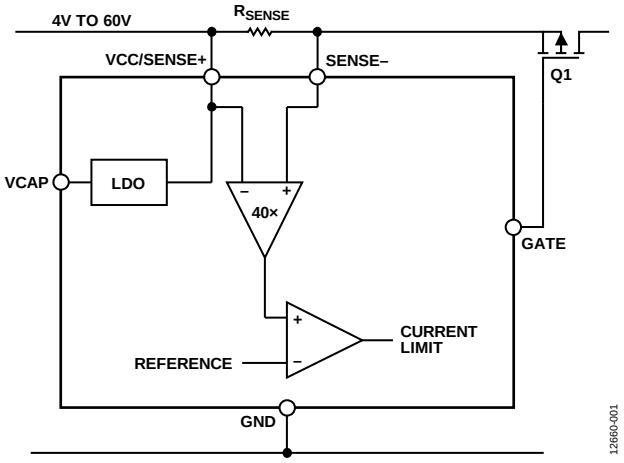

Figure 1. Hot Swap Current Sense Amplifier

CURRENT-LIMIT REFERENCE

The current-limit reference voltage determines the load current at which the ADM1270 limits the current during an overcurrent event. This reference voltage is compared to the amplified current sense voltage to determine when the current-limit threshold is reached.

An internal current-limit reference selector block continuously compares the current-limit (ISET) and foldback (FLB) voltages to determine which voltage is the lowest at any given time; the lowest voltage is used as the current-limit reference. This behavior ensures that the programmed current limit, ISET, is used in normal operation, and that the foldback feature reduces the current limit when required during startup and/or fault conditions.

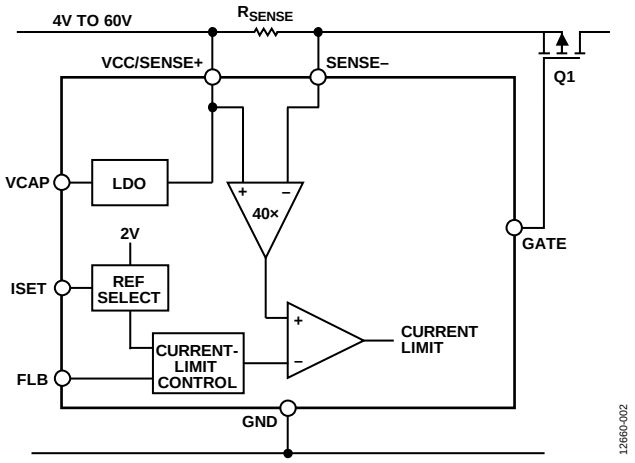

Figure 2. Current-Limit Reference Selection

The FLB voltage varies during different modes of operation and, therefore, is clamped to a minimum level of 200 mV. This behavior prevents zero current flow due to the current limit being set too low. Figure 3 provides an example of how the FLB and ISET voltages interact during startup as the ADM1270 turns on the FET and charges the load capacitance. Depending on how the foldback feature is configured, the transition point varies to ensure that the FET operates within the correct limits.

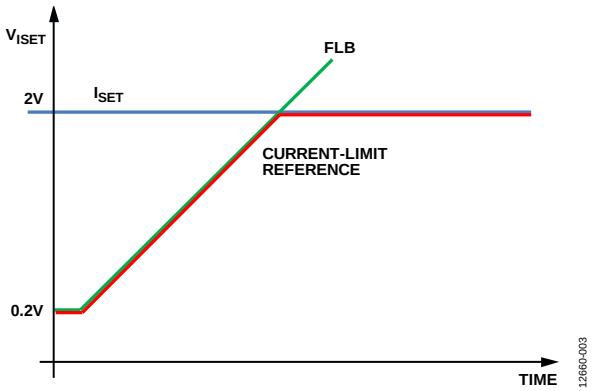

Figure 3. Interaction of Foldback (FLB) and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor value decreases for a given current sense voltage. Choosing an appropriate current sense resistor can be difficult due to the limited selection of low value resistors. The ADM1270 provides an adjustable current sense voltage limit to handle this issue. The device allows the user to program the required current sense voltage limit from 12.5 mV to 62.5 mV.

The default value is 50 mV and is achieved by connecting the ISET pin directly to the VCAP pin. This circuit configuration configures the device to use an internal 2 V reference, which results in 50 mV at the sense inputs (see Figure 4).

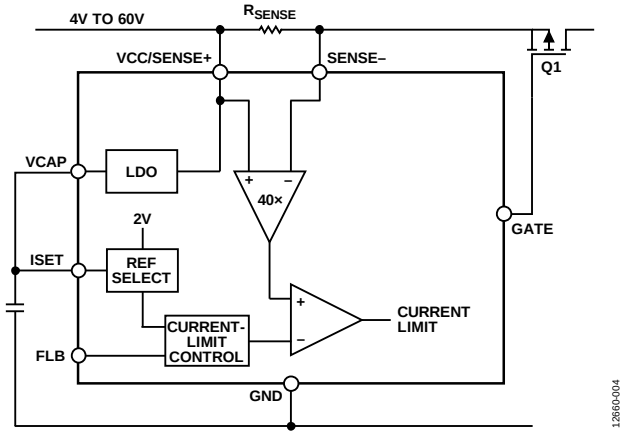

Figure 4. Fixed 50 mV Current Sense Limit

To program the sense voltage from 12.5 mV to 62.5 mV, an external resistor divider sets the reference voltage on the ISET pin (see Figure 5).

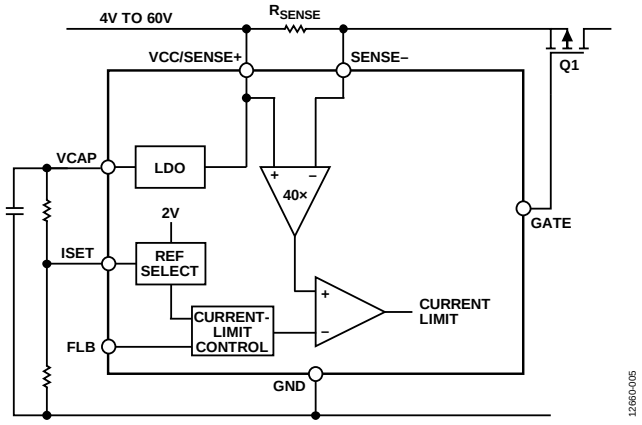

Figure 5. Adjustable 12.5 mV to 62.5 mV Current Sense Limit

The VCAP pin has a 3.6 V internally generated voltage that can set a voltage at the ISET pin. Assuming that V_{ISET} equals the voltage on the ISET pin, select the resistor divider values to set the ISET voltage as follows:

$$V_{ISET} = V_{SENSE} \times 40$$

where V_{SENSE} is the current sense voltage limit.

The VCAP rail also can be used as the pull-up supply for setting other pins. To guarantee that VCAP meets its accuracy specifications, do not apply a load to the VCAP pin greater than 100 µA.

FOLDBACK

Foldback is a method to actively reduce the current limit as the voltage drop across the FET increases. This technique keeps the power dissipation in the FET at a minimum during power-up, overcurrent, or short-circuit events. It also reduces the need to oversize the FET to accommodate worst-case conditions, resulting in board size and cost savings.

Assuming that the supply voltage remains constant and within tolerance, the ADM1270 detects the voltage drop across the FET by sensing output voltage through a resistor divider. The device, therefore, relies on the principle that the drain of the FET is at the maximum expected supply voltage, and that the magnitude of the output voltage is relative to that of the V_{DS} of the FET. Using a resistor divider from the output voltage to the FLB pin, the relationship from V_{OUT}, and thus V_{DS}, to V_{FLB} can be derived.

Design the resistor divider to result in a voltage equal to $V_{ISET}/2$ when V_{OUT} falls below the desired level. This voltage must be well below the working tolerance of the supply rail. As V_{OUT} continues to drop, the current-limit reference follows V_{FLB} because it is now the lowest voltage input to the current-limit reference selector block, resulting in a reduction of the current limit and, therefore, the regulated load current. To prevent the current from decreasing to zero, a clamp activates when V_{FLB} reaches 200 mV. The current limit cannot drop below this level.

To ensure that the SOA characteristics of a particular FET are not violated, the minimum current for this clamp varies from design to design. However, the current-limit reference fixes this clamp at 200 mV, which equals 10 mV across the sense resistor. Therefore, the main ISET voltage can be adjusted to adjust the clamp to the required percentage current reduction. For example, if V_{ISET} equals 1.6 V, set the clamp at 25% of the maximum current.

TIMER

An essential block of the ADM1270 is the TIMER function, which limits the time the current is in regulation during an overcurrent event. MOSFETs are designed to withstand a given amount of power for a prescribed maximum time. The MOSFET manufacturers outline this range, or SOA, using a graph such as that shown in Figure 6.

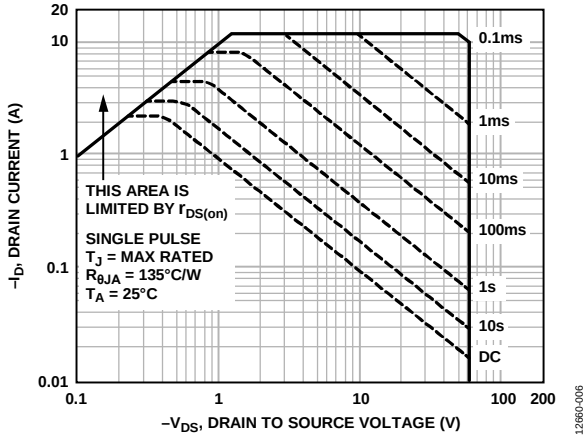

Figure 6. MOSFET SOA Graph

The SOA graph shows a relationship between the combined drain to source voltage, the drain current, and the time duration that the MOSFET can withstand this dissipation. For example, the MOSFET in Figure 6 can withstand 60 V and 2 A (120 W) for 1 ms. If this condition persists for a greater duration, the MOSFET may be damaged. The TIMER circuit can ensure that the length of time the MOSFET is subject to these worst-case conditions is limited by the external TIMER capacitor. For example, if the TIMER is set to 1 ms, and the current exceeds the limit for more than 1 ms, the circuit times out and shuts down the MOSFET.

The TIMER pin handles the timing function with an external capacitor, C_{TIMER}. The two TIMER pin comparator thresholds are V_{TIMERL} (0.1 V) and V_{TIMERH} (2.0 V). There are two timing current sources as well: a 20 µA pull-up current and a 1 µA pull-down current.

These current and voltage levels, in combination with the user chosen value of C_{TIMER}, determine the fault current-limit time and the on-time of the hot swap retry duty cycle. The TIMER pin capacitor value is determined using the following equation:

$$C_{TIMER} = (t_{ON} \times 20\ \mu A)/V_{TIMERH}$$

where:

t_{ON} is the time that the FET is allowed to spend in regulation at the current limit.
V_{TIMERH} is the TIMER high threshold.

The choice of FET is based on matching this time with the SOA characteristics of the FET. Foldback can also be used to simplify the selection.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 20 µA TIMER pull-up current is activated. The ADM1270 begins to regulate the load current at the current limit, initiating a rising voltage ramp on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH}, the 20 µA pull-up current is disabled, and the 1 µA pull-down current is enabled. If the voltage on the TIMER pin falls below V_{TIMERL}, the TIMER pin is discharged to GND using a strong pull-down current on the TIMER pin.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which causes the timer to start a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 20 µA pull-up current remains active, and the FET remains in regulation. This condition allows the TIMER pin to reach V_{TIMERH} and to initiate the GATE shutdown, and the $\overline{\text{FAULT}}$ pin is pulled low immediately.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which causes the timer to start shortly before the current reaches the defined current limit.

In latch-off mode, the TIMER pin is discharged to GND when it reaches the V_{TIMERH} threshold. The TIMER_OFF pin begins to charge up. While the TIMER_OFF pin is ramping up, the hot swap controller remains off and cannot be turned back on, and the $\overline{\text{FAULT}}$ pin remains low. When the voltage on the TIMER_OFF pin rises above the $V_{TMROFFH}$ threshold, the hot swap controller can be reenabled by toggling the ENABLE pin from high to low and then high again.

TIMER_OFF

The TIMER_OFF pin handles two timing functions with an external capacitor, C_{TIMER_OFF}. There is one TIMER_OFF pin comparator threshold at $V_{TMROFFH}$ (2.0 V). There are two timing current sources, a 20 µA pull-up current and a 1 µA pull-up current.

These current and voltage levels, in combination with the user chosen value of C_{TIMER_OFF}, determine the initial power-on reset time and also set the fault current-limit off time.

When VCC is connected to the input supply, the internal supply (VCAP) of the ADM1270 must charge up. VCAP starts up and settles in a very short time. When the UVLO threshold voltage is exceeded at VCAP, the device emerges from reset. During this first brief reset period, the GATE and TIMER pins are both held low.

The ADM1270 then proceeds through an initial timing cycle. The TIMER_OFF pin is pulled high with 20 µA. When the TIMER_OFF pin reaches the $V_{TMROFFH}$ threshold (2.0 V), the initial timing cycle is complete. This initial power-on reset duration is determined by the following equation:

$$t_{INITIAL} = V_{TMROFFH} \times (C_{TIMER\_OFF}/20\ \mu A)$$

For example, a 100 nF capacitor results in a delay of approximately 10 ms. If the UV and OV inputs indicate that VCC is within the defined window of operation when the initial timing cycle terminates, the device is ready to start a hot swap operation.

At the completion of this initial power-on reset cycle, the TIMER_OFF pin is ready to perform a second function. When the voltage at the TIMER pin exceeds the fault current-limit time threshold voltage of V_{TIMERH} (2.0 V), the 1 µA pull-up current is activated on TIMER_OFF, and C_{TIMER_OFF} begins to charge initiating a voltage ramp on the TIMER_OFF pin. When the TIMER_OFF pin reaches $V_{TMROFFH}$, the TIMER_OFF fault current-limit off time is complete.

This fault current-limit off time is determined by the following equation:

$$t_{TIMER\_OFF} = V_{TMROFFH} \times (C_{TIMER\_OFF}/1\ \mu A)$$

For example, a 100 nF capacitor results in an off time of approximately 200 ms from the time that TIMER exceeds V_{TIMERH} to the time that TIMER_OFF reaches $V_{TMROFFH}$.

HOT SWAP RETRY DUTY CYCLE

The ADM1270 turns off the FET after an overcurrent fault and then uses the capacitor on the TIMER_OFF pin to generate a delay before automatically retrying the hot swap operation. To configure the ADM1270 for automatic retry mode, tie the $\overline{\text{FAULT}}$ pin to the ENABLE pin. Note that a pull-up resistor to VCAP is required on the $\overline{\text{FAULT}}$ pin.

When an overcurrent fault occurs, the capacitor on the TIMER pin charges with a 20 µA pull-up current. When the TIMER pin reaches V_{TIMERH} (2.0 V), the GATE pin is pulled high, turning off the FET. When the $\overline{\text{FAULT}}$ pin is tied to the ENABLE pin for automatic retry mode, the TIMER_OFF pin begins to charge with a 1 µA current source. When the TIMER_OFF pin reaches $V_{TMROFFH}$ (2.0 V), the ADM1270 automatically restarts the hot swap operation.

The automatic retry duty cycle is set by the ratio of 1 µA/20 µA and the ratio of C_{TIMER}/C_{TIMER_OFF}. The retry duty cycle is set by the following equation:

$$Duty\_Cycle = (C_{TIMER} \times 1\ \mu A)/(C_{TIMER\_OFF} \times 20\ \mu A)$$

The value of the CTIMER and CTIMER_OFF capacitors determine the on and off time of this cycle, which are calculated as follows:

$$t_{ON} = V_{TIMERH} \times (C_{TIMER}/20\ \mu A)$$

$$t_{OFF} = V_{TMROFFH} \times (C_{TIMER\_OFF}/1\ \mu A)$$

A 100 nF capacitor on the TIMER pin gives an on time of 10 ms. A 100 nF capacitor on the TIMER_OFF pin gives an off time of 200 ms. The device retries continuously in this manner and can be disabled manually by holding the ENABLE pin low, or by disconnecting the $\overline{\text{FAULT}}$ pin. To prevent thermal stress in the FET, a capacitor on the TIMER_OFF pin can be used to extend the retry time to any desired level.

GATE AND RPFG CLAMPS

The circuits driving the GATE and RPFG pins are clamped to less than 14 V below the VCC/SENSE+ pin. These clamps ensure that the maximum V_{GS} rating of the external FETs is not exceeded.

The reverse protection FET gate pin (RPFG) drives the gate of an external PMOSFET. This PMOSFET, Q2, provides reverse polarity protection to the ADM1270 and the system being powered. If the VCC and GND pins have been reverse connected (that is, where power is actually applied to GND), VCC is negative with respect to the system ground. In this condition, Q2 prevents current from flowing in the reverse direction because the gate of Q2 is held at GND, and Q2 is off. V_{OUT} is not pulled below GND, and the system is protected against a reverse polarity connection.

In the typical case where power is applied to VCC, the gate is still pulled down and allows the FET Q2 to turn on and conduct current in the forward direction. Operating Q2 in this way provides a low on-resistance, low voltage drop compared to a diode for reverse polarity protection, giving the system higher efficiency and more headroom for operation. Refer to the ADM1270 data sheet for the connection of Q2 and RPFG for proper operation.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1270 includes a separate, high bandwidth, current sense amplifier to detect a severe overcurrent that is indicative of a short circuit. The fast response time allows the ADM1270 to handle events of this type that could otherwise cause catastrophic damage if not detected and dealt with very quickly. The fast response circuit ensures that the ADM1270 can detect an overcurrent event of approximately 200% of the normal current limit and control the current within approximately 2 µs.

UNDERVOLTAGE AND OVERVOLTAGE

The ADM1270 monitors the supply voltage for UV and OV conditions. The UV and OV pins are connected to the inputs of the voltage comparators and compared to an internal 1 V voltage reference.

Figure 7 illustrates the voltage monitoring input connections. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UV pin falls below 1 V, and the FET is turned off using the 10 mA pull-up current. Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the FET is turned off using the 10 mA pull-up current.

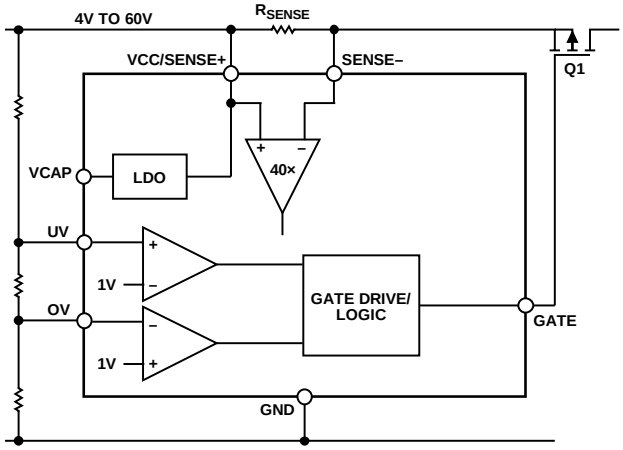

Figure 7. Undervoltage and Overvoltage Supply Monitoring

ENABLE INPUT

The ADM1270 provides a dedicated ENABLE digital input pin. The ENABLE pin allows the ADM1270 to remain off by using a hardware signal, even when the voltage on the UV pin is greater than 1.0 V, and the voltage on the OV pin is less than 1.0 V. Although the UV pin can be used to provide a digital enable signal, using the ENABLE pin for this purpose keeps the ability of the UV pin free to monitor undervoltage conditions.

In addition to the conditions for the UV and OV pins, the ADM1270 ENABLE input pin must be high for the device to begin a power-up sequence.

A similar function can be achieved using the UV pin directly. Alternatively, if the UV divider function is still required, the configuration shown in Figure 8 can be used.

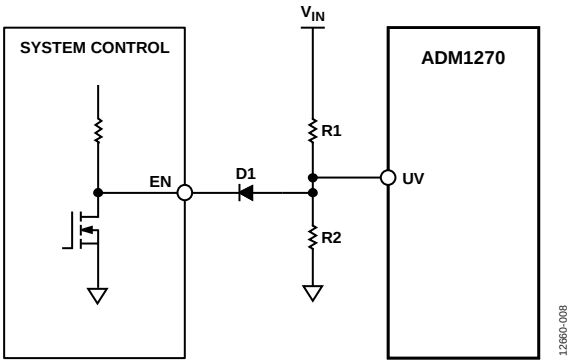

Figure 8. Using the UV Pin as an Enable

Diode D1 prevents the external driver pull-up resistor from affecting the UV threshold. Select Diode D1 using the following criteria:

$$(V_F \times D1) + (V_{OL} \times EN) << 1.0\ V\ (I_F = V_{IN}/R1)$$

Ensure that the EN sink current does not exceed the specified V_{OL} value. If the open-drain device has no pull-up, the diode is not required.

POWER GOOD

The power-good (PWRGD) output can be used to indicate whether the output voltage exceeds a user defined threshold and can, therefore, be considered good. The PWRGD output is set by a resistor divider connected to the FB_PG pin (see Figure 9).

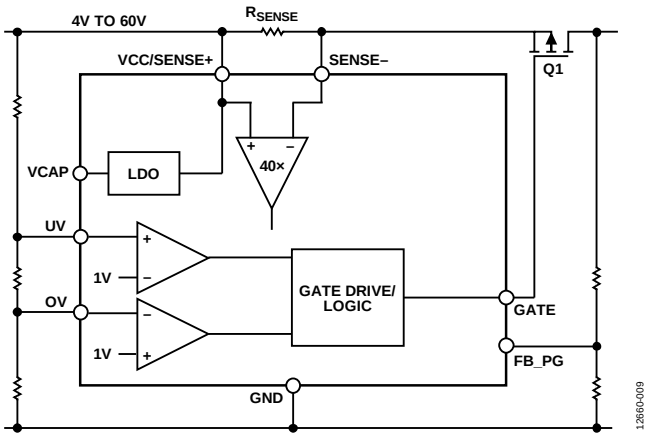

Figure 9. Generation of PWRGD Signal

When the voltage at the FB_PG pin exceeds the 1 V threshold (indicating that the output voltage has risen), the open-drain pull-down current is disabled, allowing PWRGD to be pulled high. The PWRGD pin is an open-drain output that pulls low when the voltage at the FB_PG pin is lower than the 1 V threshold minus the hysteresis (power bad). Hysteresis on the FB_PG pin is fixed at 30 mV. PWRGD is guaranteed to be in a valid state for $V_{CC} \geq 1.7$ V.

Calculate the power-good threshold using the following equation:

$$V_{PWRGD} = 1\ V \times (1 + RPG1/RPG2)$$

where:

RPG1 is the resistance from V_{OUT} to FB_PG.
RPG2 is the resistance from FB_PG to GND.

EVALUATION BOARD SCHEMATICS AND ARTWORK

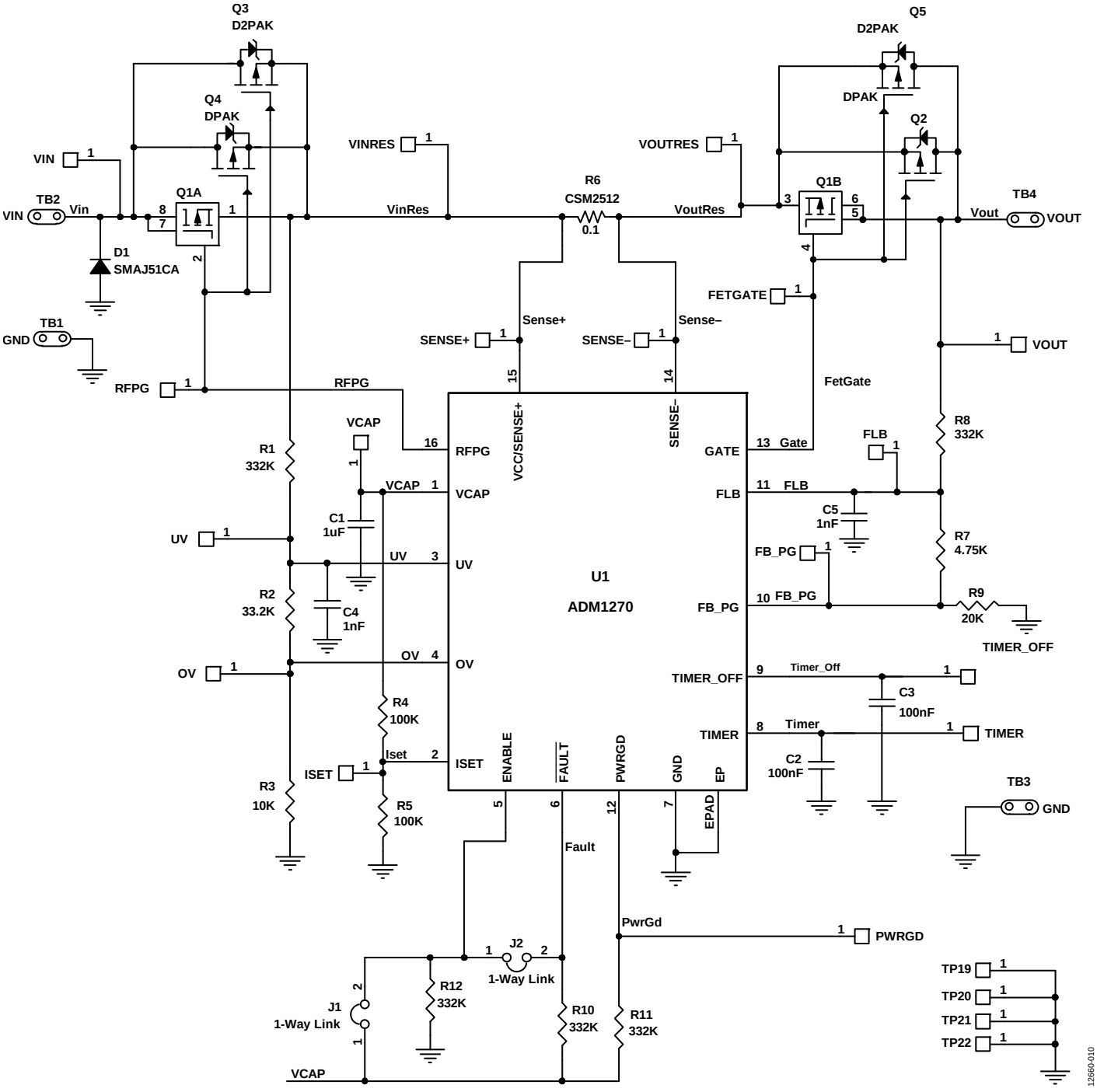

Figure 10. ADM1270CP-EVALZ LFCSP Evaluation Board Schematic

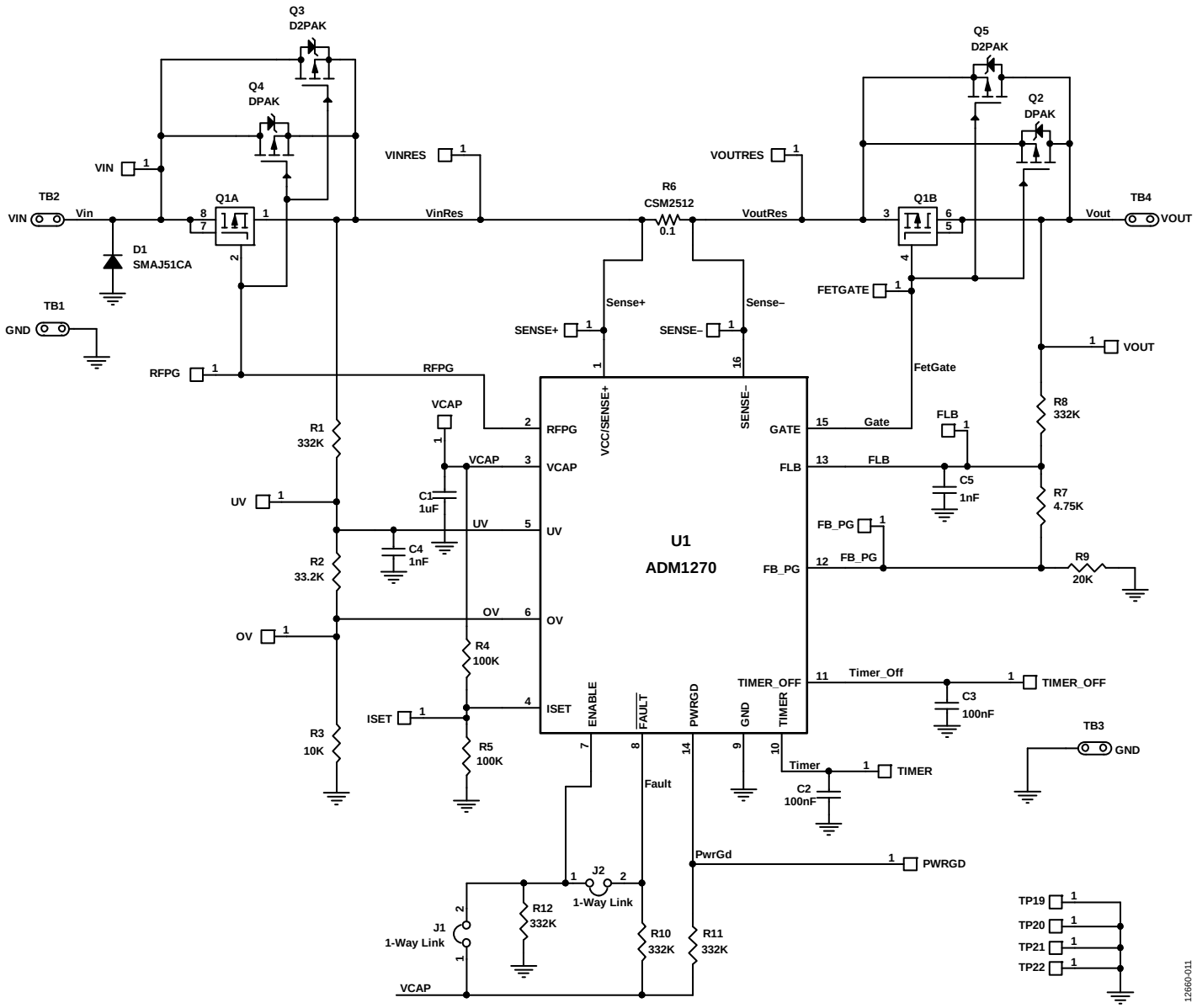

Figure 11. ADM1270RQ-EVALZ QSOP Evaluation Board Schematic

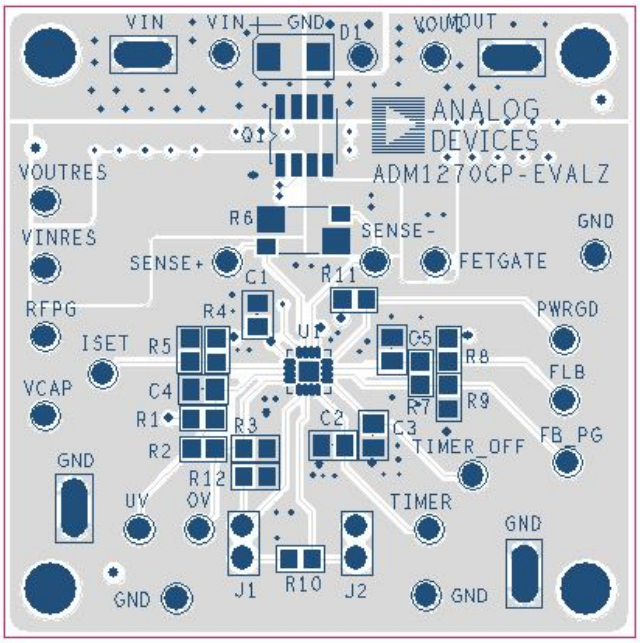

Figure 12. ADM1270CP-EVALZ LFCSP Evaluation Board Top Layer

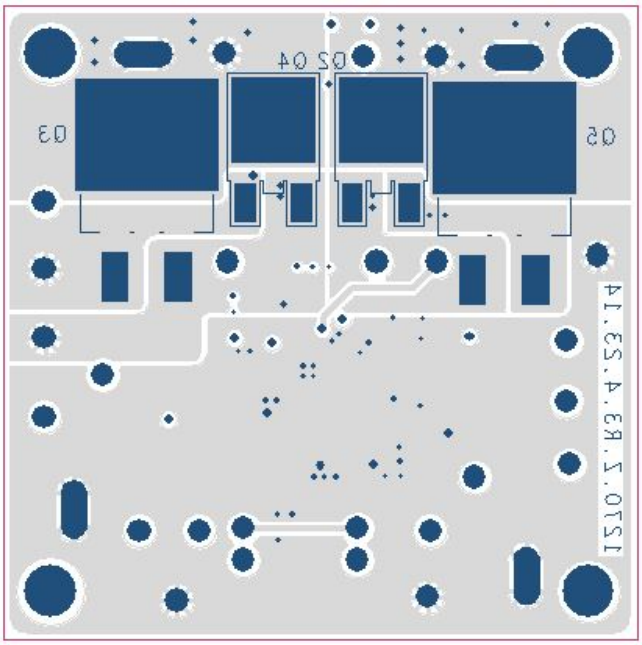

Figure 14. ADM1270CP-EVALZ LFCSP Evaluation Board Bottom Layer

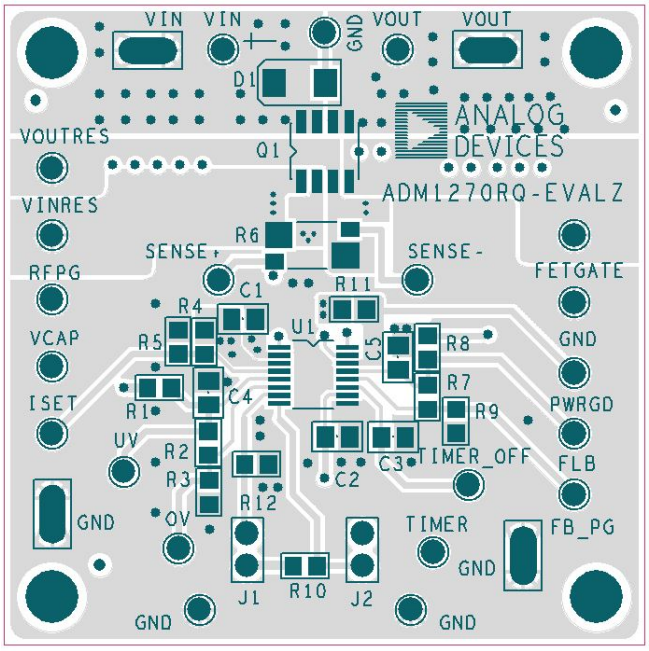

Figure 13. ADM1270RQ-EVALZ QSOP Evaluation Board Top Layer

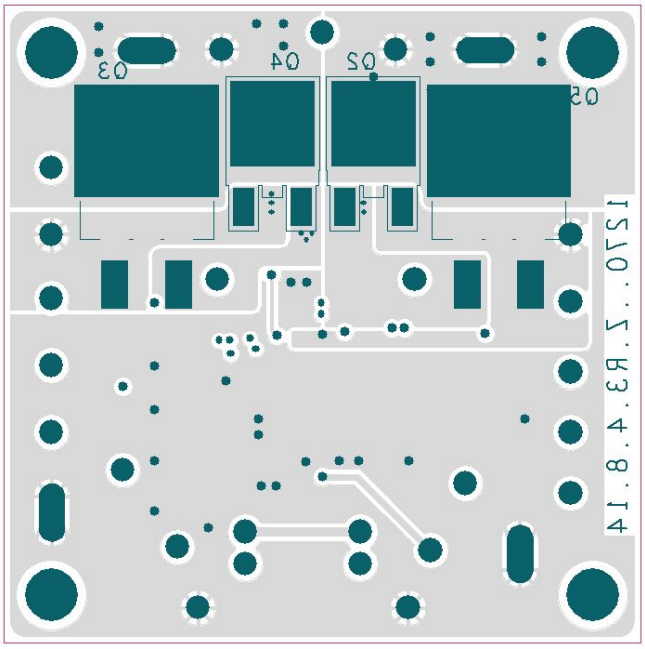

Figure 15. ADM1270RQ-EVALZ QSOP Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Qty	Designator	Description	Manufacturer/Vendor	Part Number
1	U1	ADM1270CP or ADM1270RQ	Analog Devices, Inc.	ADM1270ACPZ-R7 or ADM1270ARQZ-R7
1	C1	Capacitor, MLCC, 1 µF, 25 V, 0805, X5R	Murata (or equivalent)	GRM216R61E105KA12
2	C2, C3	Capacitor, MLCC, 100 nF, 25 V, 0805, X7R	Murata (or equivalent)	GRM21BR71E104KA01
2	J1, J2	Header, single, straight, 2 pins	Sullins Connector Solutions	PEC02SAAN
5	R1, R8, R10 to R12	Resistor, 332 kΩ, 1%, 0805 case	Vishay Dale	CRCW0805332KFKEA
1	R2	Resistor, 33.2 kΩ, 1%, 0805 case	Vishay Dale	CRCW080533K2FKEA
1	R3	Resistor, 10 kΩ, 1%, 0805 case	Vishay Dale	CRCW080510K0FKEA
2	R4, R5	Resistor, 100 kΩ, 1%, 0805 case	Vishay Dale	CRCW0805100KFKEA
1	R6	Resistor, 0.10 Ω, 1%, 2512 case	Vishay Precision Group	CSM2512
1	R7	Resistor, 4.75 kΩ, 1%, 0805 case	Vishay Dale	CRCW08054K75FKEA
1	R9	Resistor, 20 kΩ, 1%, 0805 case	Vishay Dale	CRCW080520K0FKEA
1	Q1	FDS9958 dual P-channel MOSFET, −60 V/−2.9 A, 105 mΩ	Fairchild	FDS9958