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Evaluating the ADP5003 Low Noise Micro PMU, 3 A Buck Regulator with 3 A LDO

FEATURES

PVIN1 input voltage range: 4.2 V to 15 V
Buck output voltage: 2.5 V (programmable from 0.6 V to 5.0 V)
PVIN2 Input voltage range: 0.65 V to 5 V
LDO output voltage: 1.8 V (programmable from 0.6 V to 3.3 V)

EVALUATION KIT CONTENTS

ADP5003CP-EVALZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

DC power supply for the PVIN1 and PVIN2 pins
Multimeters for voltage and current measurements
Electronic or resistive loads

GENERAL DESCRIPTION

The ADP5003CP-EVALZ evaluation board demonstrates the functionality of the ADP5003 dc-to-dc converter and low noise low dropout regulator (LDO).

Use the ADP5003CP-EVALZ to evaluate simple device measurements such as line regulation, load regulation, and efficiency. Device features include the buck regulator in fixed output or in adaptive headroom control and syncing the operating frequency to the external clock.

A full description of the ADP5003 is available in the ADP5003 data sheet and should be consulted when using this evaluation board.

PHOTOGRAPH OF THE ADP5003CP-EVALZ EVALUATION BOARD

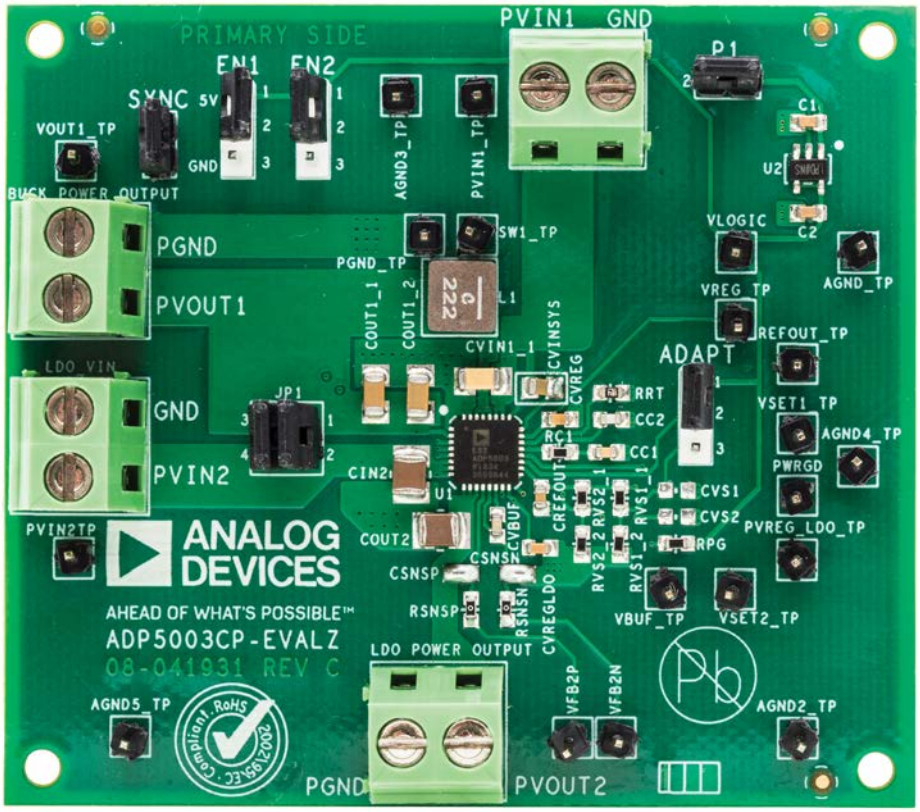

Figure 1.

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REVISION HISTORY

11/2017—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

EVALUATION BOARD CONFIGURATIONS

The ADP5003CP-EVALZ evaluation board is configured to provide a 1.8 V LDO output from a 4.2 V to 15 V input. To achieve this, the dc-to-dc regulator is configured to a 2.5 V output in fixed output mode or, when the ADAPT jumper is shorted, an output voltage that adaptively follows the LDO output voltage according to the load current.

Table 1 lists the ADP5003CP-EVALZ functions and Table 2 lists the components for the ADP5003 board.

Figure 2 outlines the ADP5003CP-EVALZ features available to the user and its supporting components.

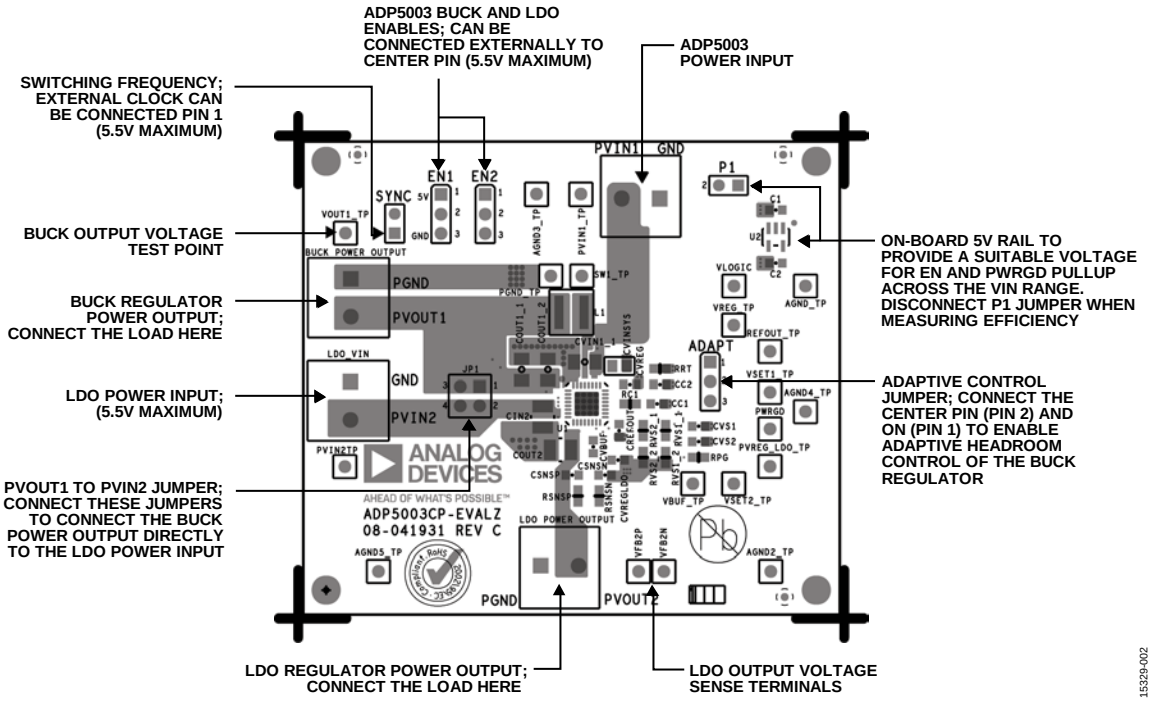

Figure 2. Outline of ADP5003 Evaluation Board Features

Table 1. Evaluation Board Function Descriptions

Jumper/Connector Mnemonic	Description
PVIN1	ADP5003 power input screw terminal.
GND	Ground screw terminal.
PVIN1_TP	Test point for buck input voltage.
P1	Insert jumper to enable the on-board 5 V LDO. Disconnect this before implementing efficiency measurements and externally connect the 5 V voltage source to the enable pins.
VLOGIC	5 V pull-up voltage for enable pins and PWRGD.
EN1	Enable input jumper. Connect center pin to 5 V pin to enable the buck regulator.
EN2	Enable input jumper. Connect center pin to 5 V pin to enable the LDO regulator.
ADAPT	Jumper for adaptive headroom control. Connect the center pin to Pin 1 to activate the adaptive headroom control. Connect the center pin to Pin 3 to disable the adaptive headroom control.
SYNC	SYNC input pin. Connect an external clock to the bottom pin to sync the operating frequency.
BUCK POWER OUTPUT	Buck output screw terminal consisting of PVOUT1 and PGND.
PVOUT1	Buck power output.
VOUT1_TP	Sense pin test point for the buck output voltage.
PGND	Power ground for buck. This must always be connected to the power supply ground terminal.
JP1	Jumper to directly connect the buck output to the LDO input.
LDO_VIN	LDO input screw terminal consisting of PVIN2 and GND.
PVIN2TP	Test point for the LDO input voltage.
LDO POWER OUTPUT	LDO output screw terminal consisting of PVOUT2 and PGND.
VFB2P	LDO positive remote sense pin. Remove the CSNSP solder bridge and connect this test point to the positive terminal of the load to enable remote sense.
VFB2N	LDO negative remote sense pin. Remove the CSNSN solder bridge and connect this test point to the negative terminal of the load to enable remote sense.

MEASUREMENT SETUP

BUCK MEASUREMENTS

Figure 3 shows the recommended setup to evaluate the buck regulator of the ADP5003CP-EVALZ. For accurate efficiency measurements, measure the input voltage between PVIN1_TP and AGND3_TP and the output voltage between VOUT1_TP and AGND3_TP.

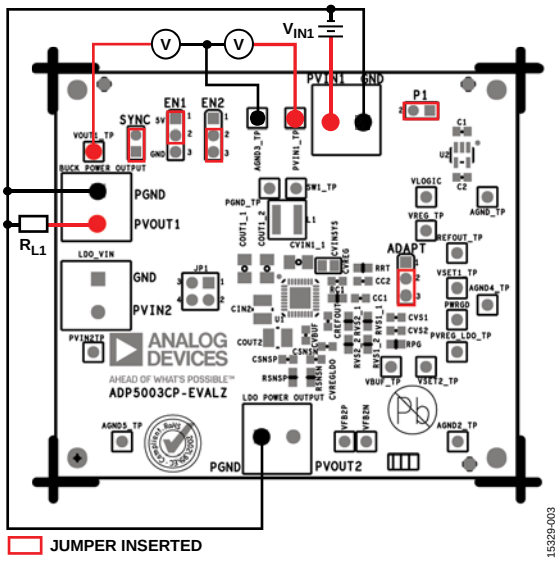

Figure 3. Buck Measurement Setup

LDO MEASUREMENTS

Figure 4 shows the recommended setup to evaluate LDO regulator of the ADP5003CP-EVALZ. Output voltage measurements are always between the VFB2P and VFB2N pins, which serve as sense nodes and the input voltage between PVIN2TP and AGND5_TP.

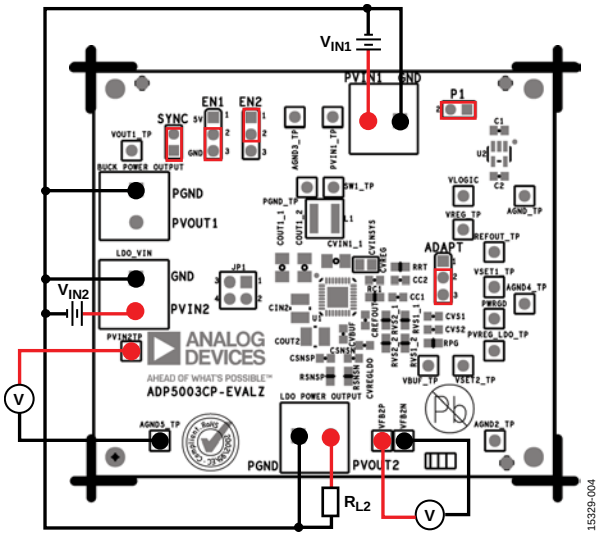

Figure 4. LDO Measurement Setup

OUTPUT VOLTAGE MEASUREMENTS

For basic output voltage accuracy measurements, connect the ADP5003CP-EVALZ evaluation board to two voltage sources and a voltmeter. Use a resistive load for either regulators when possible. Ensure that the resistor has an adequate power rating to handle the expected power dissipation. Use an electronic load as an alternative. Ensure the voltage source supplies enough current for the expected load levels, accounting for device efficiency.

Follow these steps to connect the evaluation board to a voltage source and voltmeter:

1. Connect the negative terminal of the first voltage source to the GND screw terminal besides the PVIN1 screw terminal located at the upper side of the evaluation board.
2. Connect the positive terminal of the first voltage source to the PVIN1 screw terminal located at the upper side of the evaluation board.
3. Connect a load between the PVOUT1 and PGND screw terminals at the BUCK POWER OUTPUT terminal block located at the left side of the evaluation board.
4. Connect the voltmeter across the PVIN1_TP and AGND3_TP test points.
5. Connect the voltmeter across the VOUT1_TP and AGND3_TP test points.
6. Connect the negative terminal of the second voltage source to the GND screw terminal of the LDO_VIN terminal block located at the left side of the evaluation board.
7. Connect the positive terminal of the second voltage source to the PVIN2 screw terminal of the LDO_VIN terminal block located at the left side of the evaluation board.
8. Connect a load between the PVOUT2 and PGND terminals at the LDO power output terminal located at the lower side of the evaluation board.
9. Connect the voltmeter across the VFB2P and VFB2N test points.

Turn on the voltage source for PVIN1 before turning on the voltage source for PVIN2. If the EN1 or EN2 jumper is in the 5V position, their respective regulator powers up.

At high loads, measure the input voltage between PVIN1_TP and AGND3_TP for the buck and PVIN2_TP and AGND5_TP for the LDO. Compensate for the voltage drop or use a power supply with a 4-wire supply and sense arrangement.

LINE REGULATION

For line regulation measurements, monitor the regulator output while its input is varied. For good line regulation, the output must change as little as possible with varying input levels. It is possible to repeat this measurement under different load conditions. During line regulation tests, keep the power supply leads short and remove any additional input capacitor. Figure 5 and Figure 6 show the typical line regulation performance of the ADP5003 at the buck output and LDO sense pins, respectively.

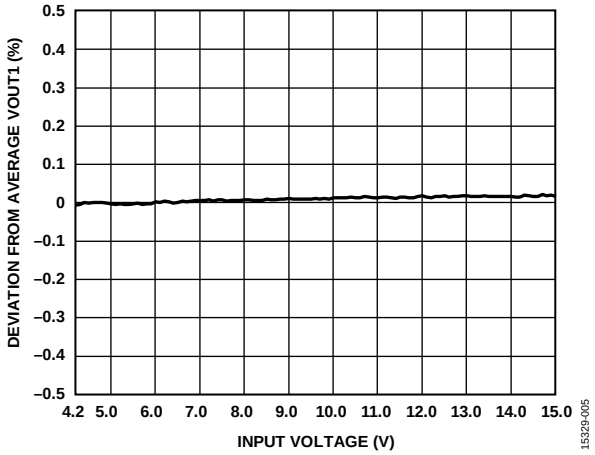

Figure 5. Buck Line Regulation

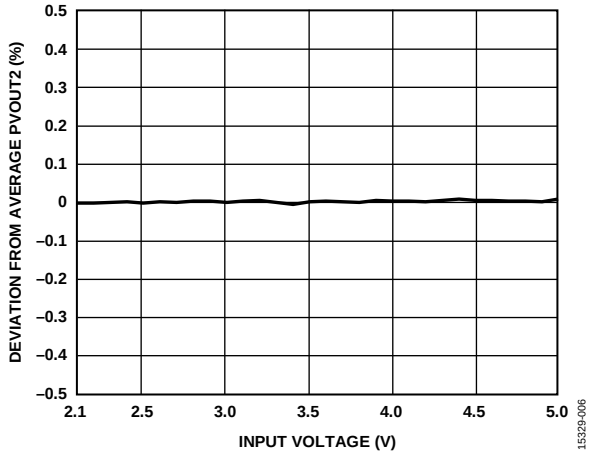

Figure 6. LDO Line Regulation

LOAD REGULATION

For load regulation measurements, monitor the regulator output while the load is varied. For good load regulation, the output must change as little as possible with varying loads. The input voltage must be held constant during this measurement. Figure 7 and Figure 8 show the typical load regulation performance of the ADP5003 at the buck output and LDO sense pins, respectively. Keep power leads short during this test and compensate for voltage drops at the input or use a power supply with remote sense.

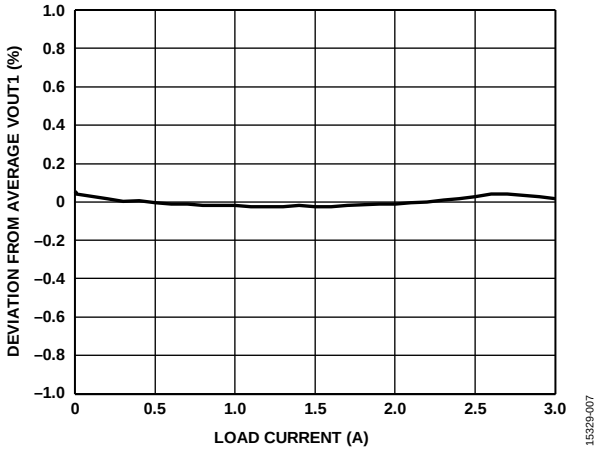

Figure 7. Buck Load Regulation

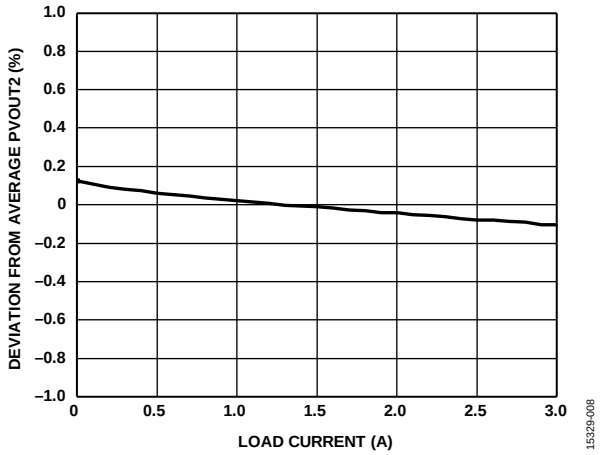

Figure 8. LDO Load Regulation

EFFICIENCY

For efficiency measurements, monitor the regulator input and output while the load is varied. The input voltage must be held constant during this measurement. Keep power leads short during this test and compensate for voltage drops at the input or use a power supply with remote sense. Connect ammeters in series with the input and output. Connect the voltmeters to their respective test points. If possible, particularly at low current, trigger the meters simultaneously and set to average readings for a period of a few hundred milliseconds or more. Figure 9 and Figure 10 show typical efficiency curves for a standalone buck and adaptive mode respectively.

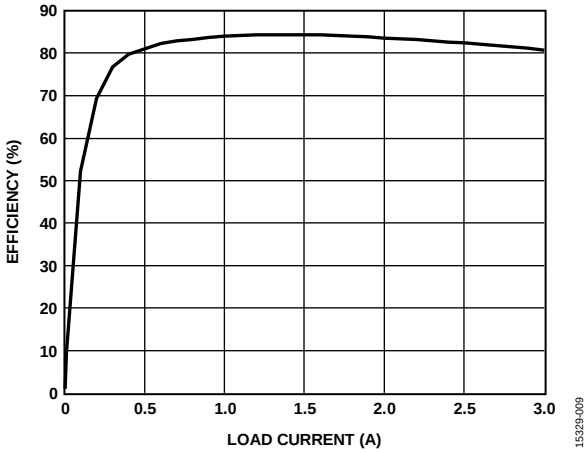

Figure 9. Buck Efficiency

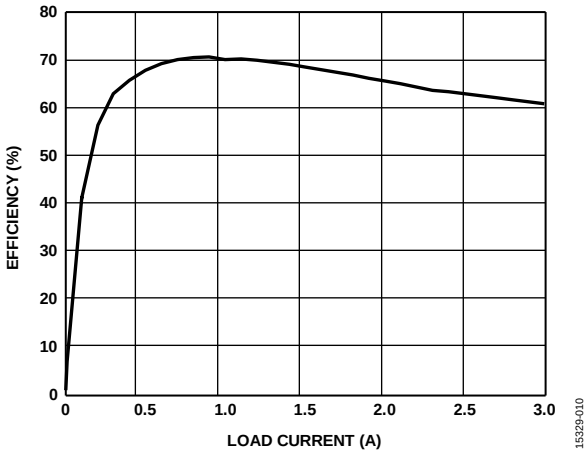

Figure 10. Adaptive Mode Efficiency

EVALUATION BOARD CONFIGURATION

ADAPTIVE HEADROOM CONTROL SETUP

The ADP5003CP-EVALZ evaluation board can be configured to operate in adaptive headroom control (see Figure 11) to provide a single step down voltage from PVIN1.

In this configuration, VSET1 is tied to VREG which activates the adaptive headroom control. When the buck is configured for adaptive headroom control, the ADP5003 manages the buck regulator output voltage depending on the LDO load current. The headroom profile of the adaptive headroom control delivers a consistent power supply rejection ratio (PSRR) across the load range while optimising efficiency of the overall system.

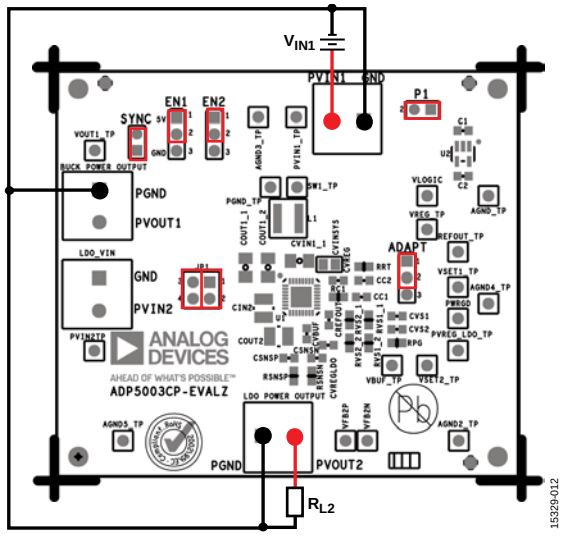

Figure 11. Circuit Diagram of Setup with Adaptive Headroom Control

FIXED OUTPUT SETUP WITH CASCADED REGULATORS

The ADP5003CP-EVALZ evaluation board can be configured to provide two voltage rails from a single input voltage (see Figure 12). The buck provides an intermediate voltage rail which also serves as the input to the LDO. The LDO provides the second rail and acts as a filter for the buck regulator switching noise and voltage ripple for noise sensitive applications. A second stage LC filter can be added between the buck output and the LDO input for additional filtering.

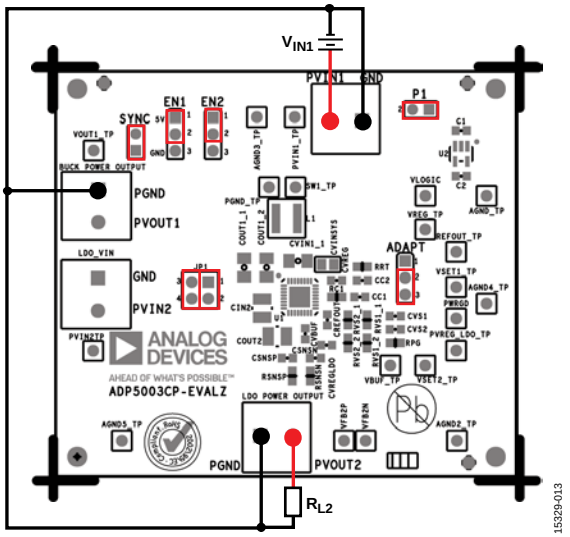

Figure 12. Circuit Diagram of Fixed Output Voltages in Cascaded Regulators Setup

EVALUATION BOARD SCHEMATICS AND ARTWORK

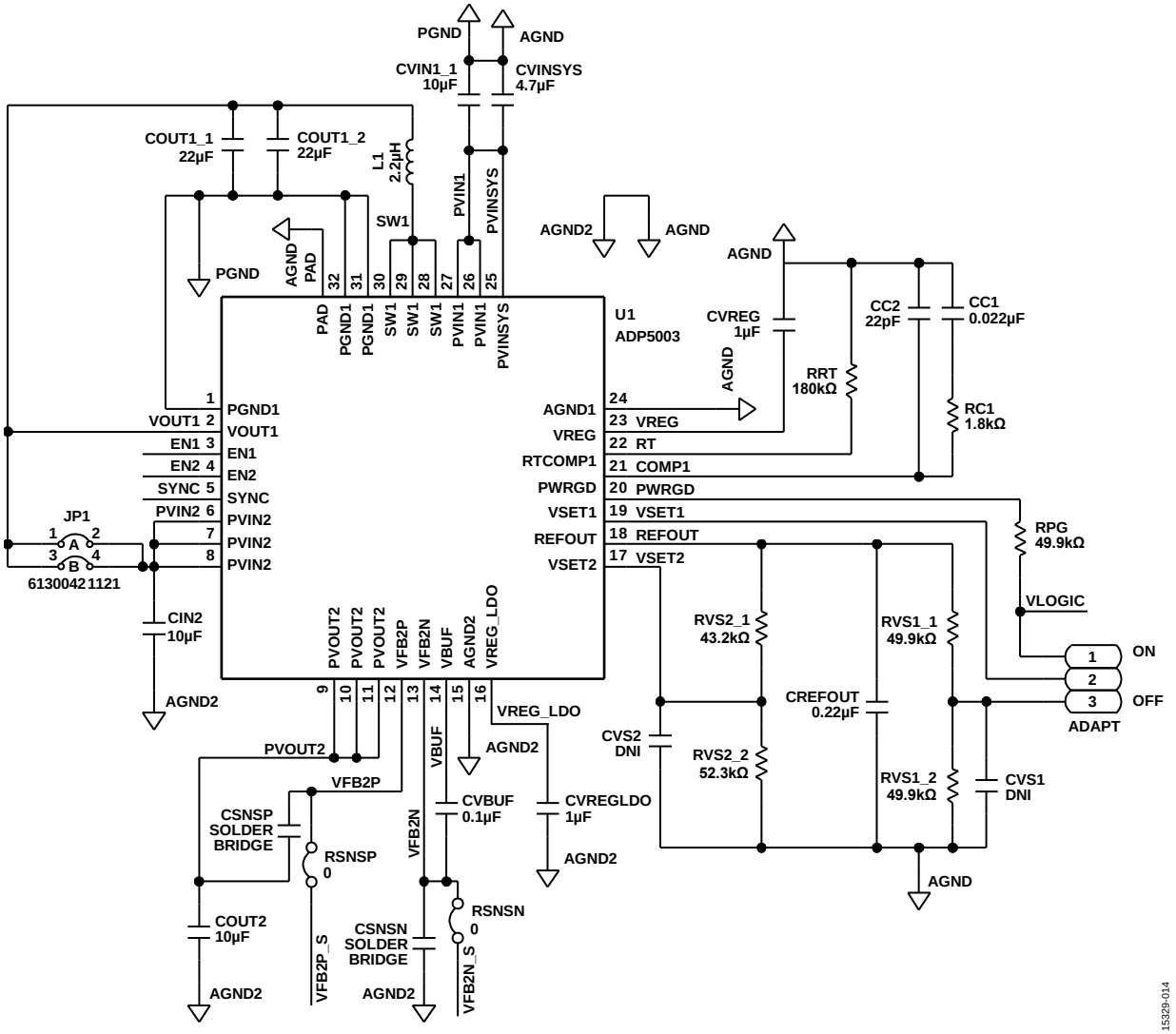

Figure 13. ADP5003CP-EVALZ Evaluation Board Schematic

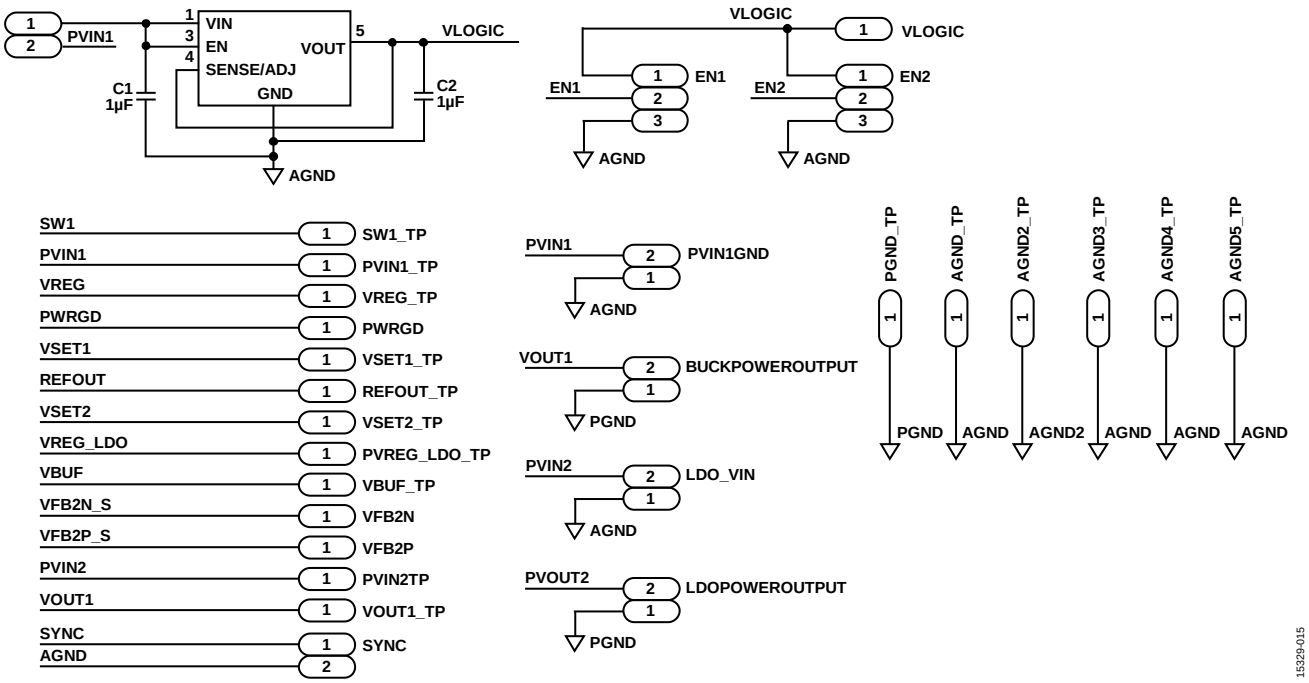

Figure 14. ADP5003CP-EVALZ Evaluation Board Schematic Connectors and Peripherals

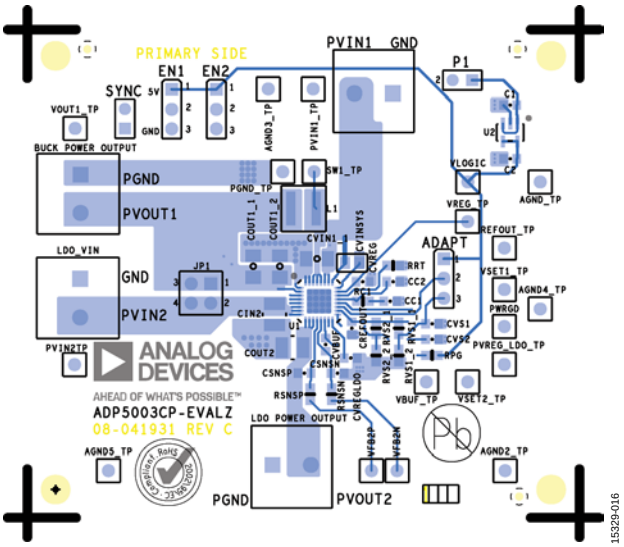

Figure 15. ADP5003CP-EVALZ Evaluation Board Top Layer

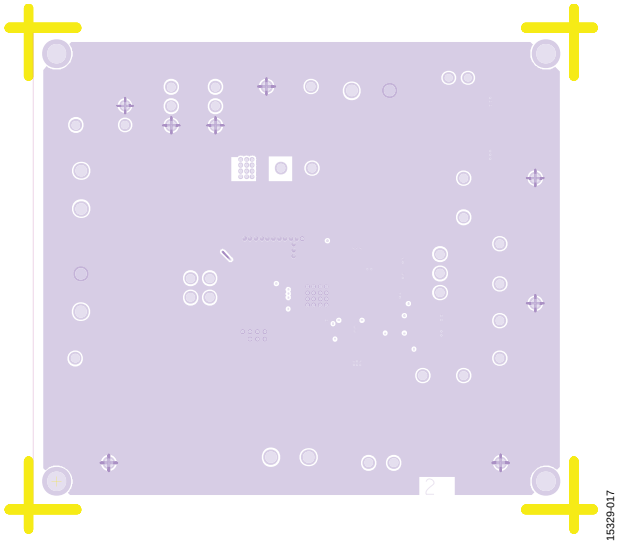

Figure 16. ADP5003CP-EVALZ Evaluation Board 2nd Layer

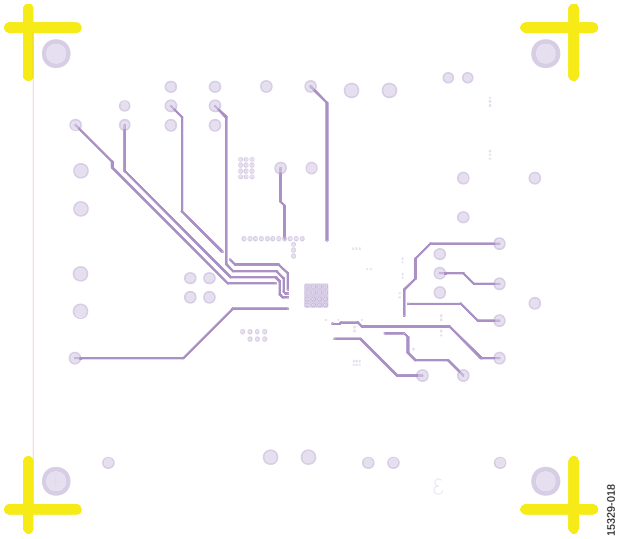

Figure 17. ADP5003CP-EVALZ Evaluation Board 3rd Layer

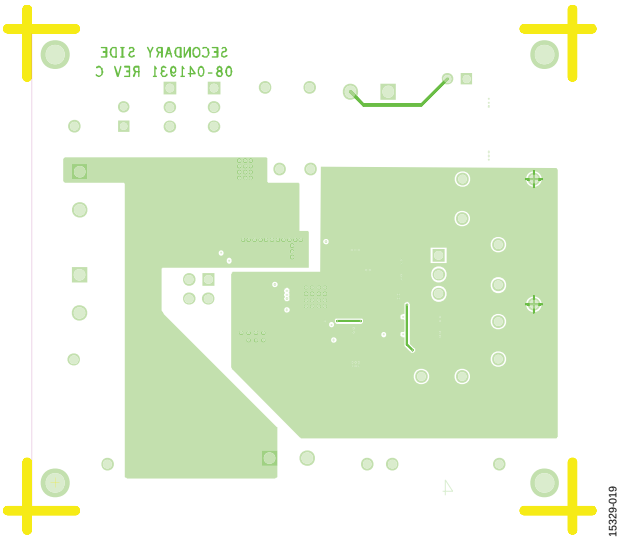

Figure 18. ADP5003CP-EVALZ Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Evaluation Board Components—ADP5003

Component	Description	Part Number	Manufacturer
U1	ADP5003, low noise, micro power management unit (PMU), 3 A buck regulator with 3 A LDO	ADP5003CP	Analog Devices, Inc.
CVIN1_1	V_{PVIN1} capacitor, 1206, 10 µF, 10%, 25 V	GRM31CR61E106KA12L	Murata
CVINSYS	$V_{PVINSYS}$ capacitor, 0805, 4.7 µF, 10%, 25 V	GRM21BR61E475KA12L	Murata
COUT1_1, COUT1_2	V_{VOUT1} capacitor, 1206, 22 µF, 10%, 16 V	1206YD2266KAT2A	AVX
L1	V_{VOUT1} inductor, XAL5030, 2.2 µH, 20%	XAL5030-222ME	Coilcraft
CC1	Buck regulator compensation capacitor, 0603, 22 nF, 10%, 50 V	06035C223KAZ2A	AVX
CC2	Buck regulator compensation capacitor, 0603, 22 pF, 5%, 50 V	06035C220JAT2A	AVX
RC1	Buck regulator compensation resistor, 0603, 1.8 kΩ, 1%		
CIN2	V_{PVIN2} capacitor, 1210, 10 µF, 10%, 63 V	GRM32ER71J106KA12L	Murata
COUT2	V_{PVOUT2} capacitor, 1210, 10 µF, 10%, 63 V	GRM32ER71J106KA12L	Murata
RVS1_1	V_{VSET1} top resistor, 0603, 49.9 kΩ, 1%		
RVS1_2	V_{VSET1} bottom resistor, 0603, 49.9 kΩ, 1%		
RVS2_1	V_{VSET2} top resistor, 0603, 43.2 kΩ, 1%		
RVS2_2	V_{VSET2} bottom resistor, 0603, 52.3 kΩ, 1%		
CVREG	V_{VREG} capacitor, 0603, 1 µF, 10%, 10 V	GRM188R71A105KA61D	Murata
CVREG_LDO	V_{VREG_LDO} capacitor, 0603, 1 µF, 10%, 10 V	GRM188R71A105KA61D	Murata
CVREFOUT	$V_{VREFOUT}$ capacitor, 0603, 220 nF, 10%, 10 V	0603ZC224KAT2A	AVX
CVBUF	V_{VBUF} capacitor, 0603, 100 nF, 10%, 16 V	CC0603KRX7R7BB104	Yageo
RRT	R_{RT} resistor, 0805, 180 kΩ, 1%		
CSNSP	Solder bridge, LDO positive sense return		
CSNSN	Solder bridge, LDO negative sense return		
RSNSP	V_{VFB2P} sense resistor, 0 Ω, 0603		
RSNSN	V_{VFB2N} sense resistor, 0 Ω, 0603		
U2	ADP7118, high voltage LDO with 5 V output voltage, thin shrink small outline package (TSSOP)	ADP7118AUJZ-5.0	Analog Devices, Inc.
C1	V_{IN} capacitor, 0603, 1 µF, 10%, 10 V	GRM188R71A105KA61D	Murata
C2	V_{LOGIC} capacitor, 0603, 1 µF, 10%, 10 V	GRM188R71A105KA61D	Murata
RPG	PWRGD pull-up resistor, 0603, 49.9 kΩ, 1%		

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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