One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

# Evaluation Board for AD5663R/AD5667R 16-Bit Dual-Channel Voltage Output DACs

## FEATURES

**Full featured evaluation board for the AD5663R and AD5667R**
**Flexible configuration options**
**On-board references**
**PC control in conjunction with Analog Devices, Inc. EVAL-SDP-CB1Z system demonstration platform (SDP)**

## PACKAGE CONTENTS

**EVAL-AD5663R-SDZ/EVAL-AD5667R-SDZ evaluation board**

## GENERAL DESCRIPTION

This user guide details the operation of the evaluation board for the AD5663R and the AD5667R. These are 16-bit, dual-channel, voltage output digital-to-analog converters (DACs). The AD5663R uses a serial peripheral interface (SPI) for configuration and control, whereas the AD5667R uses an $I^2C$ interface.

The evaluation board is designed to allow straightforward customer evaluation of the device using the hardware and software provided. The evaluation board can also be used to quickly create a prototype with the AD5663R/AD5667R, reducing design time. The AD5663R/AD5667R operate from a single 2.7 V to 5.5 V supply.

Full data on the AD5663R/AD5667R can be found in the appropriate data sheets available from Analog Devices and should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP board.

This evaluation board requires the EVAL-SDP-CB1Z board (SDP-B controller board), which is available for order on the Analog Devices website at www.analog.com.

## AD5663R/AD5667R EVALUATION BOARD

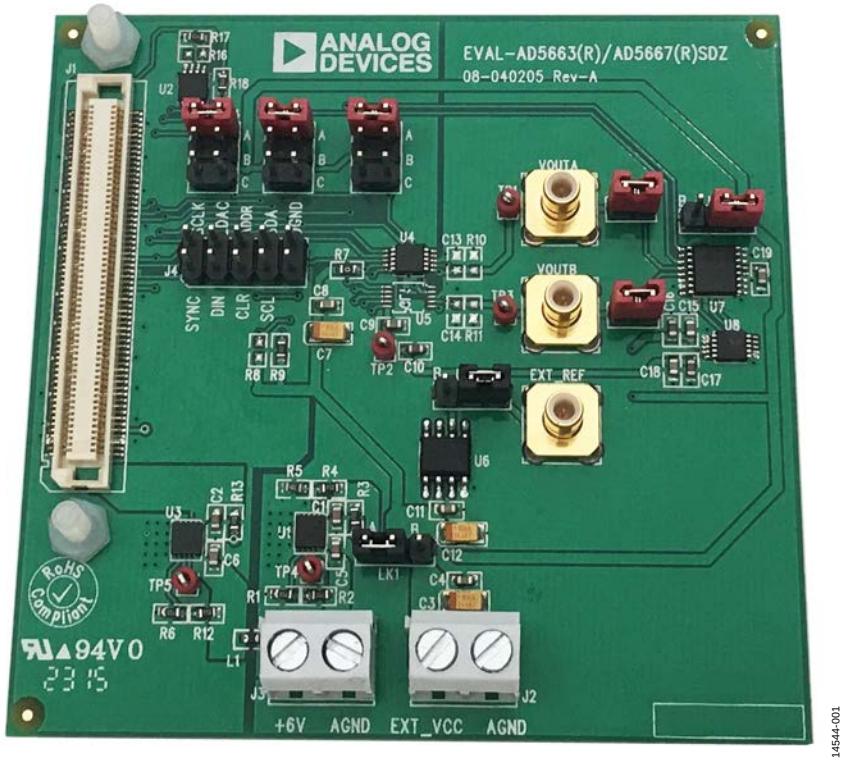


*Figure 1. AD5663R/AD5667R Evaluation Board*

# TABLE OF CONTENTS



## REVISION HISTORY

**5/2016—Revision 0: Initial Version**

# EVALUATION BOARD HARDWARE

## POWER SUPPLIES

The EVAL-AD5663R-SDZ and EVAL-AD5667R-SDZ evaluation board can be powered by the J3 or J2 connector. Supply the J3 connector with 6 V to 20 V and is regulated by the ADP7102 low noise, complimentary metal-oxide semiconductor (CMOS) low dropout regulator (LDO). Alternatively, the J2 connector can provide power to the board, bypassing the LDOs, and is intended for use with well regulated, bench supplies. All supplies are decoupled to ground with 10 µF tantalum and 0.1 µF ceramic capacitors.

**Table 1. Power Supply Connectors**

| Connector No. | Label | Voltage |
|---|---|---|
| J3, Pin 1 | +6 V | Single 6 V power supply, used to generate the INT_VCC board supply |
| J3, Pin 2 | AGND | Analog ground |
| J2, Pin 1 | EXT_VCC | External $V_{CC}$ |
| J2, Pin 2 | AGND | Analog ground |

## LINK OPTIONS

A number of link options are provided on the EVAL-AD5663R-SDZ and EVAL-AD5667R-SDZ board that must be set for the required operating conditions before using the board. Table 2 describes the positions of the links to control the evaluation board via the SDP board using a PC and external power supplies. The functions of these link options are described in detail in Table 3.

**Table 2. Link Options for SDP Control (Default)**

| Link Number | Option |
|---|---|
| LK1 | A |
| LK2 | A |
| LK3 | A |
| LK4 | B |
| LK5 | A |
| LK6 | Inserted |
| LK7 | Inserted |
| LK8 | A |

**Table 3. Link Functions**

| Link Number | Function |
|---|---|
| LK1 | This link selects the positive voltage source (VCC) for the board.<br>Position A selects the output from the LDO ADP7102 as the voltage source for the board (supplied by 6 V).<br>Position B selects the external voltage as the voltage source for the board. |
| LK2 | This link selects the $\overline{\text{LDAC}}$ pin voltage source.<br>Position A selects the voltage source from the SDP general-purpose input/output (GPIO).<br>Position B selects the voltage source (VCC).<br>Position C selects AGND. |
| LK3 | This link selects the $\overline{\text{CLR}}$ pin voltage source.<br>Position A selects the voltage source from the SDP GPIO.<br>Position B selects the voltage source (VCC).<br>Position C selects AGND. |
| LK4 | This link selects the ADDR pin voltage source, which sets the [A1:A0] $I^2C$ address bits on the AD5667R.<br>Position A selects the voltage source from the SDP GPIO. Address bits depend on state of GPIO.<br>Position B selects the voltage source (VCC), giving address bits of 00.<br>Position C selects AGND, giving address bits of 11.<br>This jumper can also be no connection, giving address bits of 10. |
| LK5 | This link selects the reference voltage source.<br>Position A allows use of the internal reference, or can also be used to apply an external reference after the internal reference is disabled.<br>Position B connects the evaluation board reference to the DAC. This position must only be used after the internal reference is disabled. |
| LK6 | This link connects the ADG728 switch and the AD7992 analog-to-digital converter (ADC) to $V_{OUT}A$ of the DAC.<br>Inserted: connected.<br>Removed: not connected. |
| LK7 | This link connects the ADG728 switch and the AD7992 ADC to $V_{OUT}B$ of the DAC.<br>Inserted: connected.<br>Removed: not connected. |
| LK8 | This link selects the $\overline{\text{RESET}}$ pin voltage level.<br>Position A selects the voltage source VCC.<br>Position B selects AGND. |

# EVALUATION BOARD SOFTWARE

## INSTALLING THE SOFTWARE

The EVAL-AD5663R-SDZ and EVAL-AD5667R-SDZ evaluation board uses the Analog Devices Analysis Control Evaluation (ACE) software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE installer installs necessary SDP drivers and .NET Framework 4 by default. Install ACE before connecting the SDP board to the USB port of the PC to ensure that the SDP board is recognized when it connects to the PC. Follow this link to download the software, and access full instructions on how to install and use this software: http://www.analog.com/ace.

After the installation is finished, the EVAL-AD5663R-SDZ and EVAL-AD5667R-SDZ evaluation board plug-ins appear when you open ACE.

## INITIAL SET UP

To set up the evaluation board, complete the following steps:

1. Connect the evaluation board to the SDP board and connect the SDP board to the computer via a USB cable.
2. Power the evaluation board as described in the Power Supplies section.
3. Run the ACE application. The EVAL-AD5663R-SDZ/ EVAL-AD5667R-SDZ board plug-ins appear in the attached hardware section of the **Start** tab.
4. Double-click on the board plug-in to open the board view seen in Figure 2.
5. The chip block diagram can be accessed by double-clicking on the AD5663R or AD5667R chip. This view provides a basic representation of functionality of the board. The main functions are labeled in Figure 3.

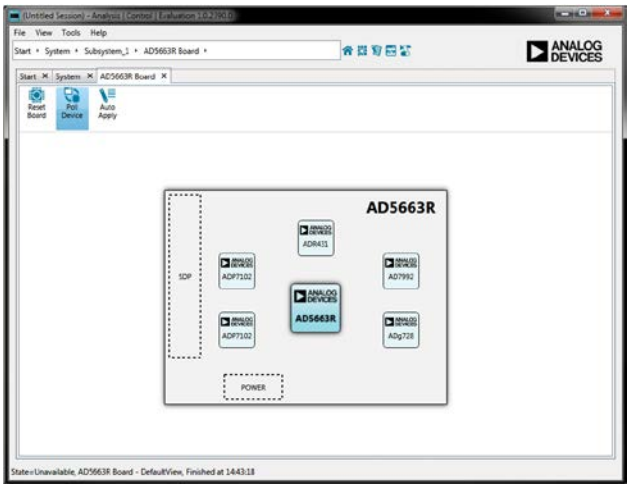


*Figure 2. Board View of the EVAL-AD5663R-SDZ*

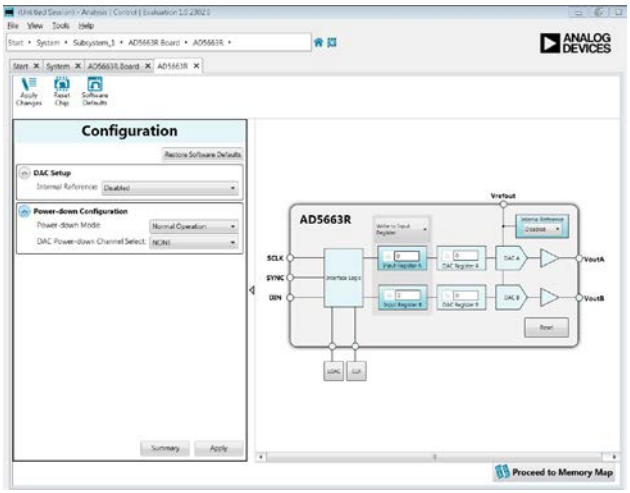


*Figure 3. Chip Block Diagram view for the AD5663R*

# BLOCK DIAGRAM AND DESCRIPTION

The EVAL-AD5663R-SDZ/EVAL-AD5667R-SDZ software is organized so that it appears similar to the functional block diagram shown in the data sheets. In this way, it is easy to correlate the functions on the board with the description in the data sheets. A full description of each block, register, and its settings is given in the AD5663R/AD5667R data sheets.

Some of the blocks and their functions are described here as they pertain to the evaluation board. The full screen block diagram is shown in Figure 4 and Table 4 describes the functionality of each block.

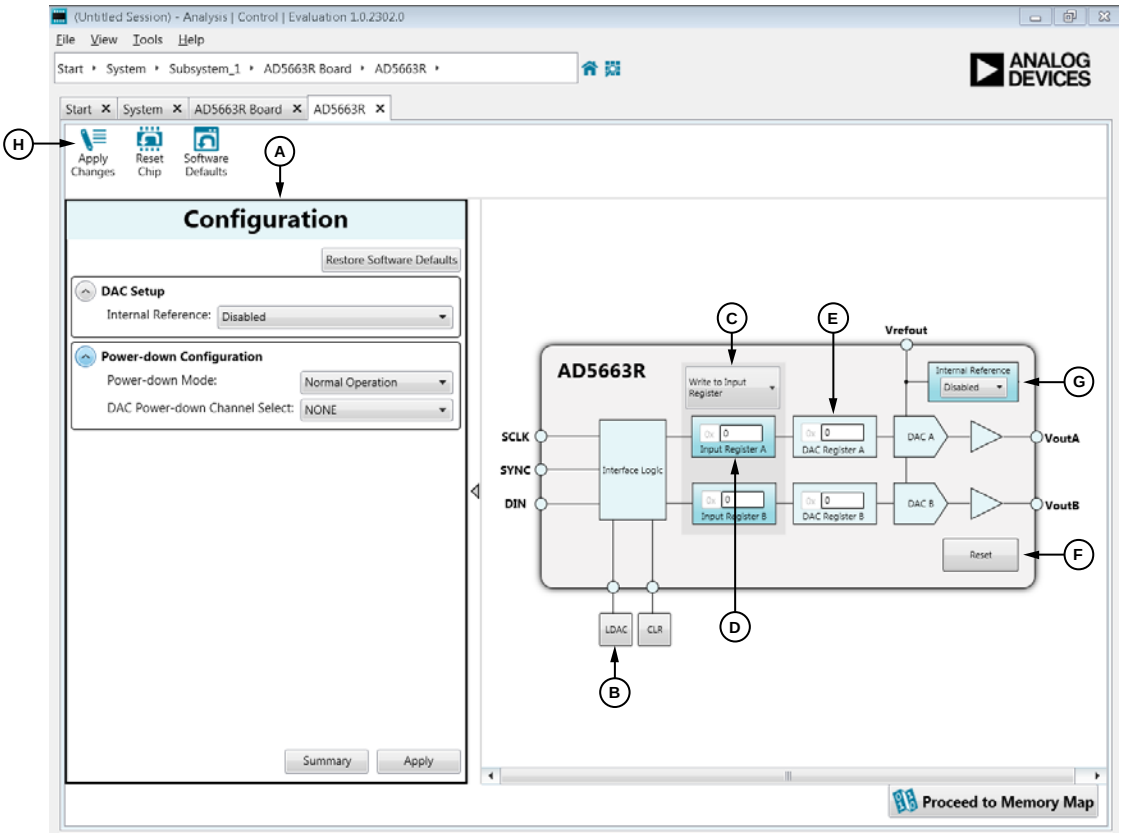


*Figure 4. Block Diagram with Labels*

**Table 4. Block Diagram Functions**

| Label | Function |
|---|---|
| A | Configuration wizard: used to set the initial configuration for the board. From the **DAC Setup** drop-down menu, the internal reference can be enabled or disabled. The reference is disabled as default. From the **Power-Down Mode** drop-down menu, either channel can be configured as normal operation, powered down, or in a high impedance state. After setting up the initial configuration, click **Apply** and the values are applied. These settings can be modified at any stage while testing. |
| B | GPIO buttons: act as external GPIO pulses to the $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ pins. The **LDAC** button pushes data from both input registers (D) to the DAC registers (E). The **CLR** button clears all data from input registers and DAC registers. These buttons are live, so there is no need to click **Apply Changes** (H). |
| C | **Command Option** drop-down menu: selects how the data being transferred to the device affects the input and DAC registers. After a data value is entered in either input register (see D), this menu determine if the data is transferred to the input register only, to the channel input register and channel DAC register (E), or to the channel input register and updates both DAC registers (E). |
| D | Input registers: 16-bit data word to be transferred to the device. Upon clicking the **Apply Changes** (H), this 16-bit data word is transferred to the device. |
| E | DAC registers: inaccessible registers, displays the value that is currently present in the DAC register on the device. The DAC registers can be updated by selecting the appropriate command option or by toggling **LDAC** (B). |
| F | Software reset: soft reset returns the board and software to default values. This button is live, so there is no need to click **Apply Changes**. |
| G | Internal reference: selecting enabled from this setting enables the on-chip reference for the board, if disabled is selected, an external reference must be applied. |
| H | **Apply Changes**: apply all modified values to the device. |

## MEMORY MAP

All registers are fully accessible from the memory map tab; this allows registers to be edited at a bit level. The bits shaded in dark gray are read only bits and cannot be accessed from ACE; all other bits are toggled. **Apply Changes** is used to transfer data to the device. All changes here correspond to the block diagram; for example, if the internal register bit is enabled, it shows as enabled on the block diagram. Any bits or registers that are in bold are modified values that have not been transferred to the board. After **Apply Changes** is clicked, the data is transferred to the board.

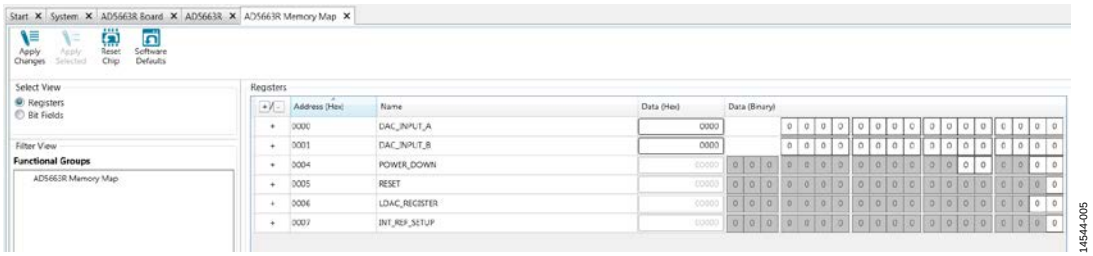


*Figure 5. AD5663R Memory Map*

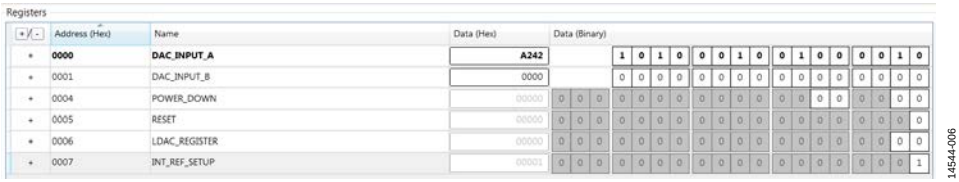


*Figure 6. AD5663R Memory Map with Unapplied Changes in DAC_INPUT_A Register*

# EVALUATION BOARD SCHEMATICS

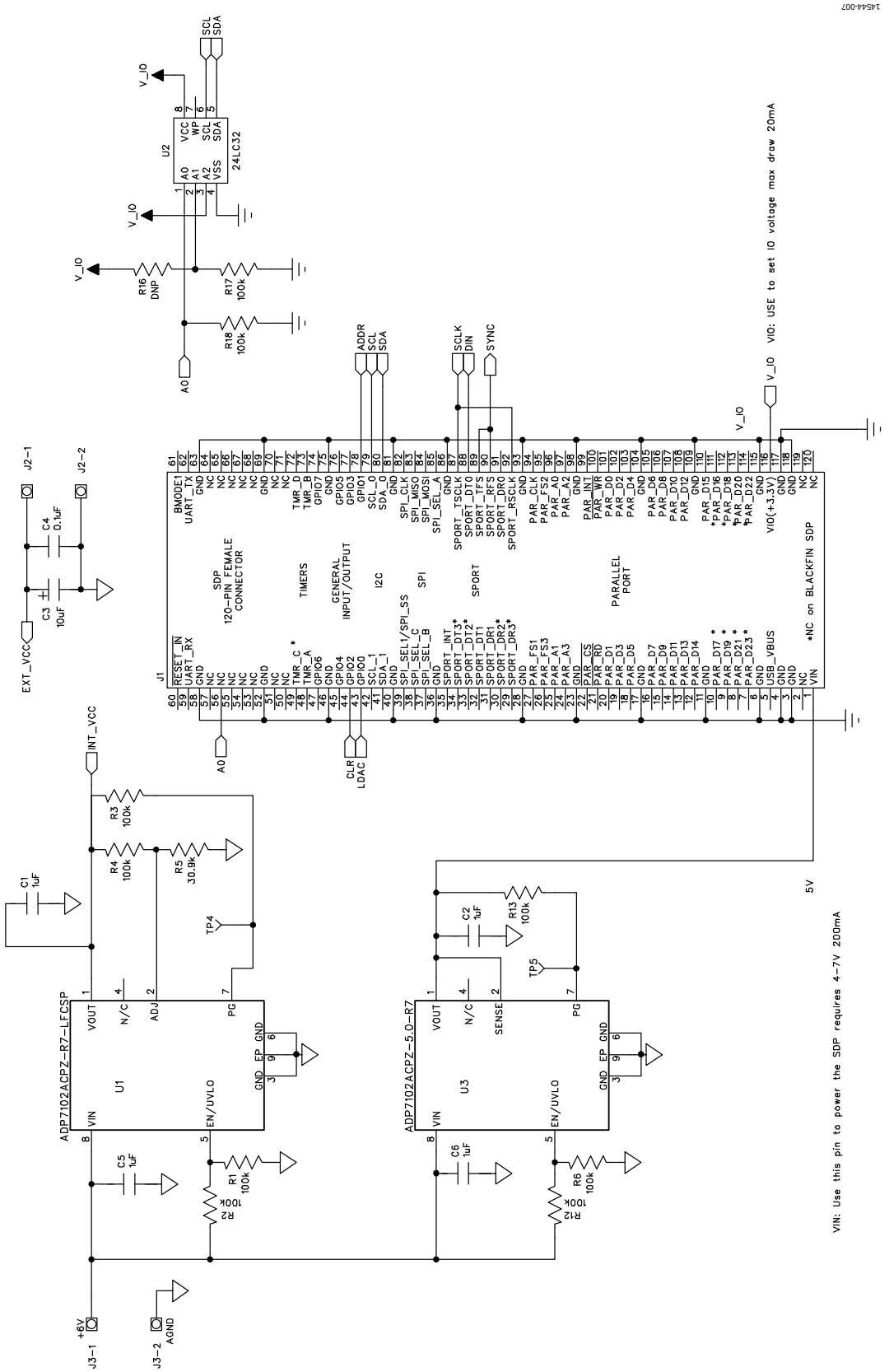


*Figure 7. Interface and Power Evaluation Board Schematics*

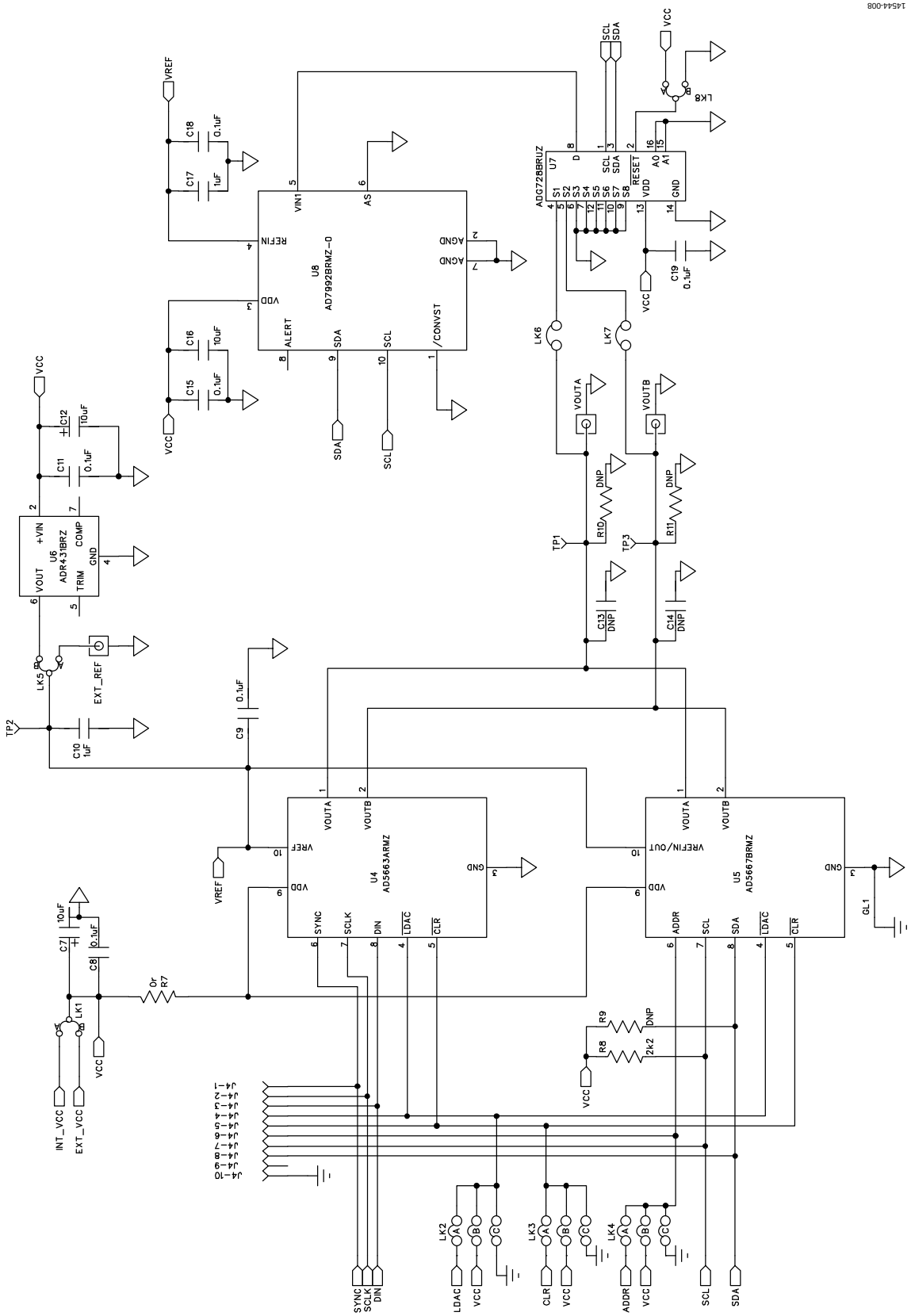


*Figure 8. DAC Circuitry Evaluation Board Schematics*

# ORDERING INFORMATION

## BILL OF MATERIALS

**Table 5.**

| Reference Designator | Value | Part Description |
|---|---|---|
| C1 | 1 µF | Capacitor, 1 µF, 25 V, 0603 |
| C2 | 1 µF | Capacitor, 1 µF, 25 V, 0603 |
| C3 | 10 µF | Capacitor, Case A, 10 µF, 10 V |
| C4 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| C5 | 1 µF | Capacitor, 1 µF, 25 V, 0603 |
| C6 | 1 µF | Capacitor, 1 µF, 25 V, 0603 |
| C7 | 10 µF | Capacitor, Case A, 10 µF, 10 V |
| C8 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| C9 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| C10 | 1 µF | Capacitor, 0603, 1 µF, Y5V, 10 V |
| C11 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| C12 | 10 µF | Capacitor, Case A, 10 µF, 10 V |
| C13 | Not placed | Not applicable |
| C14 | Not placed | Not applicable |
| C15 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| C16 | 1 µF | Capacitor, 0603, 1 µF, Y5V, 10 V |
| C17 | 1 µF | Capacitor, 0603, 1 µF, Y5V, 10 V |
| C18 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| C19 | 0.1 µF | 50 V X7R multilayer ceramic capacitor |
| EXT_REF | Not applicable | Straight printed circuit board mount (PCB) SMB jack, 50 Ω |
| GL1 | Not applicable | Solder short |
| J1 | Not applicable | 120-way female connector, 0.6 mm pitch |
| J2 | Not applicable | 2-pin terminal block (5 mm pitch. |
| J3 | Not applicable | 2-pin terminal block (5 mm pitch) |
| J4 | Not applicable | 10-pin (2 × 5) 0.1" pitch SMT header |
| L1 | 600 Ω at 100 MHz | Ferrite bead |
| LK1 | Not applicable | Jumper block using 3-Pin SIP header |
| LK2 | Not applicable | 6-pin (3 × 2) 0.1" header and shorting block |
| LK3 | Not applicable | 6-pin (3 × 2) 0.1" header and shorting block |
| LK4 | Not applicable | 6-pin (3 × 2) 0.1" header and shorting block |
| LK5 | Not applicable | Jumper block using 3-pin SIP header |
| LK6 | Not applicable | 2-pin (0.1" pitch) header and shorting shunt |
| LK7 | Not applicable | 2-pin (0.1" pitch) header and shorting shunt |
| LK8 | Not applicable | 3-pin (0.1" pitch) header and shorting shunt |
| R1 | 100 kΩ | SMD resistor |
| R2 | 100 kΩ | SMD resistor |
| R3 | 100 kΩ | SMD resistor |
| R4 | 100 kΩ | SMD resistor |
| R5 | 30.9 kΩ | SMD resistor |
| R6 | 100 kΩ | SMD resistor |
| R7 | 0 Ω | Resistor, 0603 1% 0R |
| R8 | Not fitted | SMD resistor 0603 |
| R9 | 2.2 kΩ | SMD resistor, 0.063 W, 1%, 0603 |
| R10 | Not placed | SMD resistor 0603 |
| R11 | Not placed | SMD resistor 0603 |
| R12 | 100 kΩ | SMD resistor |
| R13 | 100 kΩ | SMD resistor |
| R16 | Not placed | SMD resistor |
| R17 | 100 kΩ | SMD resistor |

| Reference Designator | Value | Part Description |
|---|---|---|
| R18 | 100 kΩ | SMD resistor |
| TP1 | Not applicable | Red test point |
| TP2 | Not applicable | Red test point |
| TP3 | Not applicable | Red test point |
| TP4 | Not applicable | Red test point |
| TP5 | Not applicable | Red test point |
| U1 | ADP7102ACPZ-R7 | Linear regulator adjustable, 20 V, 300 mA, ultralow noise, CMOS |
| U2 | 24LC32 | 32 kB I²C serial EEPROM |
| U3 | ADP7102ACPZ-5.0-R7 | LDO 5 V |
| U4 | AD5663RBRMZ-5 | Dual 16-bit *nano*DAC® with SPI interface; only placed on EVAL-AD5663R-SDZ |
| U5 | AD5667RBRMZ-1 | Dual 16- bit *nano*DAC with I²C interface; only placed on EVAL-AD5667R-SDZ |
| U6 | ADR431BRZ | Ultralow noise XFET® voltage reference |
| U7 | ADG728BRUZ | Serial controlled mux |
| U8 | AD7992BRMZ-0 | 12-bit ADC |
| $V_{OUT}A$ | Not applicable | Straight PCB mount SMB jack, 50 Ω |
| $V_{OUT}B$ | Not applicable | Straight PCB mount SMB jack, 50 Ω |

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**
**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



ANALOG DEVICES

www.analog.com