Features

- Utilizes the AVR[®] RISC Architecture
- AVR High-performance and Low-power RISC Architecture
 - 120 Powerful Instructions Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 20 MIPS Throughput at 20 MHz
- Data and Non-volatile Program and Data Memories
 - 2K Bytes of In-System Self Programmable Flash Endurance 10,000 Write/Erase Cycles
 - 128 Bytes In-System Programmable EEPROM Endurance: 100,000 Write/Erase Cycles
 - 128 Bytes Internal SRAM
 - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
 - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
 - One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Modes
 - Four PWM Channels
 - On-chip Analog Comparator
 - Programmable Watchdog Timer with On-chip Oscillator
 - USI Universal Serial Interface
 - Full Duplex USART
- Special Microcontroller Features
 - debugWIRE On-chip Debugging
 - In-System Programmable via SPI Port
 - External and Internal Interrupt Sources
 - Low-power Idle, Power-down, and Standby Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-out Detection Circuit
 - Internal Calibrated Oscillator
- I/O and Packages
 - 18 Programmable I/O Lines
 - 20-pin PDIP, 20-pin SOIC, 20-pad QFN/MLF
- Operating Voltages
 - 1.8 5.5V (ATtiny2313V)
 - 2.7 5.5V (ATtiny2313)
- Speed Grades
 - ATtiny2313V: 0 4 MHz @ 1.8 5.5V, 0 10 MHz @ 2.7 5.5V
 - ATtiny2313: 0 10 MHz @ 2.7 5.5V, 0 20 MHz @ 4.5 5.5V
- Typical Power Consumption
 - Active Mode
 - 1 MHz, 1.8V: 230 μA
 - 32 kHz, 1.8V: 20 µA (including oscillator)
 - Power-down Mode
 - < 0.1 µA at 1.8V

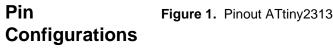


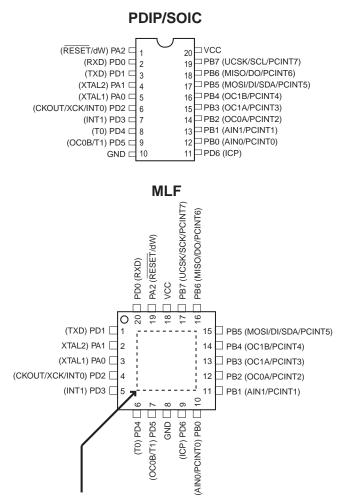
8-bit **AVR**[®] Microcontroller with 2K Bytes In-System Programmable Flash

ATtiny2313/V

Summary







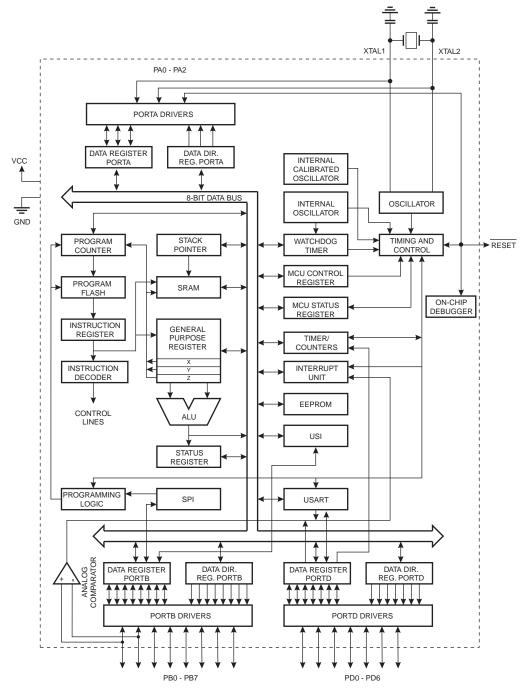
NOTE: Bottom pad should be soldered to ground.

Overview The ATtiny2313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny2313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

² ATtiny2313

Block Diagram









The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny2313 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 18 general purpose I/O lines, 32 general purpose working registers, a single-wire Interface for On-chip Debugging, two flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, or by a conventional non-volatile memory programmer. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny2313 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny2313 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

Pin Descriptions

GND Ground.

Port A (PA2..PA0) Port A is a 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny2313 as listed on page 53.

Port B (PB7..PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny2313 as listed on page 53.

Port D (PD6..PD0) Port D is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATtiny2313 as listed on page 56.

- **RESET** Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 34. Shorter pulses are not guaranteed to generate a reset. The Reset Input is an alternate function for PA2 and dW.
- XTAL1Input to the inverting Oscillator amplifier and input to the internal clock operating circuit. XTAL1
is an alternate function for PA0.
- **XTAL2** Output from the inverting Oscillator amplifier. XTAL2 is an alternate function for PA1.





General Information Resources A comprehensive set of development tools, application notes and datasheets are available for download at http://www.atmel.com/avr. Code Examples This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

Data Retention Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

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Register Summary

abd fields SREs 1 T H S Y N Z C $-$ 0-20 (0x50) SPI SP7 SP9 SP1 SP1<	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
obsit Series Series<	0x3E (0x5E)	SREG	1	т	н	S	V	N	7	C	
Intel Control OCENNE PCR TransControl Compare Registry III PCR IIII 0358 0059 01896 NTT NTTO PCR IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII				-		-	-		_	-	0
DAB (DAB) GAB (SA) INTI INTO PC/E 61 DAB (DAB) TIMBK TOTE1 OCIE1A OCIE1A ICIE OCIE0B TOLE OCIE0B TOLE OCIE0B TOLE OCIE0B TOLE OCIE0B TOLE OCIEA 78 OCIEA 78 OCIEA TOLE OCIEA TOLE OCIEA TOLE OCIEA TOLE OCIEA TOLE TOL			SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
GAA (GAA) EFR NTF1 NTF0 OCT6 OCT6 Image TOTE OCT6	0x3C (0x5C)	OCR0B			1	Fimer/Counter0 –	Compare Registe	er B			77
chaff bessig TMSK TOTEI OCIE M OCIE M <thocie m<="" th=""> OCIE M OCIE</thocie>	0x3B (0x5B)	GIMSK	INT1	INT0	PCIE	-	-	-	-	-	60
Date Boss) TFR TOVI OCFA OCFA C F OFR TOVE OCFA SELFACE T6 Dote Boss) OCRA						-	-	-	-	-	
0x07 SPMCBR 0x0 x CTPB RFIB POWRT POSRS SELPPEGIN 156 0x08 0x08 0x08 MCURR PUD SM1 SE SM0 SGC11 ISC10 ISC11 ISC10 ISC10 ISC11 SGC02 63 0x08 0x08 TCCK98 FOCM POC TmerCounter Regime Regime CS02 CS01 SC00 77 0x08 0x06 OSCAL - Ox06 CS02 CS01 SC00 73 0x01 0x06 OSCAL - Ox06 COM01 COM01 COM01 CM11 COM10 COM01 CM11 CM21 CS13 CS14	· /					-					
Ox80050 CORNA TransControl_Corports Register A. TransControl_Corports Register A. TransControl_Corports Register A. Ox800050 MCURR P.U SN1 SSC 11 SSC 11 SSC 10 SSC 10<	· /										
0x5 0x50 MOUR PUD SM1 SE SM0 ISC11 ISC10 ISC10 <thisc10< th=""> <thisc10< th=""></thisc10<></thisc10<>			-	-					PGERS	SELFPRGEN	
Order (abs.) MCURE IMCURE IMCURE IMCURE IMCURE IMCURE IMCURE IPORF 37 Ob28 (05.5) TCHR8 FORT FCR04 COL13 CAL1 CAL1 CAL1 CAL2 CAL1 CAL2 CAL1 CAL3 CAL2	· /		PLID	SM1					19001	18000	
obs2 CCR0B FOC0A FOC0A <th< td=""><td>· /</td><td></td><td></td><td>-</td><td>-</td><td>-</td><td></td><td></td><td></td><td></td><td></td></th<>	· /			-	-	-					
0x2 (0x5) CTCR10			FOC0A	FOC0B	_	_					
0x00 (059) TCCRAN COMMAI COMMAI COMMED COMBED WGM11 WGM00 73 0x67 (0xF) TCCRAN COMMAI COMMAI COMMED COMBED WGM11 WGM10 104 0x62 (0x40) TCCRAN COMIA COMMAI COMMED COMIA COMMAI COMMAI COMMAI COMMAI COMMAI COMMAI COMIA COMMAI TransCounterI - Inspl Caluer Register Hights Hights 108 1024 109 1024 CUKPSI	0x32 (0x52)			•		Timer/Co	unter0 (8-bit)			•	
OAF (OAF) TOCRIFA COMIA COMIA COMIBO WGM10 104 OAE (OAF) TOCRIFA ICACI ICRSI ICRSI CS12 CS11 CS1	0x31 (0x51)	OSCCAL	-	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	26
odd (over) TCCRHB ICKET IP WMM3 WGM12 CS12 CS10 IOT 0202 (0x0C) TGNTH TTERE/Contret - Counter Register Low Byte 108 026 (0x0C) TGNTH TTERE/Counter 1- Counter Register Low Byte 108 026 (0x0C) CCRNAL TTERE/Counter 1- Counter Register Low Byte 108 026 (0x0C) OCRNAL TTERE/Counter 1- Compare Register Low Byte 109 026 (0x0C) OCRNAL TTERE/Counter 1- Compare Register Low Byte 109 026 (0x0C) OCRNAL TTERE/Counter 1- Compare Register Low Byte 109 026 (0x0C) OCRNAL TTERE/Counter 1- Compare Register Low Byte 109 026 (0x0C) OCRNAL TTERE/Counter 1- Compare Register Low Byte 109 026 (0x0C) ICRNAL TTERE/Counter 1- Compare Register Low Byte 108 026 (0x0C) ICRNAL TTERE/Counter 1- Compare Register Low Byte 108 026 (0x0C) ICRNAL TTERE/Counter 1- Compare Register Low Byte 108 027 (0x1C) TCRNAL TTERE/Counter Low Byte PRNAL PRNAL	0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00	73
bud2 (bxd2) TGNT1L TimerConnert - Conner Register Mg/Bya 108 bud2 (bxd2) OCR1AH TimerConnert - Compare Register AHg/B Bye 108 bud2 (bxd2) OCR1AH TimerConnert - Compare Register AHg/B Bye 108 bud3 (bxd3) OCR1AH TimerConnert - Compare Register A Use Byte 109 bud3 (bxd3) OCR1BL TimerConnert - Compare Register A Use Byte 109 bud3 (bxd3) OCR1BL TimerConnert - Compare Register Aus Byte 109 bud3 (bxd3) OCR1BL TimerConnert - Compare Register Aus Byte 109 bud3 (bxd3) OCR1BL TimerConnert - Compare Register Aus Byte 109 bud3 (bxd3) OCR1BL TimerConnert - Compare Register Aus Byte 109 bud3 (bxd3) OCR1BL TimerConnert - Compare Register Aus Byte 109 bud3 (bxd3) OCR1CR TimerConnert - Compare Register Aus Byte 109 024 bud4 (bxt1) TimerConnert - Compare Register Aus Byte 109 024 020 024 024 024 024 024 024 024 024 024 <t< td=""><td>0x2F (0x4F)</td><td>TCCR1A</td><td>COM1A1</td><td>COM1A0</td><td>COM1B1</td><td>COM1BO</td><td>-</td><td>-</td><td>WGM11</td><td>WGM10</td><td>104</td></t<>	0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1BO	-	-	WGM11	WGM10	104
0x2C (0x4C) TONTIL Timer/Counter1 - Compare Register Alue byte 108 0x2G (0x49) OCR14H Timer/Counter1 - Compare Register Alue byte 109 0x2G (0x49) OCR15H Timer/Counter1 - Compare Register Black byte 109 0x2G (0x49) OCR15H Timer/Counter1 - Compare Register Black byte 109 0x2G (0x40) OCR15H Timer/Counter1 - Ingut Counter 1 - Register Black byte 109 0x2G (0x40) ICR1H Timer/Counter1 - Ingut Counter Register High Byte 109 0x2G (0x40) ICR1H Timer/Counter1 - Ingut Counter Register High Byte 109 0x2G (0x40) ICR1H Timer/Counter1 - Ingut Counter Register High Byte 109 0x2G (0x40) ICR1H Timer/Counter1 - Ingut Counter Register High Byte 109 0x2G (0x40) PCDR4 PCDR5 PCDR4 PCDR4 <td< td=""><td></td><td></td><td>ICNC1</td><td>ICES1</td><td></td><td></td><td></td><td></td><td>CS11</td><td>CS10</td><td></td></td<>			ICNC1	ICES1					CS11	CS10	
0x8 (0x8) OCR14H TimerCounter1 - Compare Register A Hub bys 108 0x8 (0x48) OCR18H TimerCounter1 - Compare Register B Hub byto 109 0x8 (0x48) OCR18L TimerCounter1 - Compare Register B Hub byto 109 0x8 (0x48) OCR18L - 109 0x2 (0x4) 0x1 (0x4)	. ,						* *				
0xA (0xA) OCR18L ThereCounter 1 - Compare Register Blue byte 108 0xB (0x48) OCR18L TimerCounter 1 - Compare Register Blue byte 109 0xB (0x48) OCR18L TimerCounter 1 - Compare Register Blue byte 109 0xB (0x47) Reserved - - - - 0xB (0x48) CLKPR - - - - 0xB (0x48) CLKPR CLKPS CLKPS1 CLKPS0 28 0xB (0x48) LICR1H TimerCounter1 - input Capture Register High Syte 109 104 0x2B (0x43) GTCCR - - - - - 108 0x2B (0x43) GTCCR PCC18 - - - - 108 0x2B (0x40) PDINTP PCINTP	· · · · ·						Ű,	,			
0c20 (0x4) OCR18H Timer/Counter1 - Compare Register Bub Byte 109 0c27 (0x47) Reserved - 109 0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:							, ,	* /			
0263 (0x48) OCK181s. TimerCounter1 - Compare Register Lus Pije 109 0x26 (0x46) CLKPR CLKPCE - 109 0x21 (x4x) WDF	· · · · ·										
0.027 (0x7) Reserved (0x44) - 109 0x23 (0x3) GTOCR - - - - - - - - - 109 0x23 (0x43) GTOCR FOC18 - - - - - - - 108 0x21 (0x41) WDTCSR WDF WDF WDF PCINT5 PCINT4 PCINT3 PCINT3 PCINT3 PCINT3 PCINT3 PCINT3 PCINT3 PCINT4 PORT4 - <td>· /</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>i v</td> <td>0)</td> <td></td> <td></td> <td></td>	· /						i v	0)			
0x68 (0x46) CLKPER CLKPER CLKPER CLKPES CLKPES CLKPES CLKPES CLKPES 28 0x25 (0x45) ICR1H Timer/Counter1 - Input Capture Register Low Byte 109 109 0x24 (0x44) CCR1 — — — — PSR10 81 0x23 (0x43) GTCCR FOC1A FOC1B — — — — PSR10 81 0x22 (0x44) WOTCR FOC1A FOC1B FOLTA PCINTS PCINT			_	_				_	_	_	100
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0x23 (0x42) OTCCR IC FOC1A FOC1B - - - - - PSR10 81 0x22 (0x42) TCCR1C FOC1A FOC1B - - - - - - - - 108 0x21 (0x44) WDTCS WOIF WDIE WDP3 WDC2 WDP1 WDP0 42 0x21 (0x44) PCINT3 <					Timer/	Counter1 - Input (
0x22 (srk2) TCCR1C FOC1A FOC1B - - - - - - - 108 0x21 (sk41) WDTCSR WDIF WDIF WD23 WD2E WD2 WDP1 WDP1 WDP0 42 0x20 (sk40) PCMST6 PCINT5 PCINT6 PCINT6 PCINT6 PCINT1 PCINT0 61 0x16 (sk35) Reserved - PCRMA PORTA - - - PORTA	0x24 (0x44)	ICR1L			Timer/	Counter1 - Input	Capture Register	Low Byte			109
Op21 (0x41) WDFCSR WDIF WDIE WDP3 WDCE WDP2 WDP4 WDP0 42 0x20 (0x40) PCMSK PCINT7 PCINT6 PCINT5 PCINT3 PCINT3 PCINT1 PCINT0 61 0x1F (0x3F) EEAR - PORTA - - - - PORTA PORTB	0x23 (0x43)	GTCCR	-	-	-	-	-	-	-	PSR10	81
0x20 (wd0) PCMSK PCINT7 PCINT6 PCINT5 PCINT4 PCINT3 PCINT2 PCINT1 PCINT0 61 0x1F (0x3F) Resorved - DORA DORA - - - - DORA DORA - - - - DDAA DDAA DDAA DDAA DDAA DDAA DDAB	0x22 (ox42)	TCCR1C	FOC1A	FOC1B	-	-	-	-	-	-	108
Dx1F (bx3F) Reserved - 16 0x1D (0x30) EECR - - - EEPRM0 EERRE EEMPE EERE EERE 17 0x18 (0x38) PORTA - - - - PORTA2 PORTA1 PORTA0 58 0x18 (0x38) PINA - - - - PINA2 PINA1 PINA0 58 0x18 (0x38) PORTB PORTB7 PORTB6 PORTB5 PORTB4 PORTB3 PORTB1 PORTB0 58 0x16 (0x39) GPINB PINB7 PINB6 PINB4 PINB3 PINB3 PINB3 PINB3 PINB3	0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	
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Dx1C (0x3C) EECR - - EEPM1 EEPM0 EERIE EEMPE EEPE EERE 17 0x1B (0x3B) PORTA - - - - PORTA2 PORTA1 PORTA0 58 0x1B (0x3B) DPINA - - - DDA2 DDA1 DDA0 58 0x1B (0x3B) PINA - - - PINA2 PINA1 PINA0 58 0x1B (0x3B) PINA - - - PINB2 PINA1 PINA0 58 0x11B (0x3G) PINB DORTB7 PORTB6 DDB5 DDB4 DDB3 DDB4 DDB3 DDB4 DDB3 DDB1 DDB0 58 0x15 (0x36) GPIOR2 - - - General Purpose UO Register 2 21 21 0x14 (0x34) GPIOR1 - PORTD6 PORTD5 PORTD4 PORTD2 PORTD1 PORTD0 58 0x11 (0x31) DRD -	· · · · ·							egister			
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$\begin{array}{c c c c c c c c c c c c c c c c c c c $	0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	58
Ox14 (0x34) GPIOR1 General Purpose I/O Register 1 21 Ox13 (0x33) GPIOR0 General Purpose I/O Register 0 21 Ox13 (0x33) GPIOR0 PORTD 9 PORTD3 PORTD2 PORTD1 PORTD0 58 Ox11 (0x31) DDR0 - PORTD6 PORTD5 PORTD4 PORTD3 PORTD2 PORTD1 PORTD0 58 0x11 (0x31) DDR0 - PIND6 PIND5 PIND4 PIND3 PIND2 PIND1 PIND0 58 0x0F (0x2F) USIDR - PIND5 PIND4 PIND3 PIND2 PIND1 PIND1 PIND0 58 0x0F (0x2F) USISR USISIF USIOF USIPF USIDC USICNT3 USICNT1 USICNT0 144 0x06 (0x2C) UDR - UART Data Register UART Data Register (8-bit) 129 0x08 (0x28) UCSRA RXC TXC UDRE <t< td=""><td></td><td></td><td>PINB7</td><td>PINB6</td><td>PINB5</td><td>PINB4</td><td>PINB3</td><td>PINB2</td><td>PINB1</td><td>PINB0</td><td></td></t<>			PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	
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Ox07 (0x27) Reserved -			107	1070	100			10:0	1000	40/25	
0x06 (0x26) Reserved -	· /					ACI	ACIE	ACIĆ	ACIS1	ACISO	149
0x05 (0x25) Reserved -				-	-	-	-	-	-	-	
0x04 (0x24) Reserved -	· /			-	-	-	-	-	_		
0x03 (0x23) UCSRC - UMSEL UPM1 UPM0 USBS UCSZ1 UCSZ0 UCPOL 132 0x02 (0x22) UBRRH - - - - UBRRH - 133 0x01 (0x21) DIDR - - - - AIN1D AIN0D 150	· /			_	_	_	_	_	_	_	
0x02 (0x22) UBRRH - - - - UBRRH - 133 0x01 (0x21) DIDR - - - - - AIN1D AIN0D 150				UMSFI	UPM1	UPM0	USBS	UCS71	UCSZ0	UCPOI	132
0x01 (0x21) DIDR AIN1D AIN0D 150	· /						0000			00.02	
			_	_	_	-	-			AIN0D	
			_	-	_	_	_	_			





- Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 - 2. I/O Registers within the address range 0x00 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 - Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
 - 4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses.

ATtiny2313

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND L	OGIC INSTRUCTION	S			
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd ullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \lor K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
BRANCH INSTRUC					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP	ĸ	Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL	ĸ	Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1/2/3
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K		Rd – K		1
SBRC		Compare Register with Immediate		Z, N,V,C,H	1/2/3
	Rr, b	Skip if Bit in Register Cleared	if $(\operatorname{Rr}(b)=0) \operatorname{PC} \leftarrow \operatorname{PC} + 2 \operatorname{or} 3$	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(\text{Rr}(b)=1) \text{PC} \leftarrow \text{PC} + 2 \text{ or } 3$	None	
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1) PC \leftarrow PC + 2 \text{ or } 3$	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC+k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC \leftarrow PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC \leftarrow PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC \leftarrow PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC \leftarrow PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V= 0) then PC \leftarrow PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V= 1) then PC \leftarrow PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC \leftarrow PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC \leftarrow PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC \leftarrow PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC \leftarrow PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC \leftarrow PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC \leftarrow PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC \leftarrow PC + k + 1	None	1/2
BIT AND BIT-TEST	INSTRUCTIONS				
	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
SBI					
SBI CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
	P,b Rd	Clear Bit in I/O Register Logical Shift Left	$I/O(P,b) \leftarrow 0$ Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0	None Z,C,N,V	2
СВІ					





Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=06	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	C ← 1	С	1
CLC		Clear Carry	$C \leftarrow 0$	С	1
SEN		Set Negative Flag	N ← 1	Ν	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	l ← 1	1	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	T ← 1	Т	1
CLT		Clear T in SREG	T ← 0	Т	1
SEH		Set Half Carry Flag in SREG	H ← 1	Н	1
CLH		Clear Half Carry Flag in SREG	H ← 0	Н	1
DATA TRANSFER I	NSTRUCTIONS				
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \operatorname{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$(Z) \leftarrow RI, Z \leftarrow Z + I$ $Z \leftarrow Z - I, (Z) \leftarrow Rr$	None	2
STD	-z, Ri Z+q,Rr		,	None	2
STS		Store Indirect with Displacement Store Direct to SRAM	$(Z + q) \leftarrow Rr$ $(k) \leftarrow Rr$	None	2
LPM	k, Rr				3
	Pd 7	Load Program Memory	$R0 \leftarrow (Z)$	None	-
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack		None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL INS	TRUCTIONS			1	
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK	1	Break	For On-chip Debug Only	None	N/A

ATtiny2313

Ordering Information

Speed (MHz) ⁽³⁾	Power Supply (V)	Ordering Code ⁽⁴⁾	Package ⁽²⁾	Operation Range
10	1.8 - 5.5	ATtiny2313V-10PU ATtiny2313V-10SU ATtiny2313V-10SUR ATtiny2313V-10MU ATtiny2313V-10MUR	20P3 20S 20S 20M1 20M1	Industrial (-40°C to +85°C) ⁽¹⁾
20	2.7 - 5.5	ATtiny2313-20PU ATtiny2313-20SU ATtiny2313-20SUR ATtiny2313-20MU ATtiny2313-20MUR	20P3 20S 20S 20M1 20M1	Industrial (-40°C to +85°C) ⁽¹⁾

Notes: 1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

- 3. For Speed vs. $V_{CC_{\textrm{,}}}$ see Figure 82 on page 180 and Figure 83 on page 180.
- 4. Code Indicators:

U: matte tin

- R: tape & reel

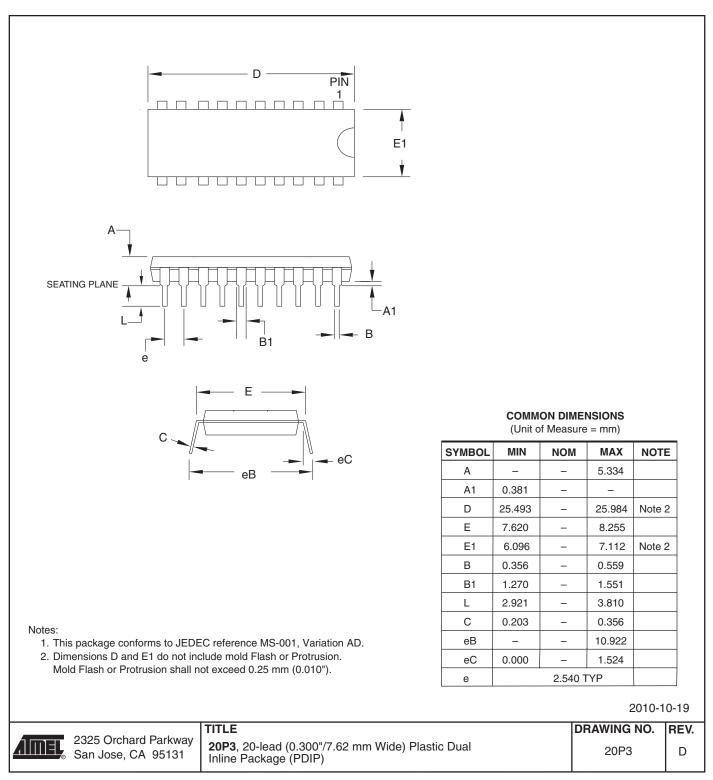
Package Type				
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)			
20S	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)			
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (MLF)			



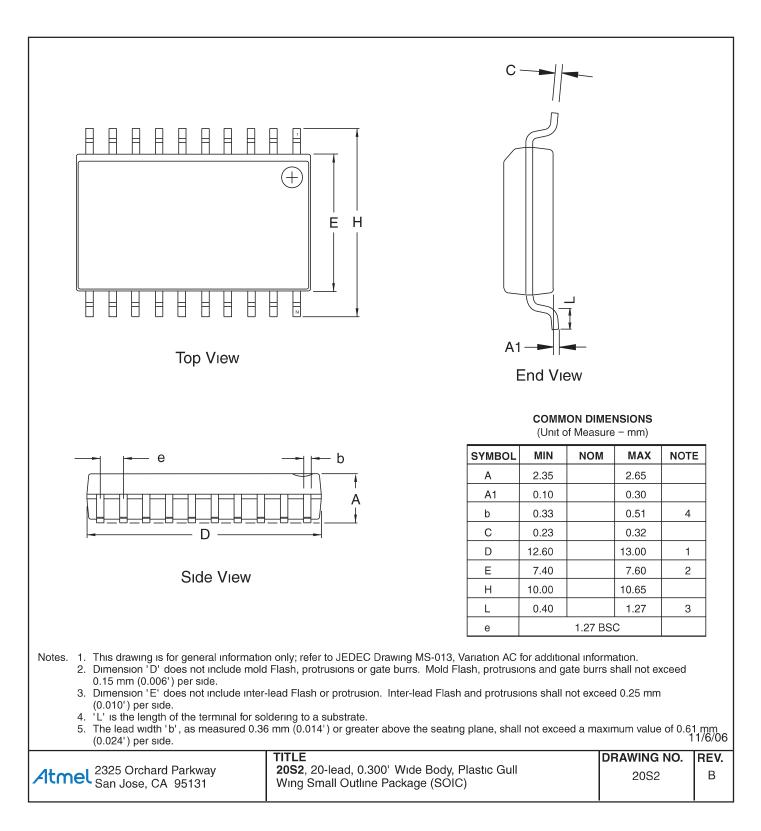


Packaging Information

20P3



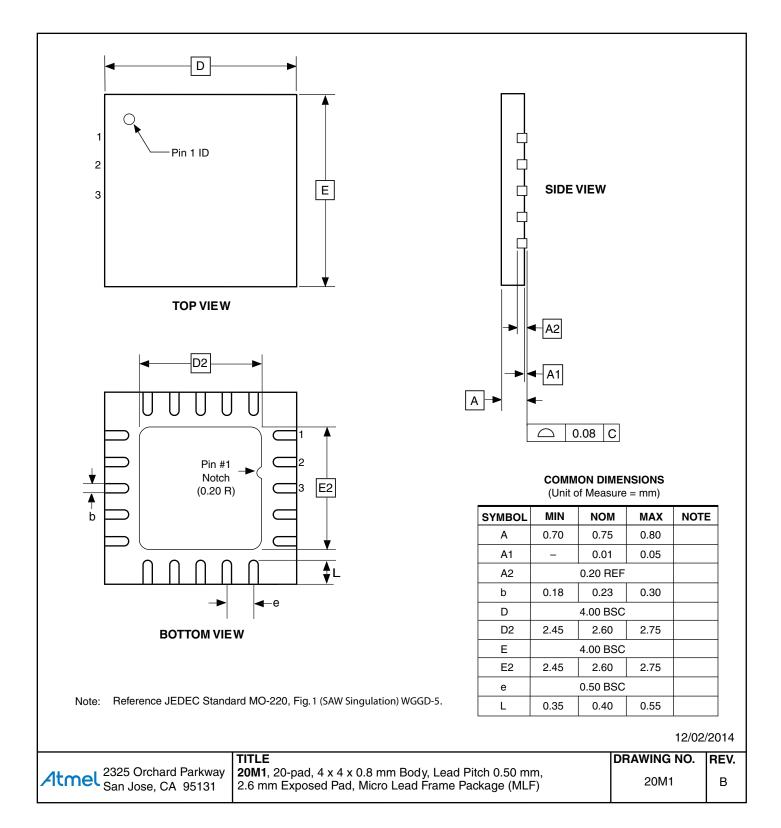
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20M1



Errata The revision in this section refers to the revision of the ATtiny2313 device.

ATtiny2313 Rev C No known errata

ATtiny2313 Rev B

- Wrong values read after Erase Only operation
- Parallel Programming does not work
- Watchdog Timer Interrupt disabled
- EEPROM can not be written below 1.9 volts

1. Wrong values read after Erase Only operation

At supply voltages below 2.7 V, an EEPROM location that is erased by the Erase Only operation may read as programmed (0x00).

Problem Fix/Workaround

If it is necessary to read an EEPROM location after Erase Only, use an Atomic Write operation with 0xFF as data in order to erase a location. In any case, the Write Only operation can be used as intended. Thus no special considerations are needed as long as the erased location is not read before it is programmed.

2. Parallel Programming does not work

Parallel Programming is not functioning correctly. Because of this, reprogramming of the device is impossible if one of the following modes are selected:

- In-System Programming disabled (SPIEN unprogrammed)
- Reset Disabled (RSTDISBL programmed)

Problem Fix/Workaround

Serial Programming is still working correctly. By avoiding the two modes above, the device can be reprogrammed serially.

3. Watchdog Timer Interrupt disabled

If the watchdog timer interrupt flag is not cleared before a new timeout occurs, the watchdog will be disabled, and the interrupt flag will automatically be cleared. This is only applicable in interrupt only mode. If the Watchdog is configured to reset the device in the watchdog timeout following an interrupt, the device works correctly.

Problem fix / Workaround

Make sure there is enough time to always service the first timeout event before a new watchdog timeout occurs. This is done by selecting a long enough time-out period.

4. EEPROM can not be written below 1.9 volts

Writing the EEPROM at V_{CC} below 1.9 volts might fail.

Problem fix / Workaround

Do not write the EEPROM when V_{CC} is below 1.9 volts.

ATtiny2313 Rev A Revision A has not been sampled.





Datasheet Revision History

Refer to the complete datasheet for revision history change log.





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