

## Description

The Atmel® ProChip Designer® v5.0 is a fully featured EDA software suite incorporating state-of-the-art synthesis and simulation tools from Mentor Graphics with the Atmel user-friendly interface and design navigator, as well as, powerful fitter technologies. The combination of these tools enables CPLD designers to achieve the highest possible logic utilization from the Atmel ATF15xxAS/ASL/ASV/ASVL/BE series CPLDs with Logic Doubling® features.

Through all of the software components available within ProChip, the following features are supported:

- Design Entry and Synthesis
  - VHDL
  - Verilog
  - CUPL <sup>(1)</sup>
  - Schematic <sup>(1)</sup>
- Simulation
  - VHDL Functional and Timing Simulation <sup>(2)</sup>
  - Verilog Functional and Timing Simulation <sup>(2)</sup>
  - CUPL Functional Simulation <sup>(1)</sup>
- Device
  - ATF15xxBE: 1.8V ultra-low-power CPLD
  - ATF15xxAS/ASL: 5.0V standard and low-power CPLD
  - ATF15xxASV/ASVL: 3.0V standard and low-power CPLD
- Programming
  - JTAG ISP

1. Optional and requires Altium software.

2. Optional and requires a separate license from Mentor Graphics.

## Features

ProChip Designer seamlessly integrates the following software components into one user-friendly Integrated Development Environment (IDE) for the ATF15xx CPLDs:

ProChip Designer Software Components	
<b>Precision® RTL Synthesis</b> (Atmel-OEM version)	VHDL and Verilog® synthesis supports from Mentor Graphics®.
<b>ModelSim®</b> ( <i>Optional*</i> ) (Atmel-OEM version)	VHDL and Verilog simulation supports from Mentor Graphics. *Requires a separate Mentor Graphics license.
<b>FIT15xx</b>	Fitting support for the ATF15xx CPLDs from Atmel.
<b>HDL Planner</b>	VHDL and Verilog design entry and text editing supports from Atmel.
<b>ATMISP</b>	JTAG In-System programming (ISP) support from Atmel.

The following optional third-party software from Altium® can be installed separately and can be used independently or in conjunction with ProChip Designer for schematic and CUPL® designs:

Optional Third-party Software	
<b>Protel® Design Explorer 99SE</b> (Atmel Edition)	Schematic and CUPL design entries, synthesis, and functional simulation supports from Altium.

# 1. ProChip Designer Software Suite Components and Licensing Terms

The software components within ProChip Designer are divided into two groups:

- Schematic/CUPL Design Flow
- VHDL/Verilog Design Flow

These two software groups, their contents, licensing terms, and ordering code are described in [Table 1-1](#) below.

**Table 1-1. ProChip Designer Contents and Licensing Terms**

Design Flow	Software Components	Licensing Term
Schematic/CUPL Design Flow	ProChip Designer v5.0 with HDL Planner, Atmel Fitter, and ATMISP.	Free
	<a href="#">Altium Design Explorer 99SE.</a>	<a href="#">Permanent License</a> [P/N: ATDS1500PC]
VHDL/Verilog Design Flow	ProChip Designer v5.0 with HDL Planner, Atmel Fitter, and ATMISP.	Free
	<a href="#">Mentor Graphics Precision RTL Synthesis (Atmel-OEM version).</a>	<a href="#">2-year License</a> [P/N: ATDS15xxKSW1]
	<a href="#">Mentor Graphics ModelSim (Atmel-OEM version).</a>	<a href="#">Contact Mentor Graphics</a>

Note: 1. The Atmel software tools are supported on Microsoft® Windows® 2000 and XP operating systems. The details of the operating system supports for other vendors' tools can be obtained from the third-party tool vendors' websites or documentation.

## 1.1 Default Installation of Software Components

By default, the installation of ProChip Designer includes the installation of the following software components:

- HDL Planner
- ATF15xx Fitters
- ATMISP
- Precision RTL Synthesis
- ModelSim



Unlike ProChip Designer v4.0, the installation of Altium tools are no longer included in ProChip Designer v5.0 installer.

*Optionally*, Protel Design Explorer 99SE can be installed separately, and it can be used independently or in conjunction with ProChip Designer v5.0 for schematic and CUPL designs.

## 1.2 Software Component Licensing

### 1.2.1 Mentor Graphics Precision RTL Synthesis

To use Mentor Graphics Precision RTL Synthesis in ProChip Designer v5.0 for VHDL or Verilog synthesis, a FLEXLM (node locked) license file from Atmel is required. License requests can be submitted to Atmel for evaluation on-line at the following URL:

<http://www.atmel.com/System/BaseForm.aspx?target=tcm:26-17233>

The 2-year license for Precision RTL Synthesis (Atmel OEM version) can also be purchased from an Atmel distributor.

**Table 1-2. Mentor Graphics Precision RTL Synthesis License**

2-year License	Atmel Ordering Code
Precision RTL Synthesis (Atmel OEM version)	ATDS15xxKSW1

Once a license has been purchased, a ProChip Designer v5.0 software CD along with instructions on how to obtain the license file will be mailed.



Atmel no longer provides licenses for the Mentor Graphics ModelSim software.

Please contact Mentor Graphics for information on how to obtain the appropriate license for ModelSim if VHDL/Verilog simulation is required.

### 1.2.2 Altium Protel Design Explorer 99SE

The 30-day trial version of Altium Protel Design Explorer 99SE is no longer available, and the Licensed Edition of Altium Protel Design Explorer 99SE *must* be ordered separately.

The Atmel Licensed Edition of Altium Protel Design Explorer 99SE can be ordered from an Atmel distributor and the Atmel.

**Table 1-3. Altium Protel Design Explorer 99SE License**

Permanent License	Atmel Ordering Code
Altium Protel Design Explorer 99SE	ATDS1500PC

Once a license has been purchased, a ProChip Designer v5.0 software CD along with the 16-digit Access Code will be mailed. Users can then follow the instructions provided to install the Licensed Edition software.

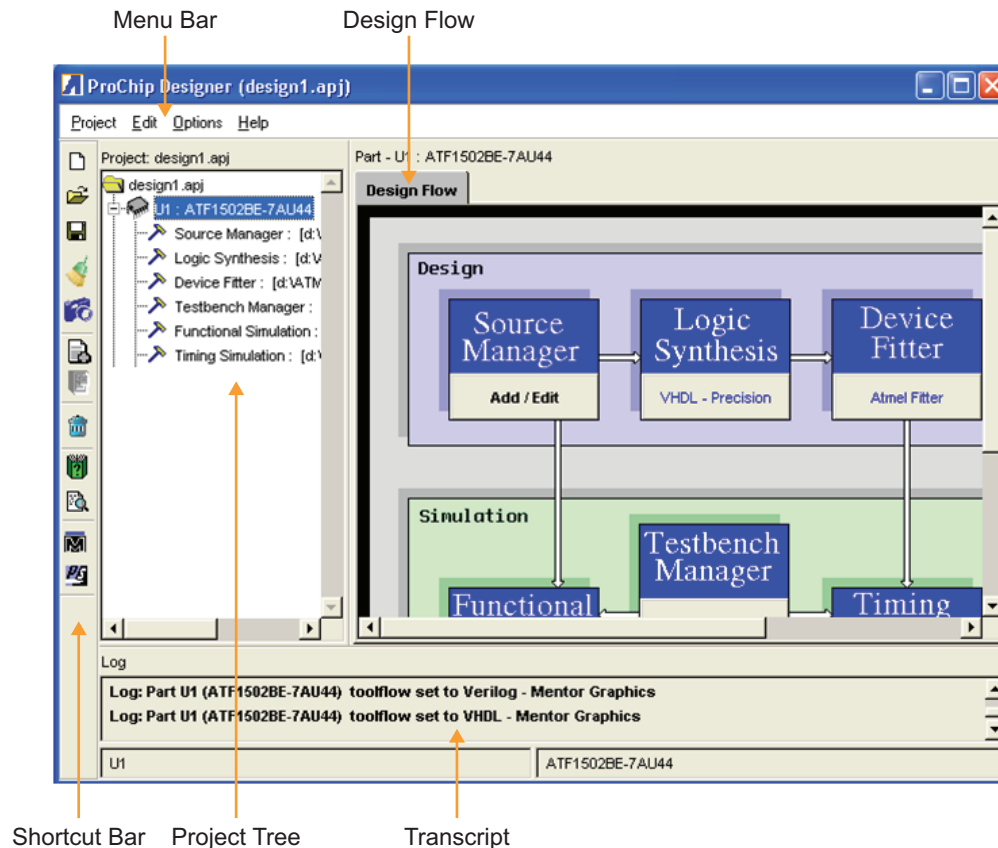
The ProChip Designer v5.0 software is available on the ProChip Designer v5.0 Software CD as well as on the Atmel website at the following URL:

[http://www.atmel.com/tools/PROCHIPDESIGNERV5\\_0.aspx](http://www.atmel.com/tools/PROCHIPDESIGNERV5_0.aspx)

## 2. Design Flow

The ProChip Designer v5.0 IDE is shown in [Figure 2-1](#). The *Design Flow* chart on the right provides push-button access to all stages of a design cycle. Feature descriptions for each design flow stage is described in [Table 2-1](#).

**Figure 2-1. ProChip Designer v5.0 IDE**



**Table 2-1. Description of Design Flow Stages**

Design Flow Stage	Description
Source Manager	To specify new or existing design file(s). Launches the appropriate design entry tool for editing based on the selected tool-flow.
Logic Synthesis	To synthesize the design file(s) to generate the appropriate netlist file.
Device Fitter	To fit the netlist into the target device with the user selected fitter options.
Testbench Manager	To specify new or existing testbench file(s). Launches the appropriate testbench entry tool for editing based on the selected tool-flow.
Functional Simulation	To perform functional simulation on the design file(s).
Timing Simulation	To perform timing simulation on the output netlist generated by the fitter after fitting.
Atmel-ISP	To program the target ATF15xx CPLD through JTAG-ISP.

### 3. Support and Resources

For details on how to use ProChip Designer, refer to the ProChip Designer help file, tutorials, and online resources. These resources are available under the ProChip **Help** menu.

**Table 3-1. Technical Support**

Request Support By:	
Email	<a href="mailto:pld@atmel.com">pld@atmel.com</a>
Hotline	(+1) (408) 436-4333
Online Support Form	<a href="http://support.atmel.com/bin/customer.exe">http://support.atmel.com/bin/customer.exe</a>
Product Information	<a href="http://www.atmel.com/products/other/spld-cpld/default.aspx">http://www.atmel.com/products/other/spld-cpld/default.aspx</a>

### 4. Revision History

Rev. Ver.	Date	Description
3628C	09/2013	General update of the overview document. Update template.

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