



ATF15xx CPLD JTAG ISP Download Cable

USER GUIDE

Introduction

The Atmel® ATF15xx Complex Programmable Logic Device (CPLD) LPT-based JTAG ISP Download Cable [Atmel PN: ATDH1150VPC] connects to a standard parallel port of a PC on one side and to a 10-pin JTAG header of a programming circuit board on the other side. It transfers the JTAG instructions and data generated by the ATMISP software running on a PC to the Atmel ATF15xx series CPLDs on the target circuit board. The ATMISP software can be downloaded from the Atmel website at http://www.atmel.com/tools/ATMISP.aspx. With this In-System Programming (ISP) download cable, design changes can easily be downloaded directly to the ATF15xx JTAG devices, resulting in easy prototyping of designs.

Features

- Supports Industry Standard IEEE 1149.1 (JTAG) Compliant Devices
- Allows Users to Perform JTAG ISP of Atmel ATF15xx CPLDs
- Supports Target Systems Using 5.0V, 3.3V, 2.5V or 1.8V V_{CC} and I/O Standards
- Fully Supported by the ATMISP Software (Version 6.x)
- Interfaces with a Standard DB25 Parallel Port of PC
- Uses a Standard 10-pin JTAG Connector

Supports

The ATDH1150VPC ISP Download Cable (Rev 6.0) supports all of the ATF15xx CPLDs with JTAG support.

Table of Contents

Functional Description	3
Ordering Information	Ę
Frequently Asked Questions	6
Гесhnical Support	7
Revision History	7



Functional Description

The ATDH1150VPC ISP Download Cable connects to a standard PC parallel port (LPT) on one side and to a 10-pin JTAG header on the programming circuit board on the other side. A functional block diagram of the ATDH1150VPC ISP Download Cable is shown in the below figure, and Table 1 provides the signal descriptions.

Figure 1. ATF15xx JTAG ISP Download Cable Functional Block Diagram

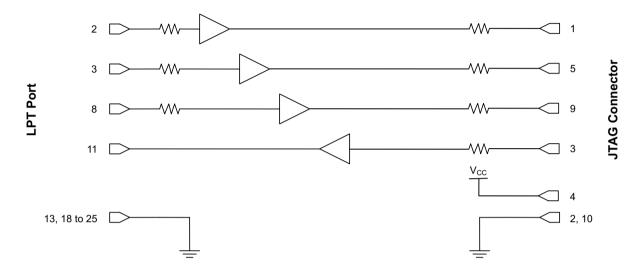


Table 1. 10-pin JTAG Header Signal Description

Pin	Signal Name	Description
1	TCK	JTAG Clock Signal
2	GND	Ground from Target System
3	TDO	JTAG Data Output Signal
4	V _{CC}	Power Supply from Target System
5	TMS	JTAG State Machine Control Signal
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	TDI	JTAG Data Input Signal
10	GND	Ground from Target System

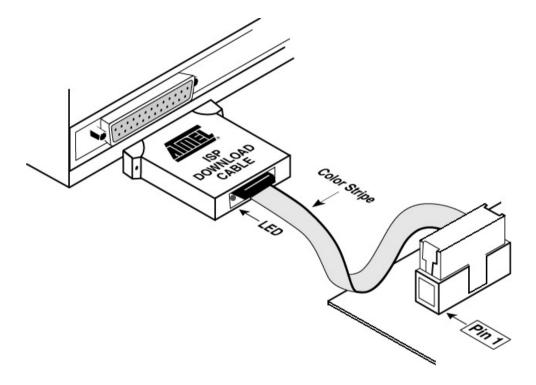


The ISP circuit board must supply V_{CC} and GND to the ATDH1150VPC ISP Download Cable through the 10-pin JTAG male header. A regulated V_{CC} voltage between 1.7V to 5.5V is recommended, and it should be the same V_{CC} supply used by the JTAG devices.



The Power LED on the 10-pin male connector can be used to show the cable is connected properly. The user must make sure this LED is turned on before using the ATMISP software to program the JTAG devices. The color stripe on ATDH1150VPC ISP Download Cable indicates the orientation of Pin 1 of the JTAG connector. The color stripe or the polarized connector can be used as a guide to assure that the female connector is properly oriented when it is attached to the board. This cable has built-in circuitry to adjust its programming voltage level according to the V_{CC} applied to the cable via Pin 4 of the 10-pin JTAG connector. The following figure illustrates the correct orientation of ATDH1150VPC ISP Download Cable on the programming circuit side.

Figure 2. Connection Diagram of ATF15xx JTAG ISP Cable



The below figure illustrates the pinout of the 10-pin female header on the ATDH1150VPC ISP Download Cable. The pinout of the 10-pin male header on the PC board must match this pinout.

Figure 3. ATDH1150VPC ISP Download Cable 10-pin Female Header Pinout

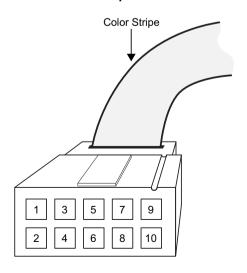




Figure 4 illustrates the dimensions for the 10-pin male header which is mounted on ISP board. Figure 5 illustrates the pinout for the 10-pin male header.

Figure 4. 10-pin Male Header Dimensions

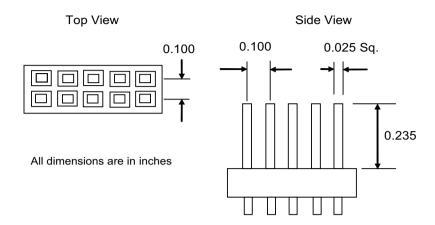
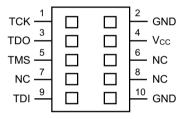


Figure 5. 10-pin Male Header Pinout



Ordering Information

The ATDH1150VPC ISP Download Cable (Rev 6.0) is included in the ATF15xx-DK3 Atmel ATF15xx CPLD Development/Programmer kit or it can be purchased separately.

Table 2. Atmel CPLD Kits Ordering Information

Part Number	Description
ATDH1150VPC	Atmel ATF15xx CPLD LPT-based JTAG ISP Download Cable
ATF15xx-DK3	Atmel ATF15xx CPLD Development/Programmer Kit



Frequently Asked Questions



For a multiple device JTAG hardware chain, which device is considered the first device (Device #1) when setting up the Atmel CPLD ISP (ATMISP) software?

The device with its TDI pin connected to the TDI pin of the 10-pin JTAG header is the first device (Device #1) of a JTAG chain. The device with its TDO pin connected to the TDO pin of the 10-pin JTAG header is the last device of the chain.



For devices with different $V_{cc}INT$ and $V_{cc}IO$ supplies, which V_{cc} ($V_{cc}IO$ or $V_{cc}INT$) should be used to supply the ATDH1150VPC ISP Download Cable's V_{cc} ?

 $V_{CC}IO$ should be used to supply the V_{CC} of the ATDH1150VPC ISP Download Cable.



Can a JEDEC file with the JTAG port feature disabled be programmed into the ATF15xx through JTAG ISP?

Since all ATF15xx devices are shipped in a blank (erased) state, the JTAG port is enabled by default. Therefore, they can be programmed with a JEDEC file with the JTAG port feature disabled ONLY ONCE via JTAG ISP. However, this is not recommended since the pins used for the JTAG port can become outputs immediately after programming is completed and they can content with the output drivers in the ATDH1150VPC ISP Download Cable. Furthermore, please note that once the JTAG port is disabled, the device can no longer be accessed through the JTAG port. To re-enable the JTAG port, you must erase the device or reprogram the device with a JEDEC file with the JTAG port feature enabled using a standalone 3rd-party device programmer from vendors such as BPM Microsystems, Data I/O, Hi-Lo Systems,. etc.



In the Port Setting dialog box of the ATMISP v6.x software window, what LPT port addresses are associated to the LPT1, LPT2 and LPT3 settings?

LPT1 - 378 (hex), LPT2 - 278 (hex), LPT3 - 3BC (hex).



The LPT port address of my PC is 1AFF (hex). How do I specify this address in the ATMISP software?

From the main ATMISP window, select Other in the Port Setting dialog box. In the Port Setting window, enter 1AFF and click OK. Any 3 or 4-digit hex values can be entered into this window.



Technical Support

For Atmel PLD technical support, please contact the Atmel PLD Applications Group at:

Phone: +1 (408) 436-4333 Email: pld@atmel.com

Online: http://support.atmel.com/bin/customer.exe

Revision History

Doc. Rev.	Date	Comments
8907A	03/2014	Initial document release.













Atmel Corporation

1600 Technology Drive, San Jose, CA 95110 USA

T: (+1)(408) 441.0311

F: (+1)(408) 436.4200

www.atmel.com

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