CY7C1440KV33
CY7C1442KV33
CY7C1440KVE33

36-Mbit (1M × 36/2M × 18) Pipelined Sync SRAM (With ECC)

Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250 MHz and 167 MHz
- Registered inputs and outputs for pipelined operation
- 3.3 V core power supply
- 2.5 V or 3.3 V I/O power supply
- Fast clock-to-output time
  - 2.5 ns (for 250 MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Single cycle chip deselect
- CY7C1440KV33, CY7C1442KV33 and CY7C1440KVE33 are available in Pb-free 100-pin TQFP, and Pb-free and non Pb-free 165-ball FBGA packages.
- IEEE 1149.1 JTAG-compatible boundary scan
- “ZZ” sleep mode option
- On-Chip error correction code (ECC) to reduce soft error rate (SER)

Functional Description

The CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 SRAM integrate 1M × 36/2M × 18/1M × 36 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{\text{CE}}_1$), depth-expansion chip enables (CE_2 and $\overline{\text{CE}}_3$), burst control inputs ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$, and $\overline{\text{ADV}}$), write enables ($\overline{\text{BW}}_X$ and $\overline{\text{BWE}}$), and global write ($\overline{\text{GW}}$). Asynchronous inputs include the output enable ($\overline{\text{OE}}$) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ($\overline{\text{ADSP}}$) or address strobe controller ($\overline{\text{ADSC}}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{\text{ADV}}$).

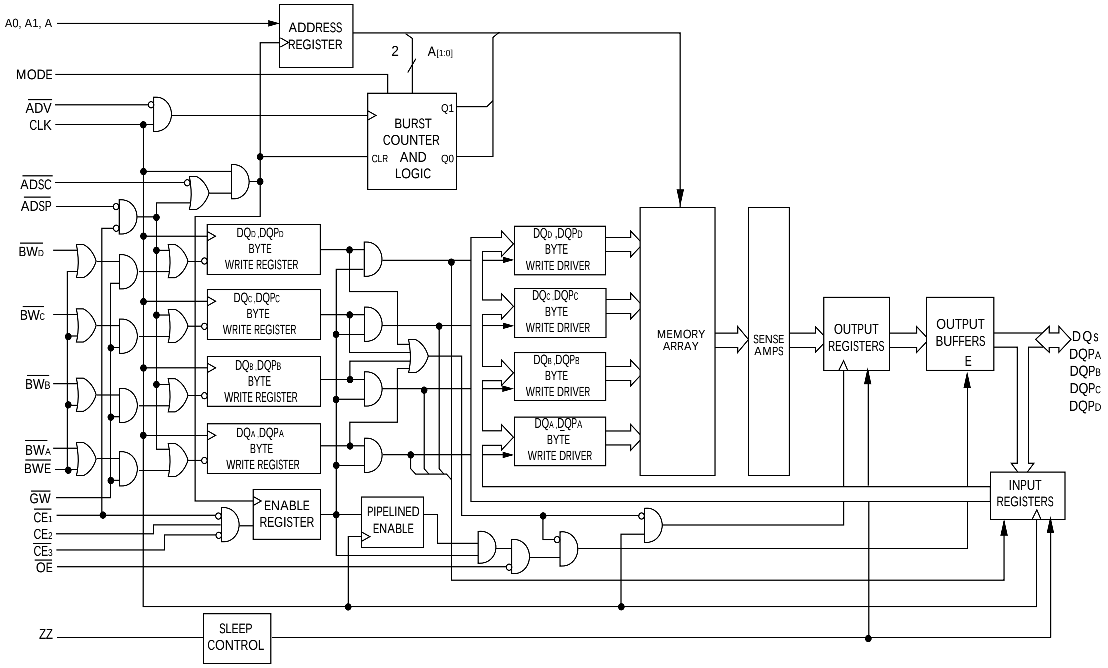
Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle. This part supports byte write operations (see pin descriptions and truth table for further details). Write cycles can be one, two or four bytes wide as controlled by the byte write control inputs. $\overline{\text{GW}}$ when active LOW causes all bytes to be written.

The CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 operate from a +3.3 V core power supply while all outputs may operate with either a +2.5 V or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

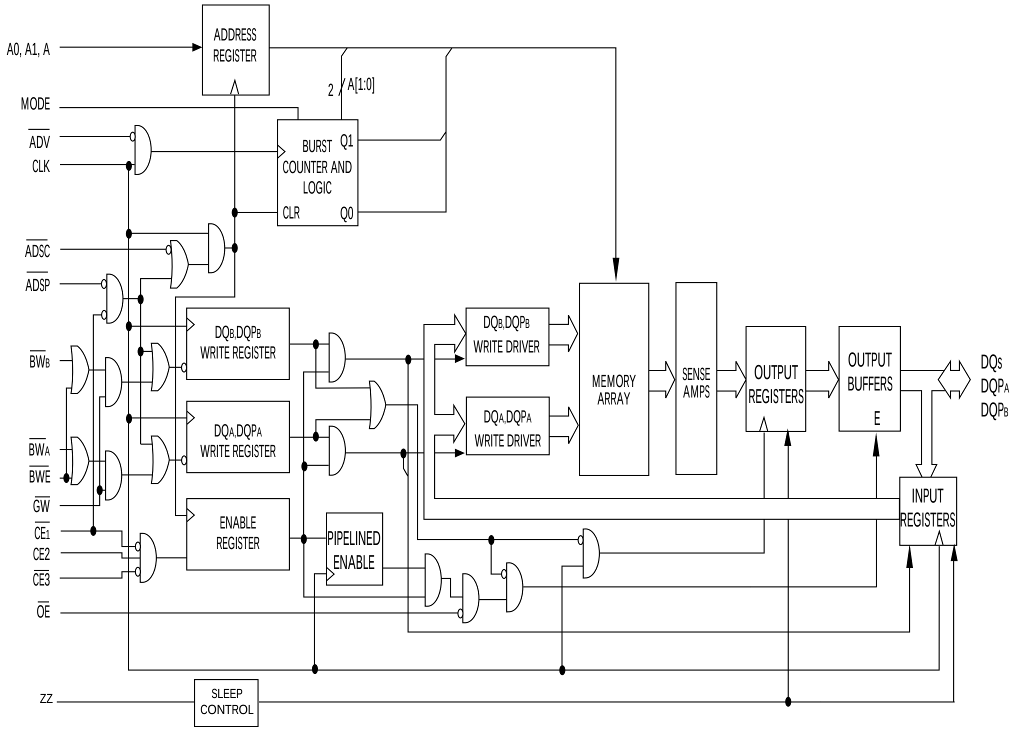
Selection Guide

Description		250 MHz	167 MHz	Unit
Maximum access time		2.5	3.4	ns
Maximum operating current	× 18	220	Not Offered	mA
	× 36	240	190	

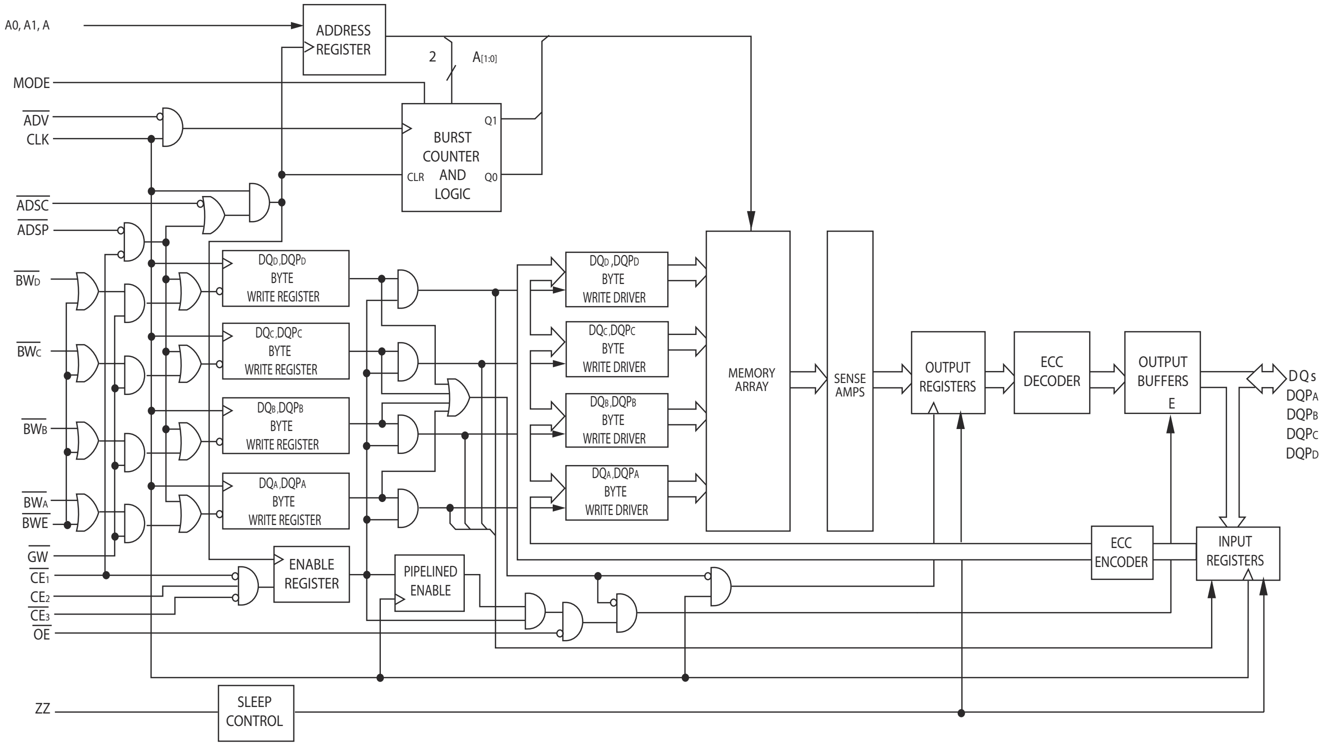
Logic Block Diagram – CY7C1440KV33



Logic Block Diagram – CY7C1442KV33



Logic Block Diagram – CY7C1440KVE33



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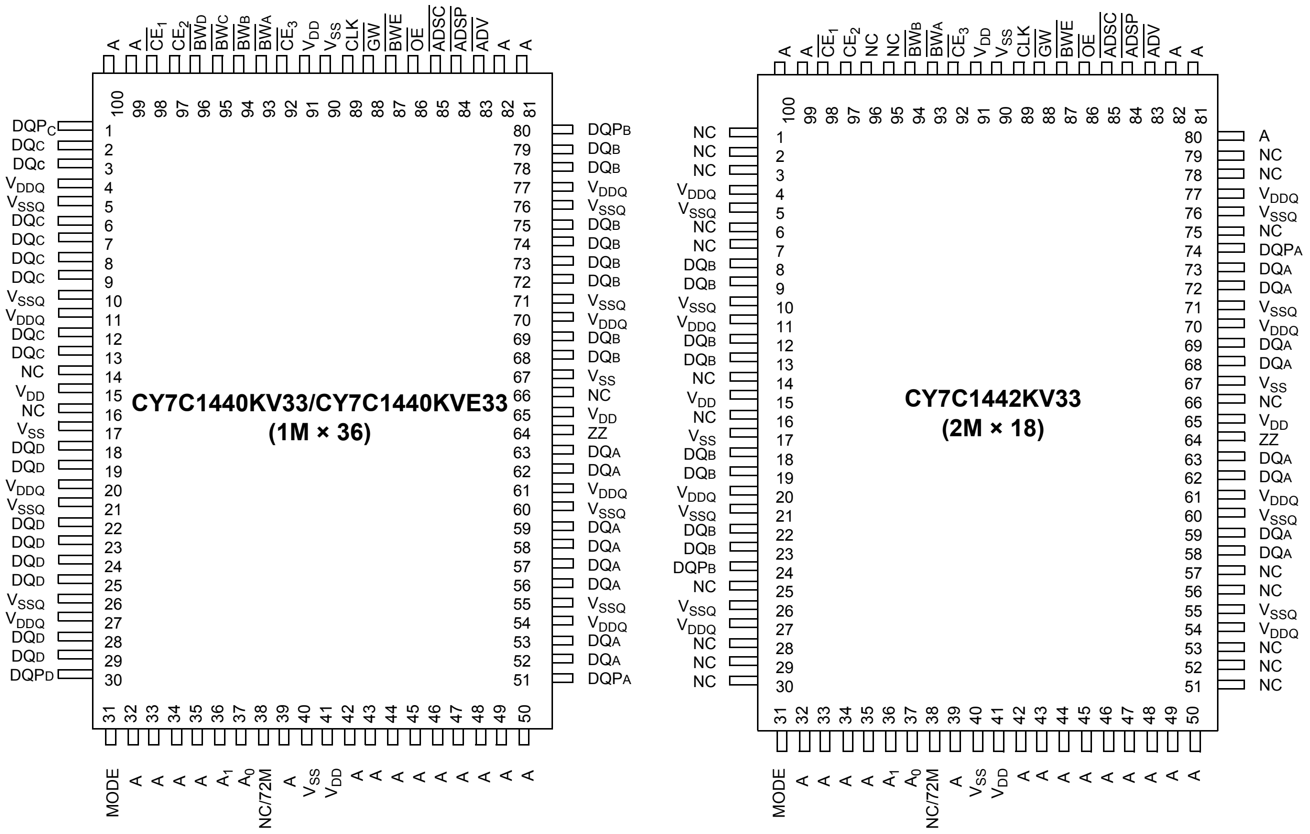
Pin Configurations

Figure 1. 100-pin TQFP Pinout



Pin Configurations *(continued)*

Figure 2. 165-ball FBGA Pinout

CY7C1440KV33 (1M × 36)

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
A	NC/288M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
B	NC/144M	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	NC/576M
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC/1G	DQP_B
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	DQP_A
P	NC	NC/72M	A	A	TDI	A1	TDO	A	A	A	A
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the address locations**. Sampled at the rising edge of the CLK if $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is active LOW, and $\overline{\text{CE}}_1$, CE_2, and $\overline{\text{CE}}_3$[1]are sampled active. A1: A0 are fed to the two-bit counter.
$\overline{\text{BW}}_A$, $\overline{\text{BW}}_B$, $\overline{\text{BW}}_C$, $\overline{\text{BW}}_D$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{\text{BWE}}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{\text{GW}}$	Input-synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on BW_X and $\overline{\text{BWE}}$).
$\overline{\text{BWE}}$	Input-synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{\text{ADV}}$ is asserted LOW, during a burst operation.
$\overline{\text{CE}}_1$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{\text{CE}}_3$ to select/deselect the device. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CE}}_1$ is HIGH. $\overline{\text{CE}}_1$ is sampled only when a new external address is loaded.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{\text{CE}}_3$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{\text{CE}}_1$ and CE_2 to select/deselect the device. Not available for AJ package version. Not connected for BGA. Where referenced, $\overline{\text{CE}}_3$ is assumed active throughout this document for BGA. $\overline{\text{CE}}_3$ is sampled only when a new external address is loaded.
$\overline{\text{OE}}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{\text{OE}}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{\text{ADV}}$	Input-synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{\text{ADSP}}$	Input-synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized. $\overline{\text{ASDP}}$ is ignored when $\overline{\text{CE}}_1$ is deasserted HIGH.
$\overline{\text{ADSC}}$	Input-synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1: A0 are also loaded into the burst counter. When $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ are both asserted, only $\overline{\text{ADSP}}$ is recognized.
ZZ	Input-asynchronous	**ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQs, DQP_X	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the read cycle. The direction of the pins is controlled by $\overline{\text{OE}}$. When $\overline{\text{OE}}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP_X are placed in a tri-state condition.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.

Note
1. X = "Don't Care." H = Logic HIGH, L = Logic LOW.

Pin Definitions *(continued)*

Name	I/O	Description
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O ground	**Ground for the I/O circuitry**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
MODE	Input-static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
TDO	JTAG serial output synchronous	**Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. If the JTAG feature is not being utilized, this pin should be disconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TMS	JTAG serial input synchronous	**Serial data-in to the JTAG circuit**. Sampled on the rising edge of TCK. If the JTAG feature is not being utilized, this pin can be disconnected or connected to V_{DD}. This pin is not available on TQFP packages.
TCK	JTAG-clock	**Clock input to the JTAG circuitry**. If the JTAG feature is not being utilized, this pin must be connected to V_{SS}. This pin is not available on TQFP packages.
NC	–	**No connects**. Not internally connected to the die.
NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No connects**. Not internally connected to the die. NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.5 ns (250-MHz device).

The CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 support secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium processors. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{\text{ADSP}}$) or the controller address strobe ($\overline{\text{ADSC}}$). Address advancement through the burst sequence is controlled by the $\overline{\text{ADV}}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{\text{BWE}}$) and byte write select ($\overline{\text{BW}}_X$) inputs. A global write enable ($\overline{\text{GW}}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous chip selects ($\overline{\text{CE}}_1$, CE_2, $\overline{\text{CE}}_3$) and an asynchronous output enable ($\overline{\text{OE}}$) provide for easy bank selection and output tri-state control. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CE}}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is asserted LOW, (2) $\overline{\text{CE}}_1$, CE_2, $\overline{\text{CE}}_3$ are all asserted active, and (3) the write signals ($\overline{\text{GW}}$, $\overline{\text{BWE}}$) are all deserted HIGH. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CE}}_1$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 2.5 ns (250-MHz device) if $\overline{\text{OE}}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{\text{OE}}$ signal. Consecutive single Read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ signals, its output will tri-state immediately.

Single Write Accesses Initiated by $\overline{\text{ADSP}}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{\text{ADSP}}$ is asserted LOW, and (2) $\overline{\text{CE}}_1$, CE_2, $\overline{\text{CE}}_3$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The write signals ($\overline{\text{GW}}$, $\overline{\text{BWE}}$, and $\overline{\text{BW}}_X$) and $\overline{\text{ADV}}$ inputs are ignored during this first cycle.

ADSP-triggered write accesses require two clock cycles to complete. If GW is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If GW is HIGH, then the write operation is controlled by BWE and BW_X signals.

The CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 provide byte write capability that is described in the Write Cycle Descriptions table. Asserting the byte write enable input (BWE) with the selected byte write (BW_X) input, will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the write operations.

Because CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 are common I/O devices, the output enable (OE) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by ADSC

ADSC Write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deserted HIGH, (3) CE_1, CE_2, CE_3 are all asserted active, and (4) the appropriate combination of the Write inputs (GW, BWE, and BW_X) are asserted active to conduct a Write to the desired byte(s). ADSC-triggered write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The ADV input is ignored during this cycle. If a global Write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the Write operations.

Because CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 are common I/O devices, the output enable (OE) must be deasserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 provide a two-bit wraparound counter, fed by A1: A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The burst sequence is user selectable through the MODE input. Asserting ADV LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. CE_1, CE_2, CE_3, ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

On-Chip ECC

CY7C1440KVE33 SRAMs include an on-chip ECC algorithm that detects and corrects all single-bit memory errors, including Soft Error Upset (SEU) events induced by cosmic rays, alpha particles etc. The resulting Soft Error Rate (SER) of these devices is anticipated to be <0.01 FITs/Mb a 4-order-of-magnitude improvement over comparable SRAMs with no On-Chip ECC, which typically have an SER of 200 FITs/Mb or more. To protect the internal data, ECC parity bits (invisible to the user) are used.

The ECC algorithm does not correct multi-bit errors. However, Cypress SRAMs are architected in such a way that a single SER event has a very low probability of causing a multi-bit error across any data word. The extreme rarity of multi-bit errors results in a SER of <0.01 FITs/Mb.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2$ V	–	75	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2$ V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33 is as follows [2, 3, 4, 5, 6, 7].

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L–H	Tri-state
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
READ cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
READ cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-state
WRITE cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L–H	D
READ cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
READ cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-state
READ cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
READ cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-state
READ cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
READ cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-state
WRITE cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
WRITE cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
READ cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
READ cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-state
READ cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
READ cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-state
WRITE cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
WRITE cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes

2. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more byte write enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are available only in the TQFP package. BGA package has only 2 chip selects $\overline{CE_1}$ and CE_2.
6. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1440KV33/CY7C1440KVE33 is as follows. [8, 9, 10]

Function (CY7C1440KV33/CY7C1440KVE33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – (DQ_A and DQP_A)	H	L	H	H	H	L
Write byte B – (DQ_B and DQP_B)	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C – (DQ_C and DQP_C)	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D – (DQ_D and DQP_D)	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Partial Truth Table for Read/Write

The partial truth table for read/write for CY7C1442KV33 is as follows. [8, 9, 10]

Function (CY7C1442KV33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ_A and DQP_A)	H	L	H	L
Write byte B – (DQ_B and DQP_B)	H	L	L	H
Write bytes B, A	H	L	L	L
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

Notes

8. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
9. BW_x represents any byte write signal. To enable any byte write BW_x, a Logic LOW signal should be applied at clock rise. Any number of bye writes can be enabled at the same time for any given write.
10. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write will be done based on which byte write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1440KV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with IEEE Standard 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1440KV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see TAP Controller Block Diagram on page 15).

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see TAP Controller State Diagram on page 15).

Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 15. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order on page 19 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions on page 18.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in this section.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a high Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the clock captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required – that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

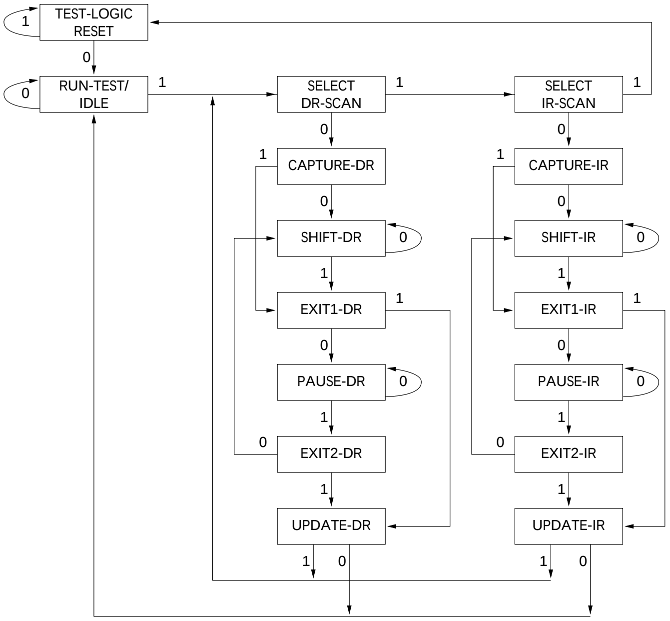
The boundary scan register has a special bit located at, bit #89 (for 165-ball FBGA package). When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the “Update-DR” state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a high Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR”, the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

Reserved

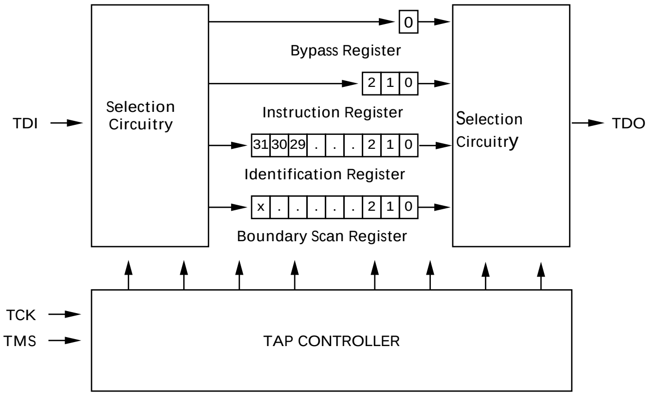
These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Controller State Diagram

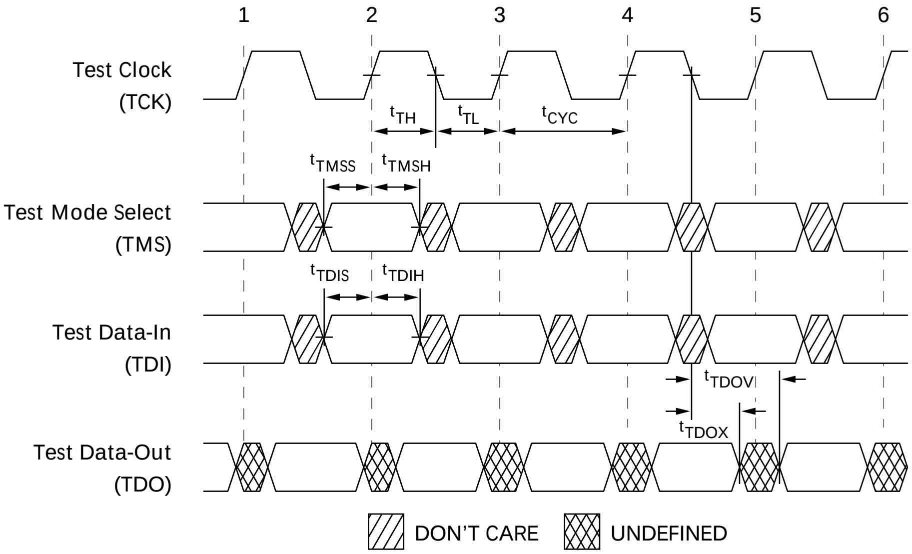


The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Timing



TAP AC Switching Characteristics

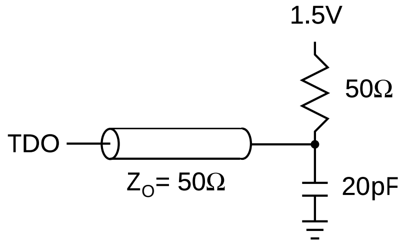
Over the operating Range

Parameter [11, 12]	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK clock cycle time	50	–	ns
t_{TF}	TCK clock frequency	–	20	MHz
t_{TH}	TCK clock HIGH time	20	–	ns
t_{TL}	TCK clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK clock LOW to TDO valid	–	10	ns
t_{TDOX}	TCK clock LOW to TDO invalid	0	–	ns
Set-up Times				
t_{TMSS}	TMS set-up to TCK clock rise	5	–	ns
t_{TDIS}	TDI set-up to TCK clock rise	5	–	ns
t_{CS}	Capture set-up to TCK rise	5	–	ns
Hold Times				
t_{TMSH}	TMS hold after TCK clock rise	5	–	ns
t_{TDIH}	TDI hold after clock rise	5	–	ns
t_{CH}	Capture hold after clock rise	5	–	ns

3.3 V TAP AC Test Conditions

Input pulse levels ....V_{SS} to 3.3 V
Input rise and fall times (Slew Rate) .... 2 V/ns
Input timing reference levels ....1.5 V
Output reference levels ....1.5 V
Test load termination supply voltage ....1.5 V

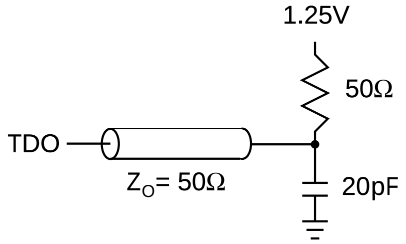
3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Test Conditions

Input pulse levels ....V_{SS} to 2.5 V
Input rise and fall times (Slew Rate) .... 2 V/ns
Input timing reference levels ....1.25 V
Output reference levels ....1.25 V
Test load termination supply voltage ....1.25 V

2.5 V TAP AC Output Load Equivalent



Notes

11. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
12. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 2 V/ns (Slew Rate).

TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T_A < +70 °C; V_{DD} = 3.135 to 3.6 V unless otherwise noted)

Parameter [13]	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3 V		2.4	–	V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5 V		2.0	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3 V	2.9	–	V
			V_{DDQ} = 2.5 V	2.1	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3 V	–	0.4	V
		I_{OL} = 1.0 mA	V_{DDQ} = 2.5 V	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3 V	–	0.2	V
			V_{DDQ} = 2.5 V	–	0.2	V
V_{IH}	Input HIGH voltage	–	V_{DDQ} = 3.3 V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage	–	V_{DDQ} = 3.3 V	–0.3	0.8	V
			V_{DDQ} = 2.5 V	–0.3	0.7	V
I_X	Input load current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Note

[13] All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1440KV33 (1M × 36)	Description
Revision number (31:29)	000	Describes the version number.
Device depth (28:24)[14]	01011	Reserved for internal use.
Architecture/memory type (23:18)	000000	Defines memory type and architecture.
Bus width/density(17:12)	100111	Defines width and density.
Cypress JEDEC ID code (11:1)	00000110100	Allows unique identification of SRAM vendor.
ID register presence indicator (0)	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size (× 36)
Instruction	3
Bypass	1
ID	32
Boundary scan order (165-ball FBGA package)	89

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the I/O ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note

[14] Bit #24 is “1” in the ID Register Definitions for both 2.5 V and 3.3 V versions of this device.

Boundary Scan Order

165-ball FBGA [15, 16]

CY7C1440KV33 (1M × 36)

Bit #	Ball ID
1	N6
2	N7
3	N10
4	P11
5	P8
6	R8
7	R9
8	P9
9	P10
10	R10
11	R11
12	H11
13	N11
14	M11
15	L11
16	K11
17	J11
18	M10
19	L10
20	K10
21	J10
22	H9
23	H10
24	G11
25	F11
26	E11
27	D11
28	G10
29	F10
30	E10
31	D10
32	C11
33	A11
34	B11
35	A10
36	B10
37	A9
38	B9
39	C10
40	A8
41	B8
42	A7
43	B7
44	B6
45	A6
46	B5
47	A5
48	A4
49	B4
50	B3
51	A3
52	A2
53	B2
54	C2
55	B1
56	A1
57	C1
58	D1
59	E1
60	F1
61	G1
62	D2
63	E2
64	F2
65	G2
66	H1
67	H3
68	J1
69	K1
70	L1
71	M1
72	J2
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

Notes

[15] Balls that are NC (No Connect) are preset LOW.

[16] Bit# 89 is preset HIGH.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND ....–0.3 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ...... –0.3 V to +V_{DD}

DC voltage applied to outputs in tri-state ....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage ....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) .... > 2001 V

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU (Device without ECC)	Logical Single-Bit Upsets	25 °C	<5	5	FIT/ Mb
LSBU (Device with ECC)			0	0.01	FIT/ Mb
LMBU (All Devices)	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/ Mb
SEL (All Devices)	Single Event Latch up	85 °C	0	0.1	FIT/ Dev

* *No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN54908 “Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates”.

Electrical Characteristics

Over the Operating Range

Parameter [17, 18]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage	–	3.135	3.6	V
V_{DDQ}	I/O supply voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA	2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA	2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA	–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage[17]	for 3.3 V I/O	2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O	1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage[17]	for 3.3 V I/O	–0.3	0.8	V
		for 2.5 V I/O	–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND $\le V_I \le V_{DDQ}$	–5	5	µA
	Input current of MODE	Input = V_{SS}	–30	–	µA
		Input = V_{DD}	–	5	µA
	Input current of ZZ	Input = V_{SS}	–5	–	µA
		Input = V_{DD}	–	30	µA
I_{OZ}	Output leakage current	GND $\le V_I \le V_{DDQ,}$ output disabled	-5	5	µA

Notes

[17] Overshoot: $V_{IH}(AC) < V_{DD}$ + 1.5 V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2$ V (Pulse width less than $t_{CYC}/2$).

[18] $T_{Power\text{-}up}$: Assumes a linear ramp from 0 V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [17, 18]	**Description**	**Test Conditions**			**Min**	**Max**	**Unit**
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz	× 18	–	220	mA
				× 36	–	240	
			6-ns cycle, 167 MHz	× 36	–	190	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz	× 18	–	85	mA
				× 36	–	90	
			6-ns cycle, 167 MHz	× 36	–	90	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = 0	All speeds	× 18	–	75	mA
				× 36	–	80	
I_{SB3}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, $V_{IN} \leq 0.3$ V or $V_{IN} \geq V_{DDQ} - 0.3$ V, f = f_{MAX} = $1/t_{CYC}$	4-ns cycle, 250 MHz	× 18	–	85	mA
				× 36		90	
			6-ns cycle, 167 MHz	× 36	–	90	mA
I_{SB4}	Automatic CE Power-down Current – TTL Inputs	V_{DD} = Max, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speeds	×18	–	75	mA
				× 36	–	80	

Capacitance

Parameter [19]	Description	Test Conditions	100-pin TQFP Max	165-ball FBGA Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	5	pF
C_{CLK}	Clock input capacitance		5	5	pF
$C_{I/O}$	Input/output capacitance		5	5	pF

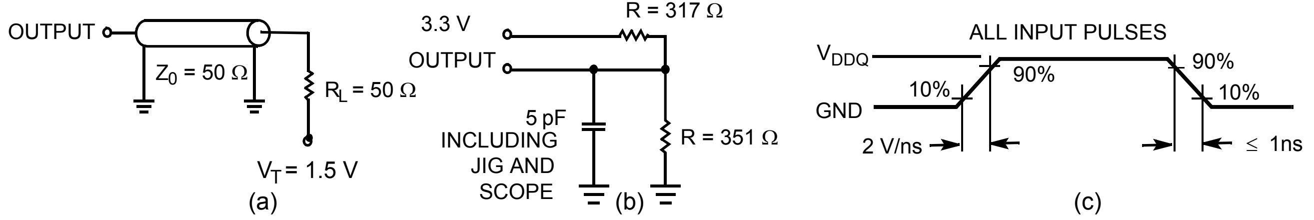
Thermal Resistance

Parameter [19]	Description	Test Conditions		100-pin TQFP Package	165-ball FBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	With Still Air (0 m/s)	35.36	14.24	°C/W
			With Air Flow (1 m/s)	31.30	12.47	°C/W
			With Air Flow (3 m/s)	28.86	11.40	°C/W
Θ_{JC}	Thermal resistance (junction to case)		–	7.52	3.92	°C/W
Θ_{JB}	Thermal resistance (junction to board)			28.89	7.19	°C/W

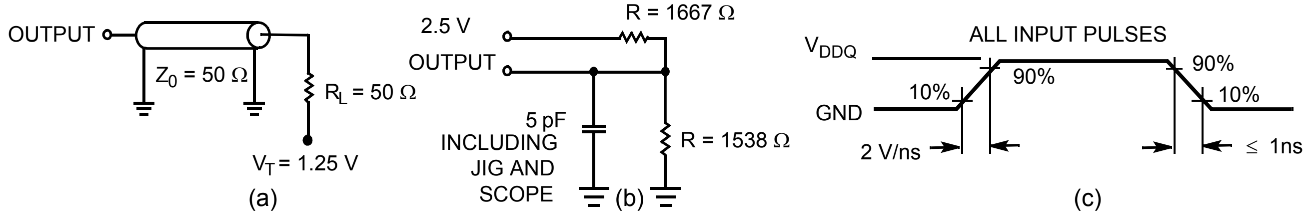
AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Note

[19] Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [20, 21]	Description	–250		–167		Unit
		Min	Max	Min	Max	
t_{POWER}	V_{DD}(Typical) to the first access[22]	1	–	1	–	ms
Clock						
t_{CYC}	Clock cycle time	4.0	–	6	–	ns
t_{CH}	Clock HIGH	1.5	–	2.4	–	ns
t_{CL}	Clock LOW	1.5	–	2.4	–	ns
Output Times						
t_{CO}	Data output valid after CLK rise	–	2.5	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.0	–	1.5	–	ns
t_{CLZ}	Clock to low Z[23, 24, 25]	1.0	–	1.5	–	ns
t_{CHZ}	Clock to high Z[23, 24, 25]	–	2.6	–	3.4	ns
t_{OEV}	$\overline{\text{OE}}$ LOW to output valid	–	2.6	–	3.4	ns
t_{OELZ}	$\overline{\text{OE}}$ LOW to output low Z[23, 24, 25]	0	–	0	–	ns
t_{OEHZ}	$\overline{\text{OE}}$ HIGH to output high Z[23, 24, 25]	–	2.6	–	3.4	ns
Set-up Times						
t_{AS}	Address set-up before CLK rise	1.2	–	1.5	–	ns
t_{ADS}	$\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$ set-up before CLK rise	1.2	–	1.5	–	ns
t_{ADVS}	$\overline{\text{ADV}}$ set-up before CLK rise	1.2	–	1.5	–	ns
t_{WES}	$\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_X$ set-up before CLK rise	1.2	–	1.5	–	ns
t_{DS}	Data input set-up before CLK rise	1.2	–	1.5	–	ns
t_{CES}	Chip enable set-up before CLK rise	1.2	–	1.5	–	ns
Hold Times						
t_{AH}	Address hold after CLK rise	0.3	–	0.5	–	ns
t_{ADH}	$\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ hold after CLK rise	0.3	–	0.5	–	ns
t_{ADVH}	$\overline{\text{ADV}}$ hold after CLK rise	0.3	–	0.5	–	ns
t_{WEH}	$\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_X$ hold after CLK rise	0.3	–	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.3	–	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.3	–	0.5	–	ns

Notes

[20] Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.

[21] Test conditions shown in (a) of AC Test Loads unless otherwise noted.

[22] This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD}(minimum) initially before a read or write operation can be initiated.

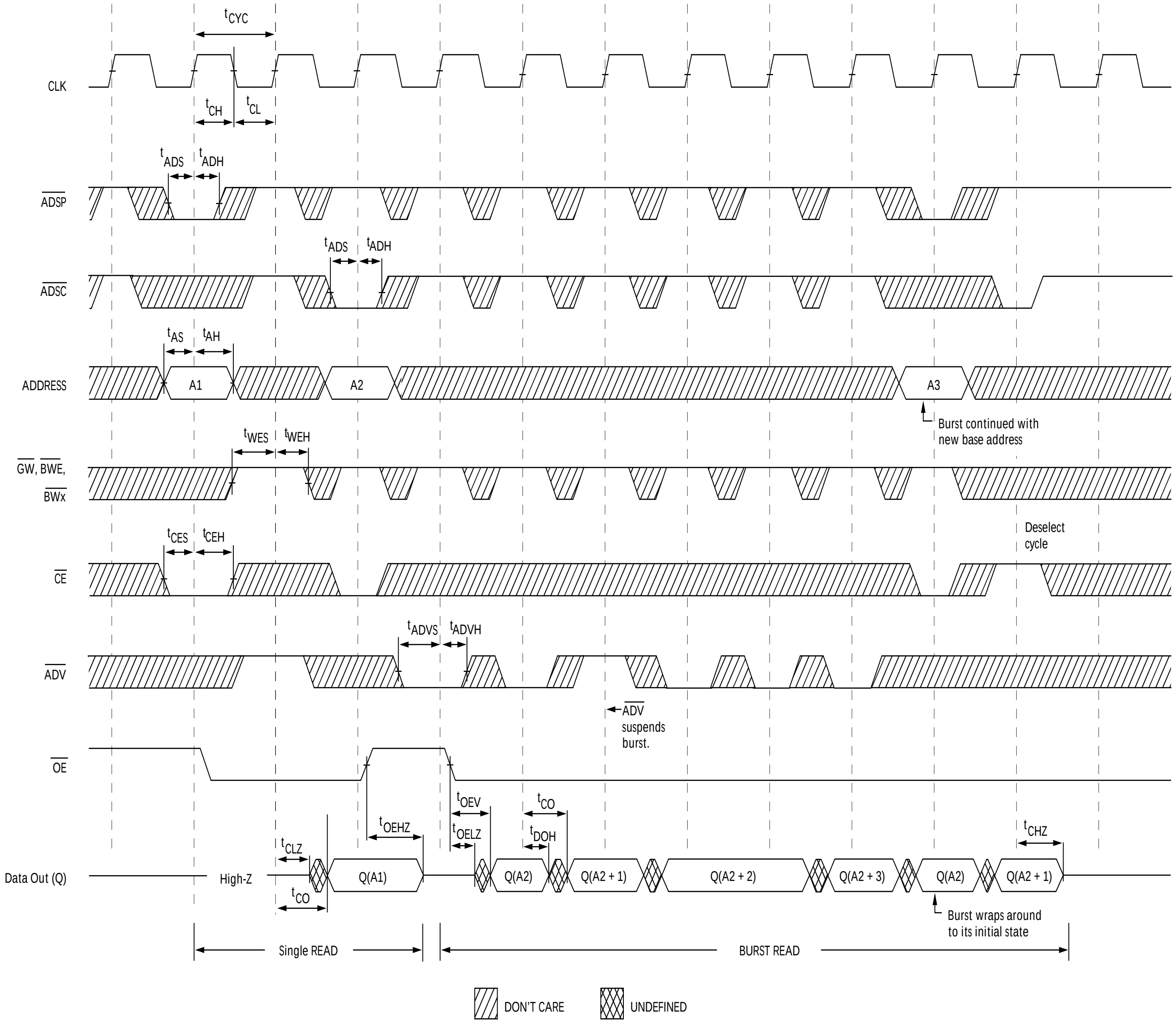
[23] t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in (b) of Figure 3 on page 22. Transition is measured ± 200 mV from steady-state voltage.

[24] At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

[25] This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 4. Read Cycle Timing [26]

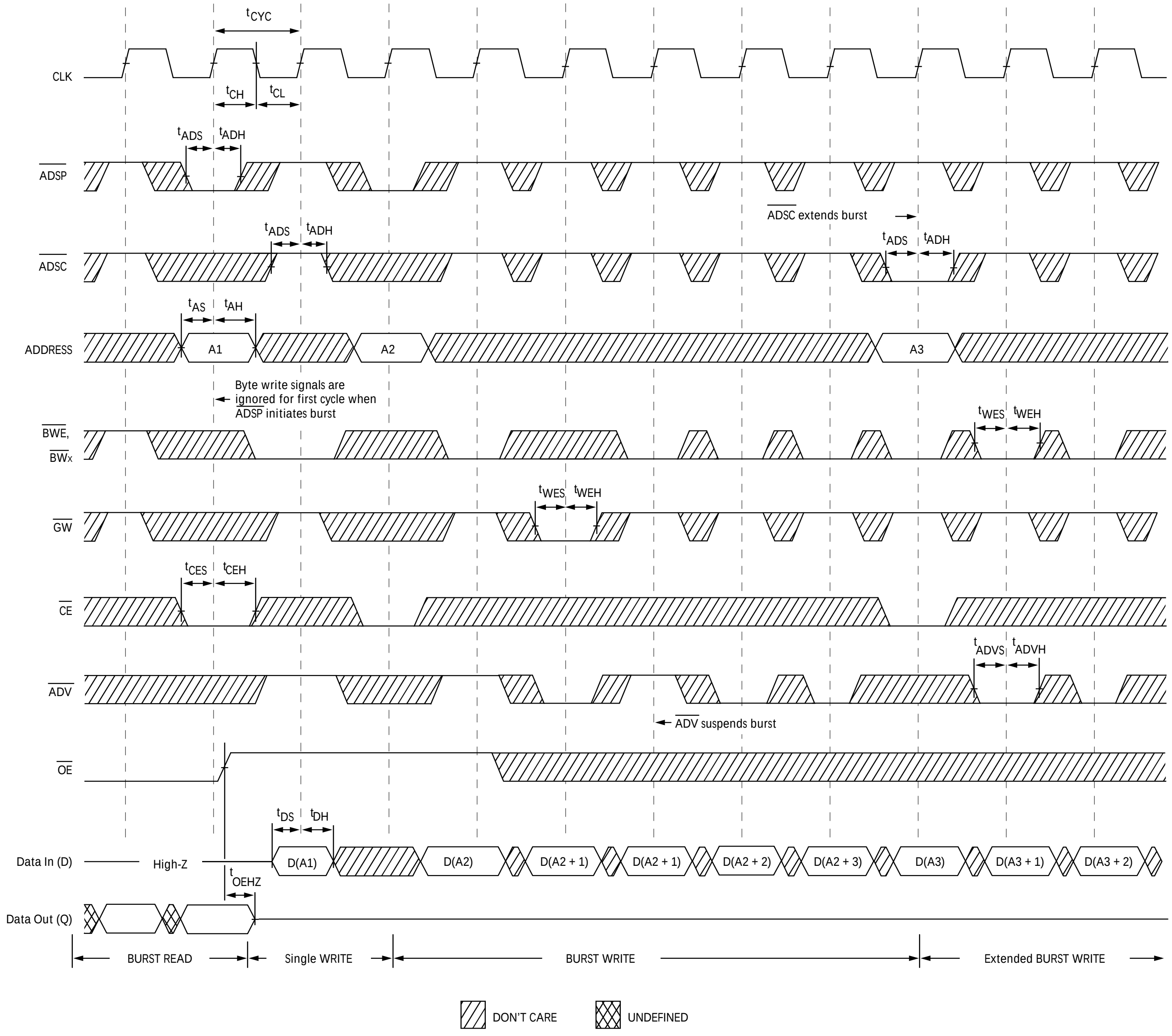


Note

26. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms *(continued)*

Figure 5. Write Cycle Timing [27, 28]

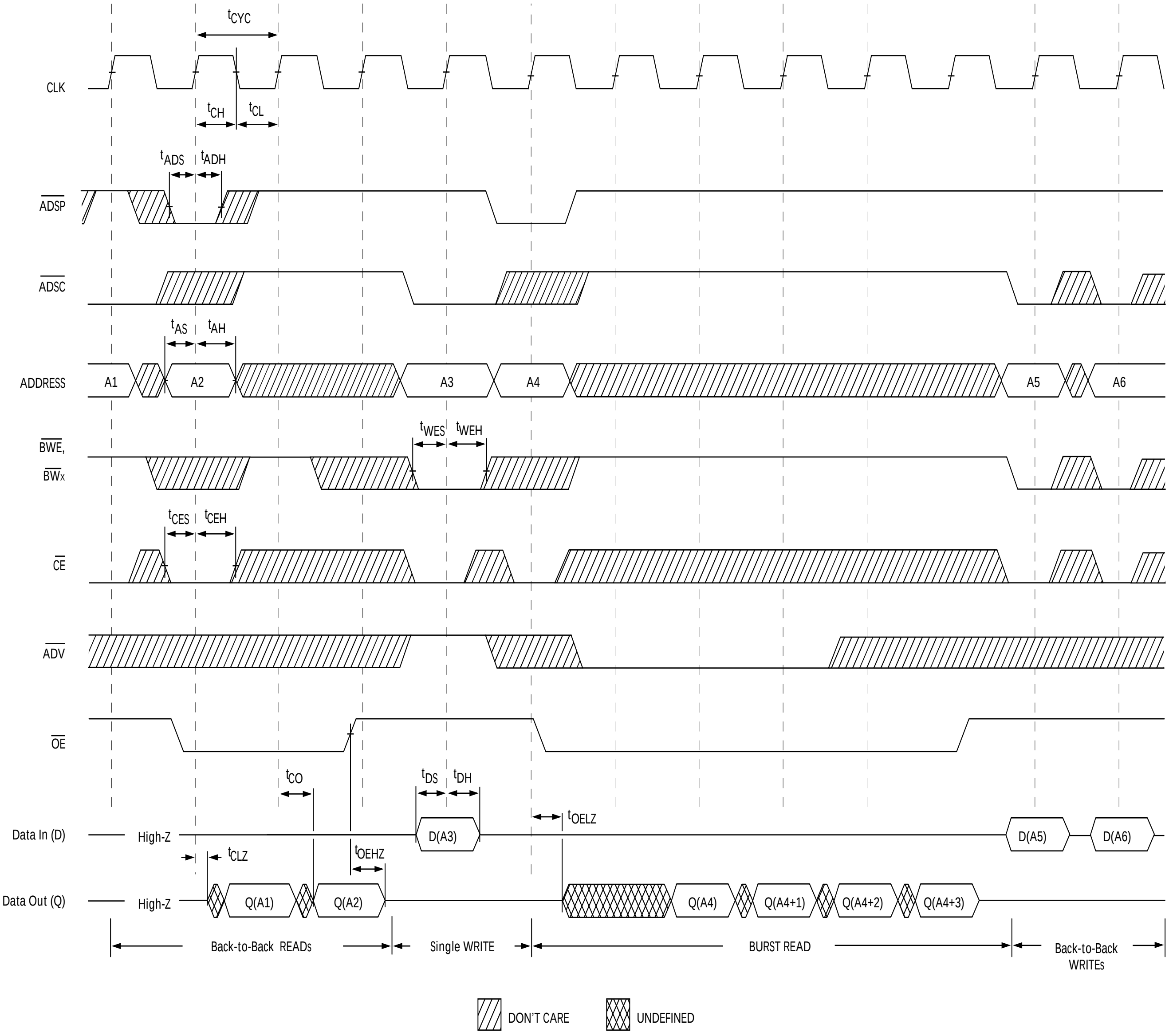


Notes

27. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
28. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Switching Waveforms *(continued)*

Figure 6. Read/Write Cycle Timing [29, 30, 31]



Notes

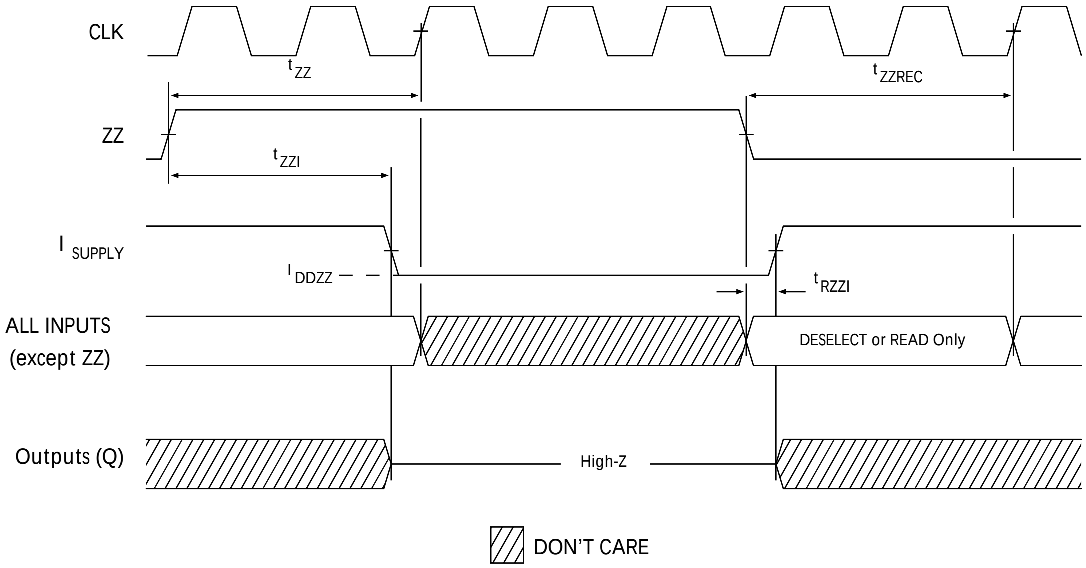
[29] On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

[30] The data bus (Q) remains in high Z following a Write cycle, unless a new read access is initiated by ADSP or ADSC.

[31] $\overline{GW}$ is HIGH.

Switching Waveforms *(continued)*

Figure 7. ZZ Mode Timing [32, 33]



Notes

[32] Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.

[33] DQs are in high Z when exiting ZZ sleep mode.

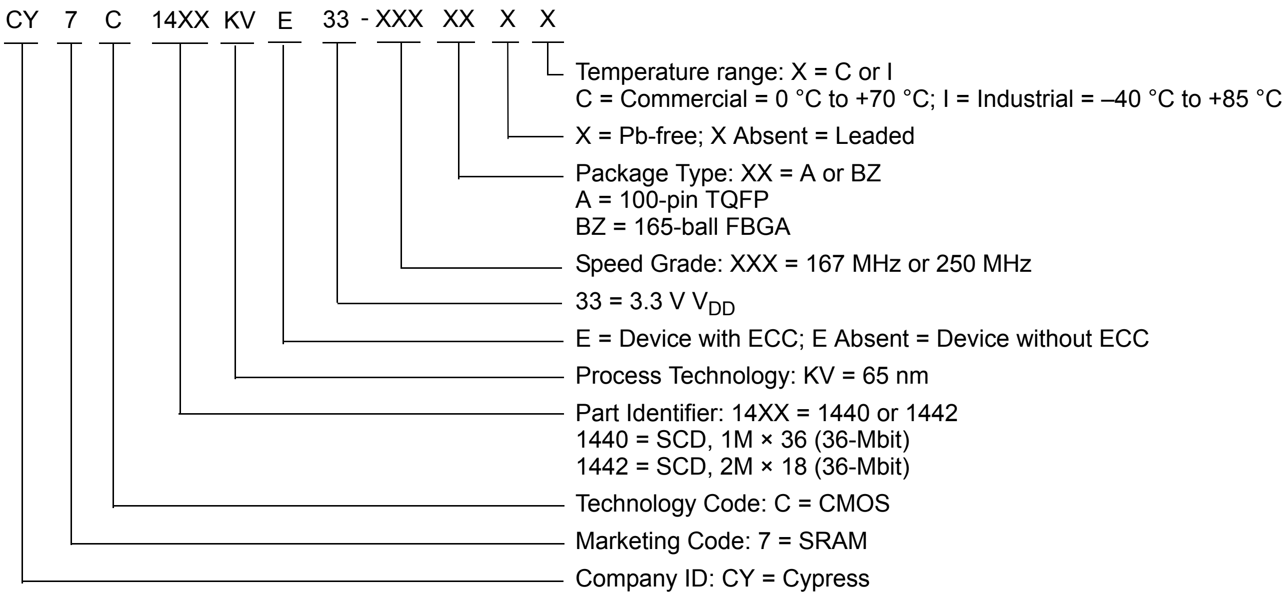
Ordering Information

Table 1 lists the ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
250	CY7C1440KV33-250AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1440KV33-250BZXI	51-85195	165-ball FBGA (15 × 17 × 1.4 mm) Pb-free	Industrial
	CY7C1442KV33-250AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial
167	CY7C1440KV33-167AXC		100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	
	CY7C1440KVE33-167AXC		100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	

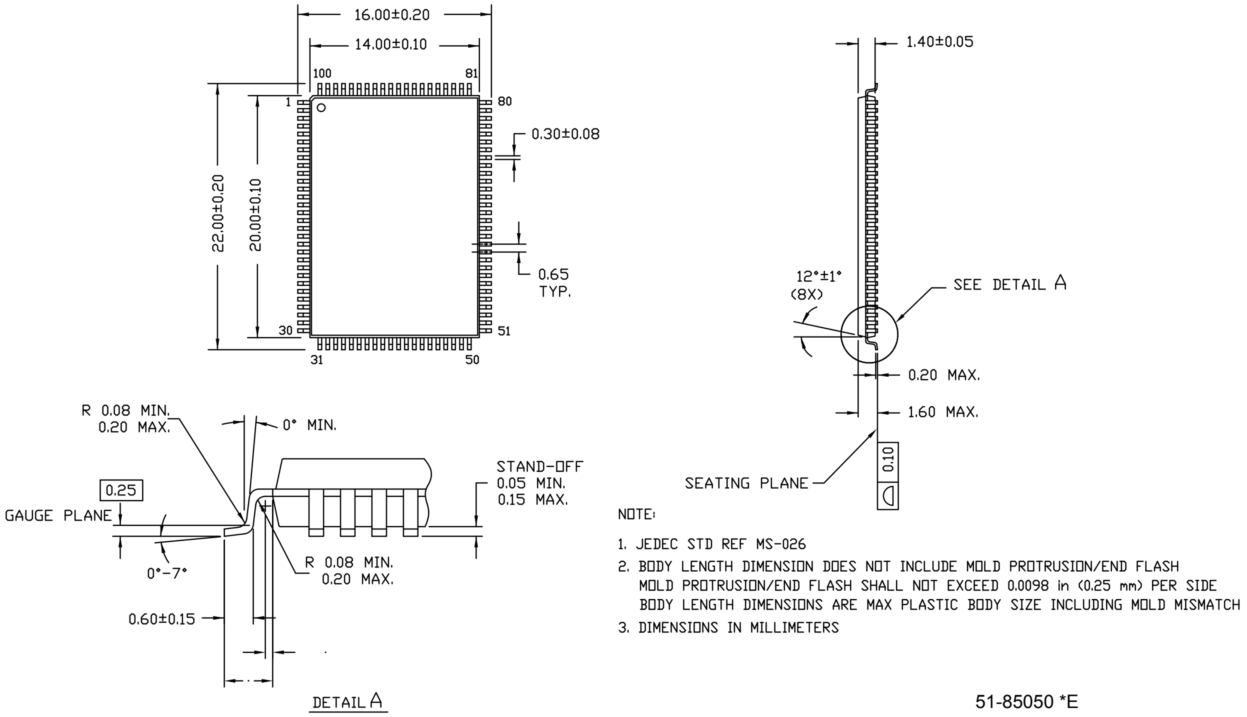
Ordering Code Definitions



Temperature range: X = C or I
C = Commercial = 0 °C to +70 °C; I = Industrial = –40 °C to +85 °C
X = Pb-free; X Absent = Leaded
Package Type: XX = A or BZ
A = 100-pin TQFP
BZ = 165-ball FBGA
Speed Grade: XXX = 167 MHz or 250 MHz
33 = 3.3 V V_{DD}
E = Device with ECC; E Absent = Device without ECC
Process Technology: KV = 65 nm
Part Identifier: 14XX = 1440 or 1442
1440 = SCD, 1M × 36 (36-Mbit)
1442 = SCD, 2M × 18 (36-Mbit)
Technology Code: C = CMOS
Marketing Code: 7 = SRAM
Company ID: CY = Cypress

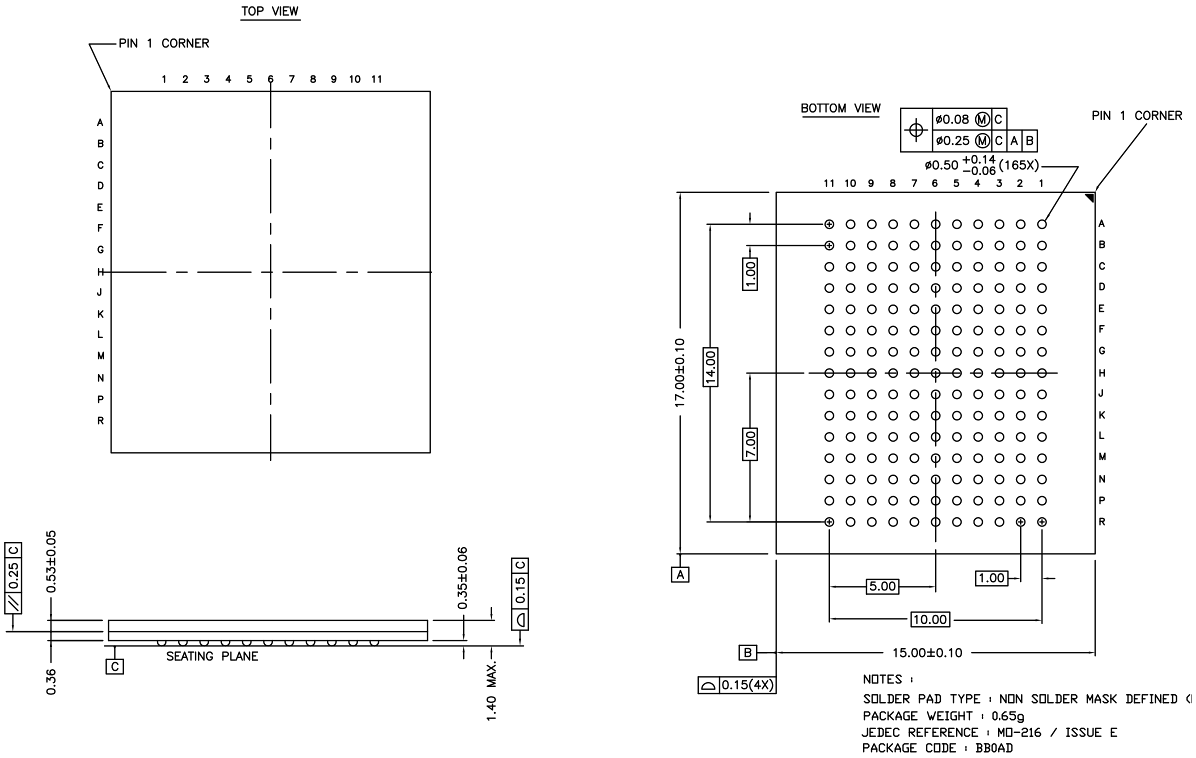
Package Diagrams

Figure 8. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



Package Diagrams *(continued)*

Figure 9. 165-ball FBGA (15 × 17 × 1.4 mm (0.5 Ball Diameter)) Package Outline, 51-85195



NOTES :
SOLDER PAD TYPE : NON SOLDER MASK DEFINED (
PACKAGE WEIGHT : 0.65g
JEDEC REFERENCE : MO-216 / ISSUE E
PACKAGE CODE : BB0AD

51-85195 *D

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
$\overline{CE}$	Chip Enable
$\overline{CEN}$	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JTAG	Joint Test Action Group
NoBL	No Bus Latency
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TCK	Test Clock
TDI	Test Data-In
TDO	Test Data-Out
TMS	Test Mode Select
TQFP	Thin Quad Flat Pack
$\overline{WE}$	Write Enable
ECC	Error Correcting Code

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1440KV33/CY7C1442KV33/CY7C1440KVE33, 36-Mbit (1M × 36/2M × 18) Pipelined Sync SRAM (With ECC)
Document Number: 001-66676

Rev.	ECN	Issue Date	Orig. of Change	Description of Change
*E	4680535	04/10/2015	PRIT	Changed status from Preliminary to Final.
*F	4757974	05/07/2015	DEVM	Updated Functional Overview: Updated ZZ Mode Electrical Characteristics: Changed maximum value of I_{DDZZ} parameter from 89 mA to 75 mA.
*G	5338013	07/05/2016	PRIT	Updated Truth Table. Updated Neutron Soft Error Immunity: Updated values in “Typ” and “Max” columns corresponding to LSBU (Device without ECC) parameter. Updated to new template.

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