FEMTOCLOCKS™ CRYSTAL-TO-2.5V LVPECL FREQUENCY SYNTHESIZER

ICS843001-40

General Description

The ICS843001-40 is an LVPECL output Synthesizer and is a member of the HiPerClocks™ family of high performance devices from IDT. The device uses a 40MHz crystal to provide a 40MHz reference clock output and to synthesize a 50MHz, 100MHz, or 106.25MHz output. The ICS843001-40 has excellent <1ps phase jitter performance over the 637kHz – 5MHz integration range. The ICS843001-40 is packaged in a 3mm x 3mm 16-pin VFQFN, making it ideal for use on space constrained boards.

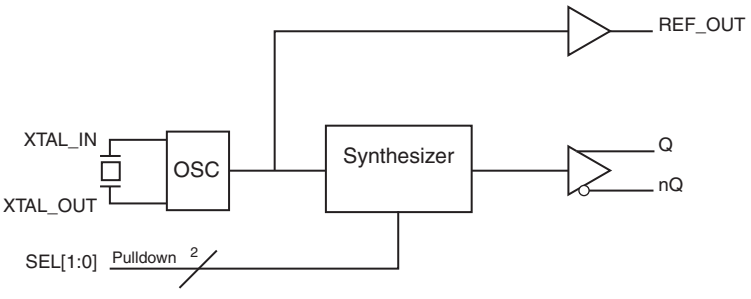
Features

- One differential 2.5V LVPECL output
  One reference clock output, 30Ω typical output impedance
- 40MHz, 10pF parallel resonant crystal
- Output frequencies: 50MHz, 100MHz, or 106.25MHz
- RMS phase jitter @ 106.25MHz, using a 40MHz crystal (637kHz –5MHz): 0.35ps (typical)
- 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Availabe in lead-free (RoHS 6) package

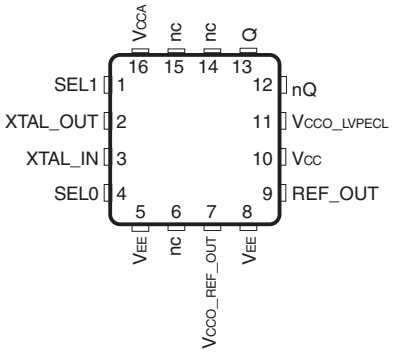
Function Table

Inputs		Outputs		
Crystal Frequency (MHz)	SEL[1:0]	Q/nQ Outputs Frequency (MHz)	REF_OUT Frequency (MHz)	Application
40	0 0	50	40	SAS (default)
40	0 1	100	40	SAS
40	1 0	106.25	40	Fiber Channel
40	1 1	106.25	40	Fiber Channel

Block Diagram



Pin Assignment



ICS843001-40
16-Lead VFQFN
3mm x 3mm x 0.925 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 4	SEL1, SEL0	Input	Pulldown	Output frequency select pins. LVCMOS/LVTTL interface levels.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
5, 8	V_{EE}	Power		Negative supply pins.
6, 14, 15	nc	Unused		No connect.
7	$V_{CCO\_REF\_OUT}$	Power		Output supply pin for REF_OUT output.
9	REF_OUT	Output		Single-ended three-state reference clock output. LVCMOS/LVTTL interface levels. 30Ω typical output impedance.
10	V_{CC}	Power		Core supply pin.
11	V_{CCO_LVPECL}	Power		Output supply pin for Q/nQ outputs.
12, 13	nQ, Q	Output		Differential output pair. LVPECL interface levels.
16	V_{CCA}	Power		Analog supply pin.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	REF_OUT			30		Ω

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, V_O (LVCMOS)	-0.5V to $V_{CCO\_REF\_OUT}$ + 0.5V
Package Thermal Impedance, θ_{JA}	74.9°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_REF\_OUT} = V_{CCO\_LVPECL} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.08	2.5	V_{CC}	V
V_{CCO_LVPECL}, $V_{CCO\_REF\_OUT}$	Output Supply Voltage		2.375	2.5	2.625	V
I_{CCA}	Analog Supply Current				8	mA
I_{EE}	Power Supply Current				80	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO\_REF\_OUT} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{CC} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	$V_{CC} = 2.625V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1	$I_{OH} = 1mA$	2.2			V
V_{OL}	Output Low Voltage; NOTE 1	$I_{OL} = -1mA$			0.4	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_REF\_OUT}/2$ See Parameter Measurement Information Section, "2.5V Output Load Test Circuit" diagram.

Table 3C. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_LVPECL} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_LVPECL} - 1.4		V_{CCO_LVPECL} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO_LVPECL} - 2.0		V_{CCO_LVPECL} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO_LVPECL} - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

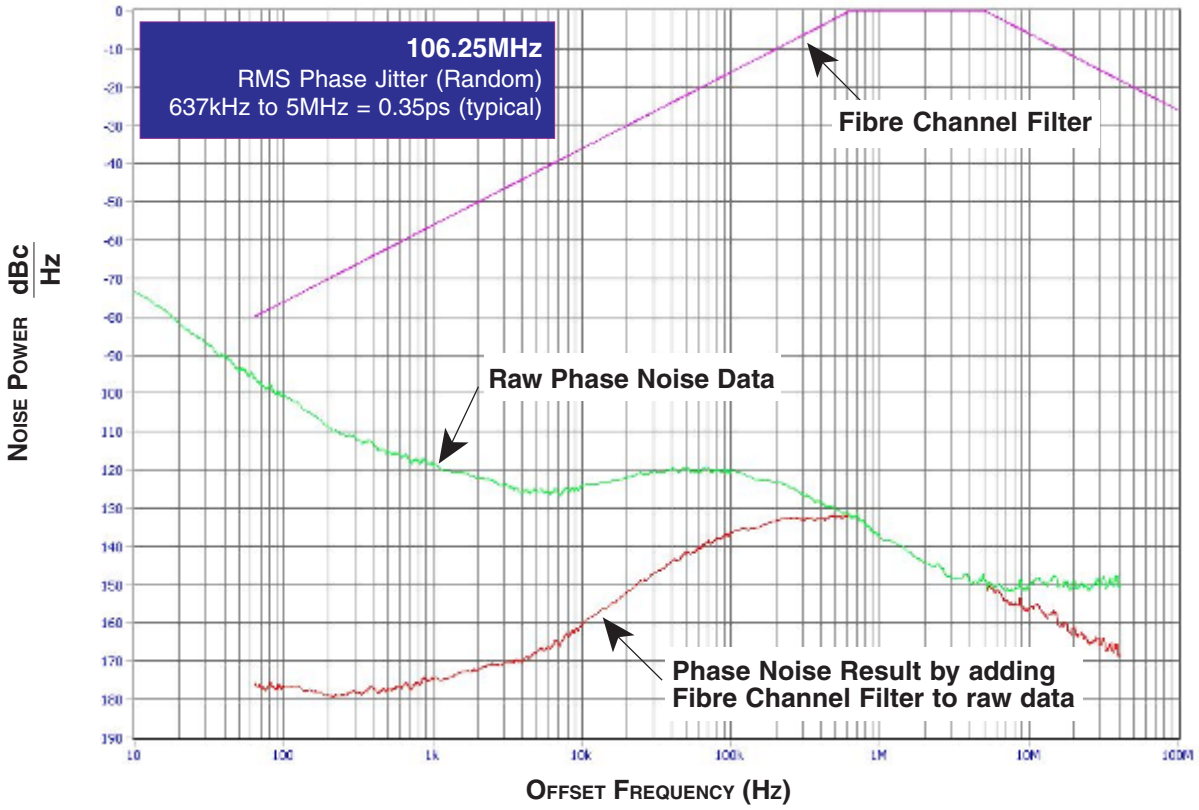
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			40		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_REF\_OUT} = V_{CCO\_LVPECL} = 2.5V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

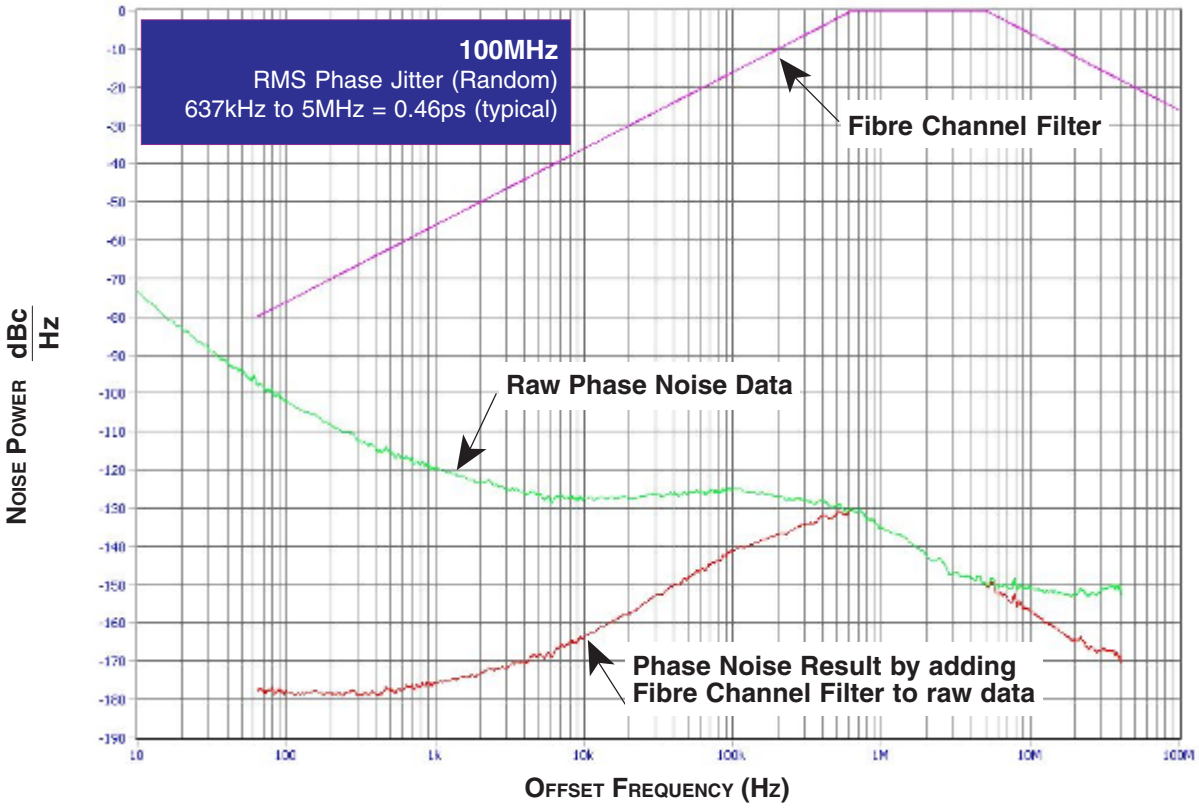
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	REF_OUT			40		MHz
		Q/nQ	SEL_OUT = 00		50		MHz
		Q/nQ	SEL_OUT = 01		100		MHz
		Q/nQ	SEL_OUT = 10 or 11		106.25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random)		50MHz, Integration Range: 637kHz – 5MHz		0.53		ps
			100MHz, Integration Range: 637kHz – 5MHz		0.46		ps
			106.25MHz, Integration Range: 637kHz – 5MHz		0.35		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1	REF_OUT	40MHz			125	ps
		Q/nQ				110	ps
t_R / t_F	Output Rise/Fall Time	REF_OUT	20% to 80%	0.7		2.1	ns
		Q/nQ	20% to 80%	150		650	ps
odc	Output Duty Cycle	REF_OUT		45		55	%
		Q/nQ		48		52	%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

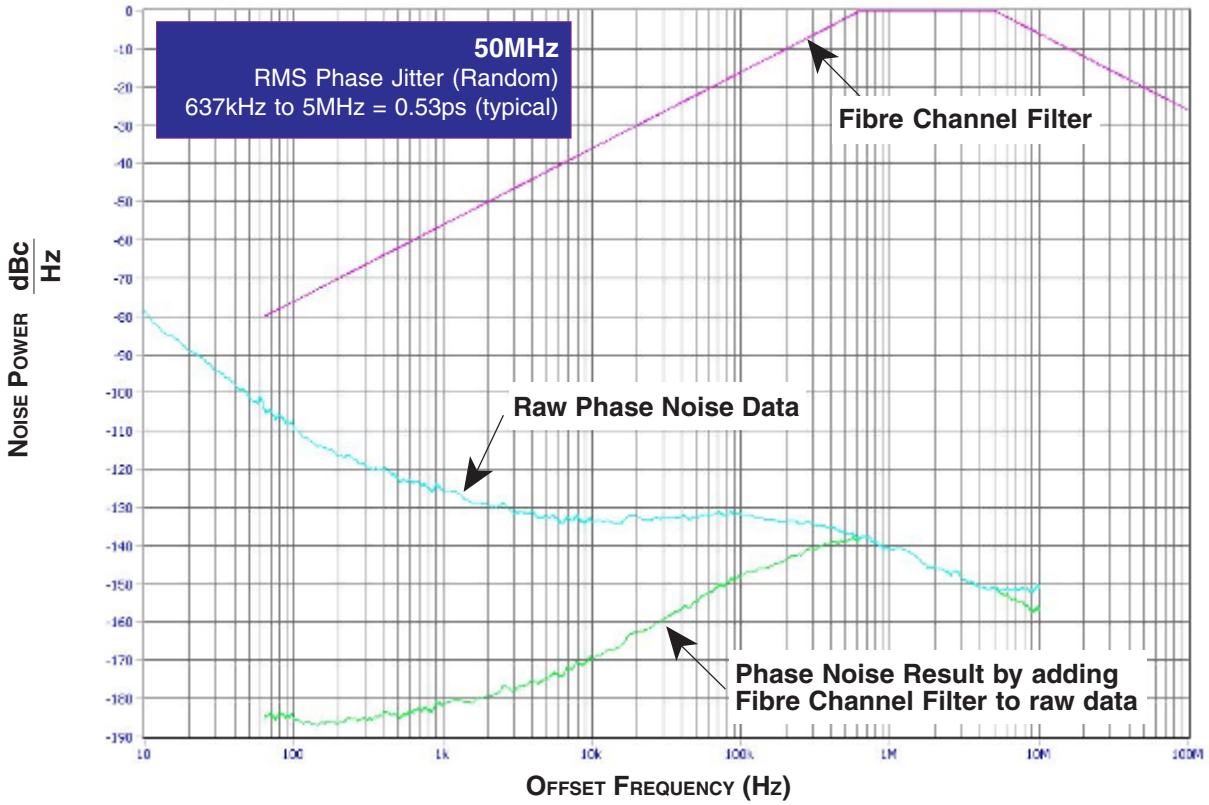
TYPICAL PHASE NOISE AT 106.25MHZ



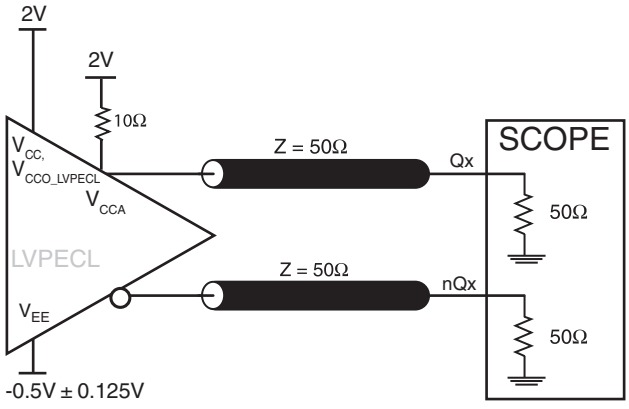
TYPICAL PHASE NOISE AT 100MHZ



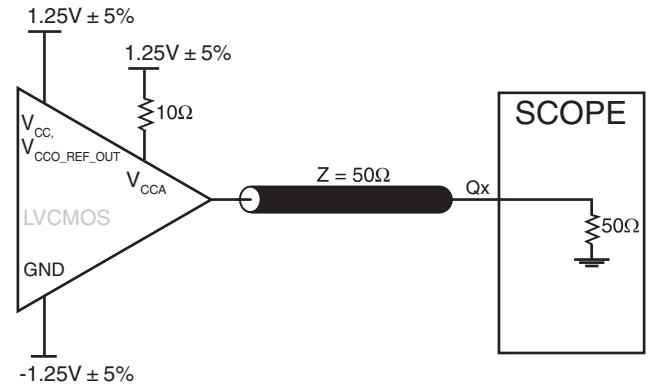
TYPICAL PHASE NOISE AT 50MHZ



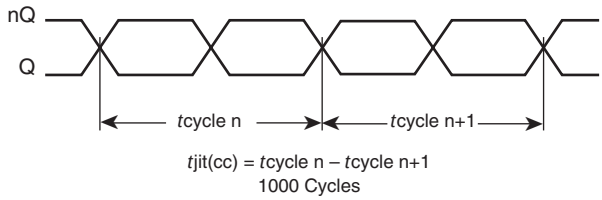
PARAMETER MEASUREMENT INFORMATION



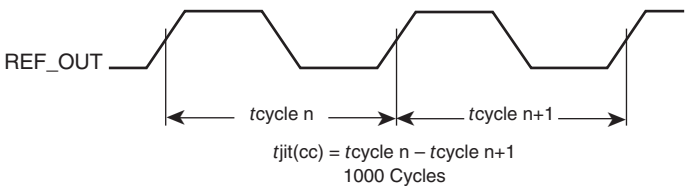
2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT



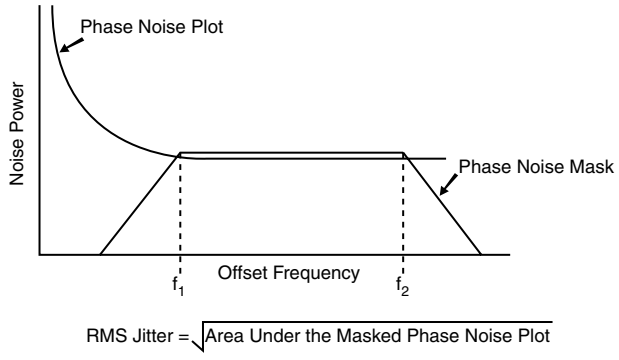
2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



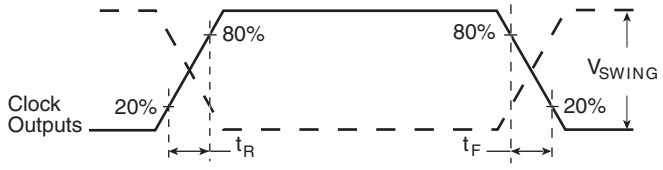
LVPECL CYCLE-TO-CYCLE JITTER



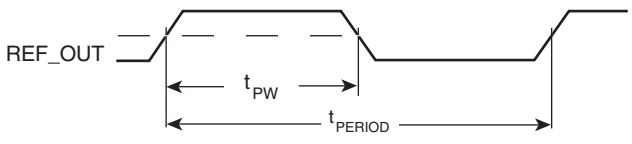
LVCMOS CYCLE-TO-CYCLE JITTER



RMS PHASE JITTER

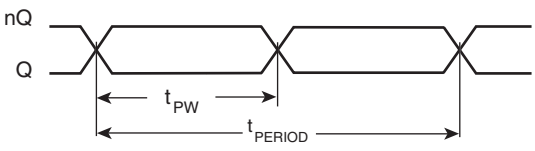


OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001-40 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, V_{CCO_LVPECL} and $V_{CCO\_REF\_OUT}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a 0.01µF bypass capacitor should be connected to each V_{CCA} pin.

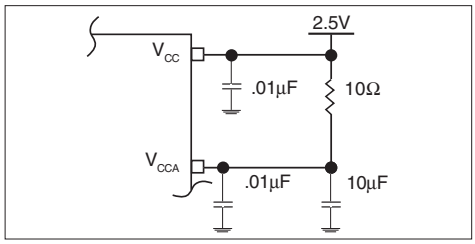


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT

All unused LVCMOS output can be left floating. There should be no trace attached.

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS843001-40 has been characterized with 10pF parallel resonant crystals. The capacitor C1 and C2 are not required if a 10pF parallel resonant crystal is used. It is recommended to provide these spare footprints if further frequency accuracy fine tuning is needed.

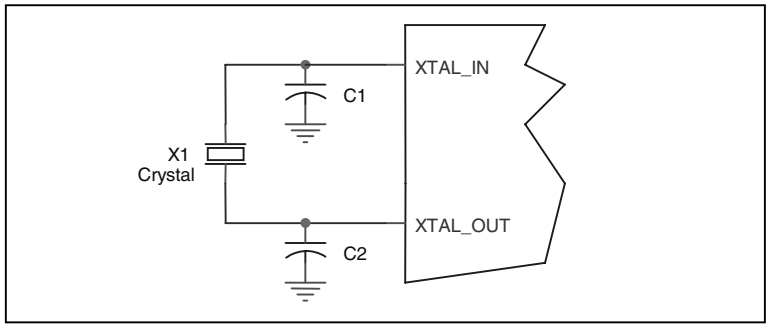


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

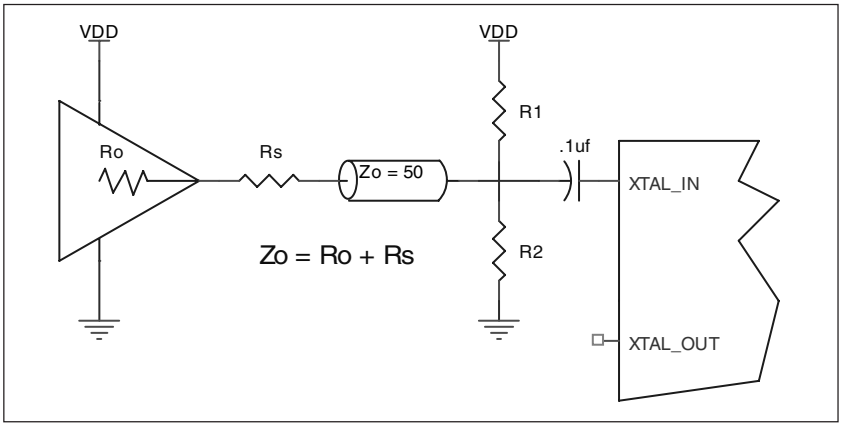


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/ slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/ Electrically Enhance Leadfame Base Package, Amkor Technology.

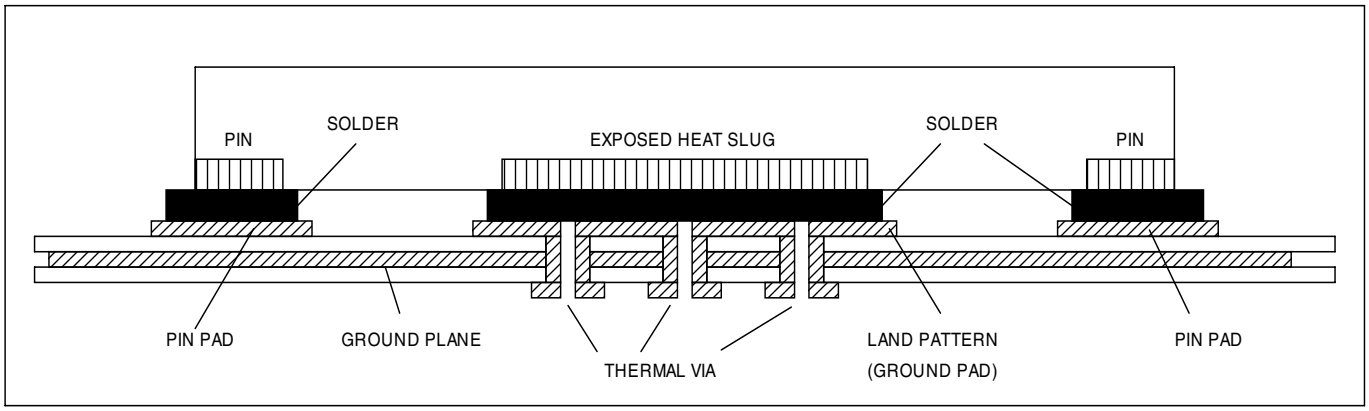


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{cc} – 2V. For V_{cco} = 2.5V, the V_{cco} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

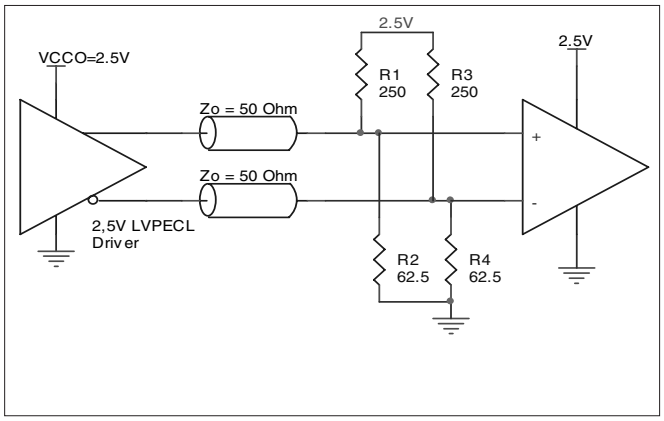


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

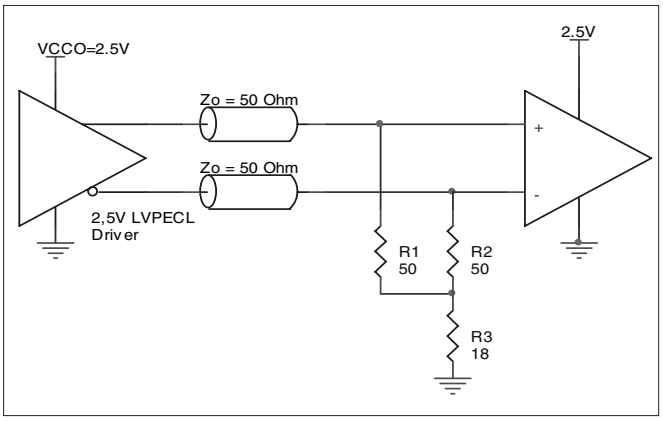


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

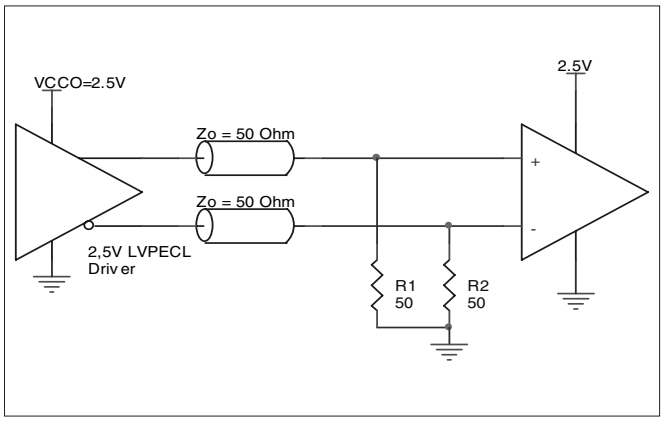


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

SCHEMATIC EXAMPLE

Figure 6 shows an example of ICS843001-40 application schematic. In this example, the device is operated at V_{CC} = 2.5V. The 10pF parallel resonant 40MHz crystal is used in characterization. The C1 and C2 capacitor are not required if a 10pF parallel resonant crystal is used. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

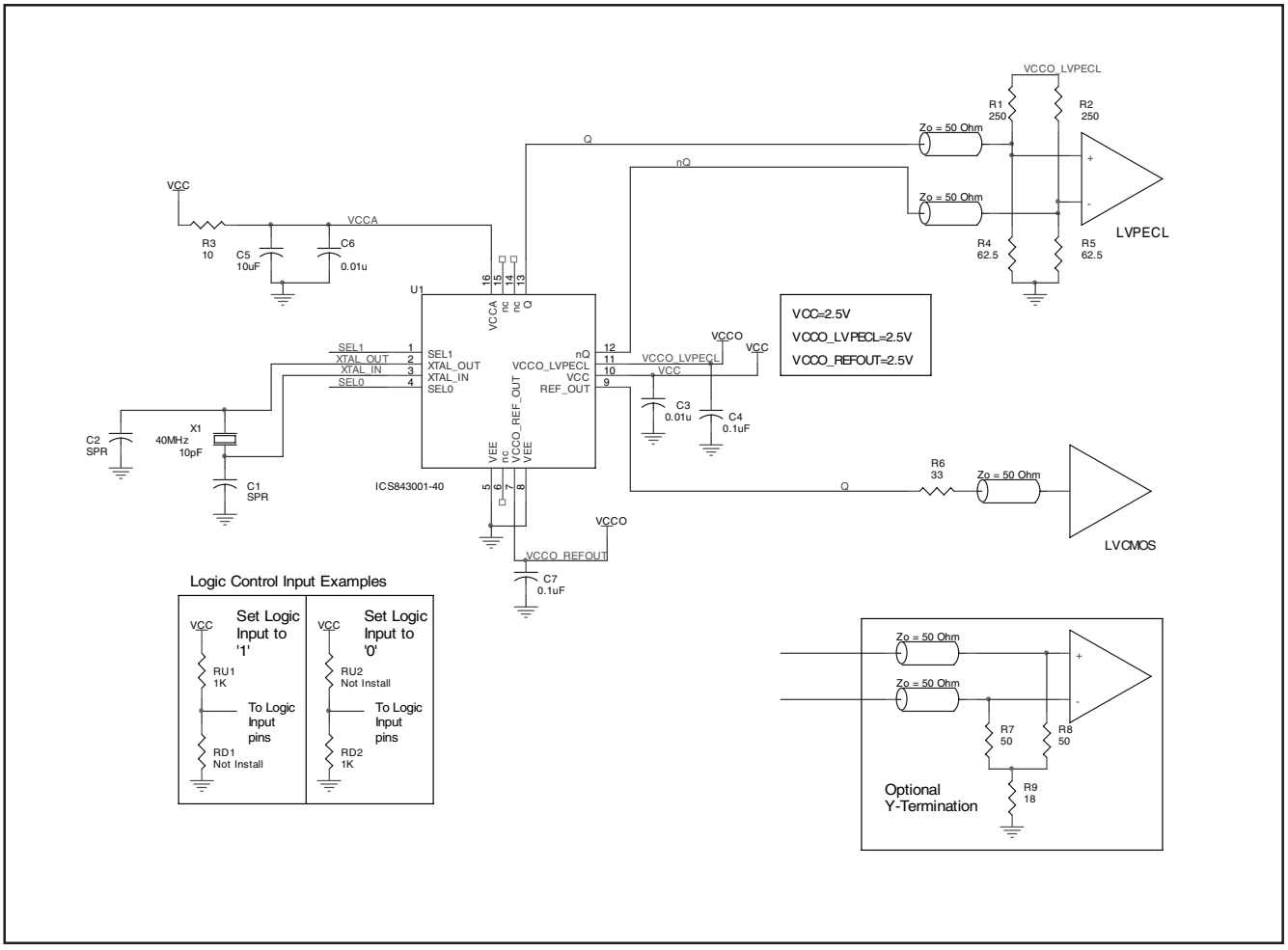


FIGURE 6. EXAMPLE ICS843001-40 FREQUENCY SYNTHESIZER SCHEMATIC

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843001-40.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843001-40 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 2.5V + 5% = 2.625V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 2.625V * 80mA = **210mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  Total Power$_{_MAX}$ = 210mW + 30mW = **240mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.240W * 74.9°C/W = 87.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.9°C/W	65.5°C/W	58.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

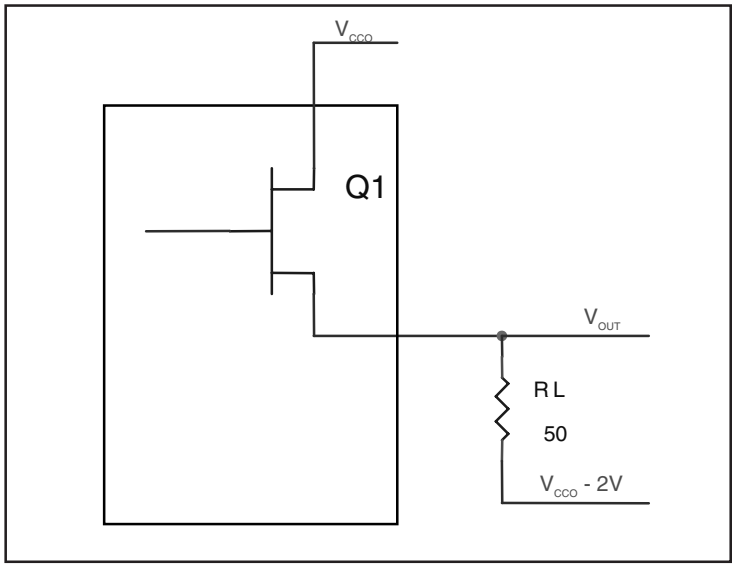


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.9°C/W	65.5°C/W	58.8°C/W

TRANSISTOR COUNT

The transistor count for ICS843001-40 is: 2121

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

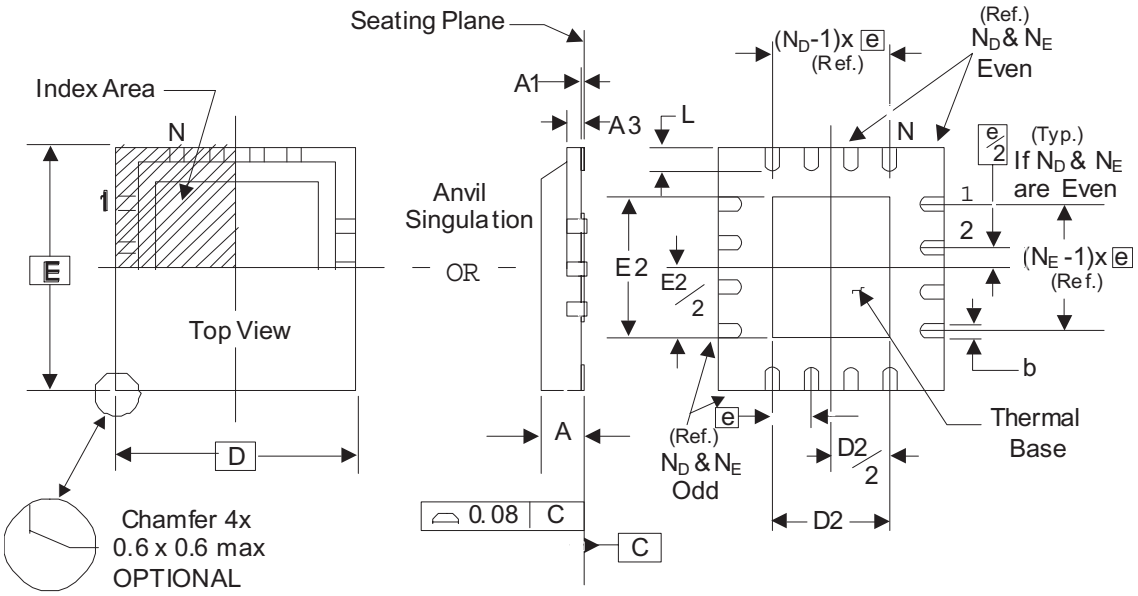


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	1.0	1.8
E	3.0	
E2	1.0	1.8
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843001AK-40LF	A40L	16 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
ICS843001AK-40LFT	A40L	16 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS complaint.

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