CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

ICS843004-02

General Description

The ICS843004-02 is a 4 output LVPECL Synthesizer optimized to generate clock frequencies for a variety of high performance applications and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. This device can select its input reference clock from either a crystal input or a single-ended clock signal and can be configured to generate a number of different output frequencies via the 3 frequency select pins (F_SEL2:0). The ICS843004-02 uses IDT' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter. This ensures that it will easily meet clocking requirements for high-speed communication protocols such as 10 and 12 Gigabit Ethernet, 10 Gigbit Fibre Channel, and SONET. This device is also suitable for next generation serial I/O technologies like serial ATA and SCSI and is conveniently packaged in a small 24-pin TSSOP package.

Function Table

Inputs			M Divider Value	N Divider Value
F_SEL2	F_SEL1	F_SEL0		
0	0	0	18	3
0	0	1	24	4
0	1	0	24	8
0	1	1	32	1
1	0	0	32	2
1	0	1	32	4
1	1	0	32	8
1	1	1	40	8

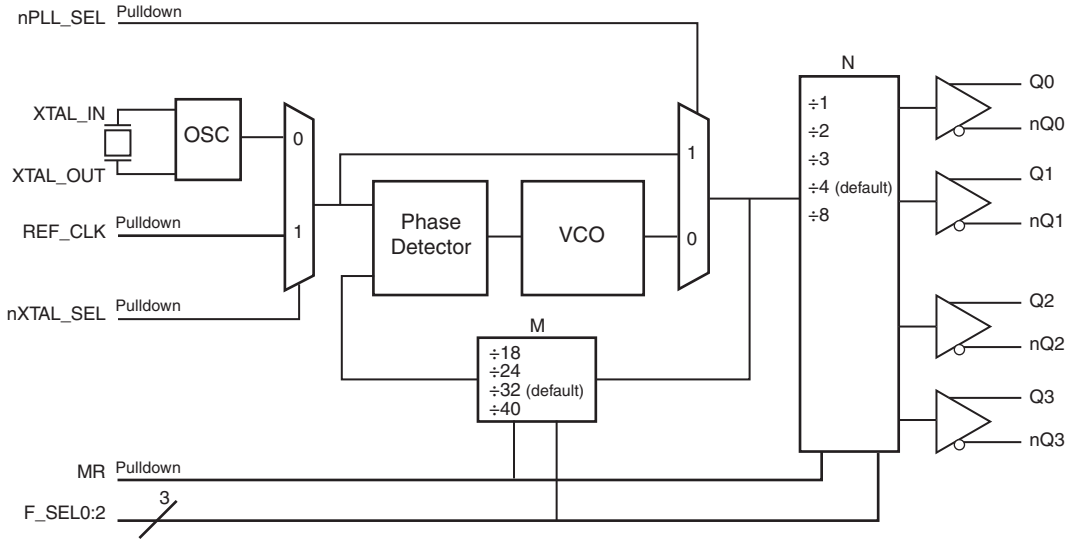
Features

- Four 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Output frequency range: 70MHz - 680MHz
- Crystal input range: 14MHz - 37.78MHz
- VCO Range: 560MHz - 680MHz
- Supports the following applications: Fibre Channel, SONET, Ethernet, Serial ATA, SCSI and HDTV
- RMS phase jitter @ 155.52MHz (12kHz - 20MHz): 0.91ps (typical)

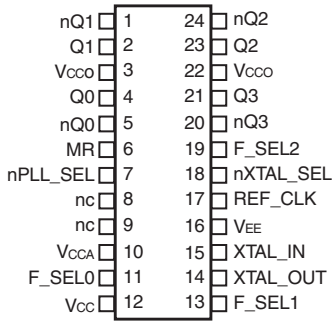
Offset	Noise Power
100Hz	-97.1 dBc/Hz
1kHz	-121.6 dBc/Hz
10kHz	-124.9 dBc/Hz
100kHz	-125.1 dBc/Hz

- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

Block Diagram



Pin Assignment



ICS843004-02
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
3, 22	V_{CCO}	Power		Output supply pins.
4, 5	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, selects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 9	nc	Unused		No connect.
10	V_{CCA}	Power		Analog supply pin.
11, 19	F_SEL0, F_SEL2	Input	Pullup	Frequency select pins. LVCMOS/LVTTL interface levels.
12	V_{CC}	Power		Core supply pin.
13	F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
14, 15	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
16	V_{EE}	Power		Negative supply pin.
17	REF_CLK	Input	Pulldown	LVCMOS/LVTTL reference clock input.
18	nXTAL_SEL	Input	Pulldown	Selects between crystal or REF_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects REF_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown and Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3. OUTPUT CONFIGURATION AND FREQUENCY RANGE FUNCTION TABLE

Inputs				M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
F_SEL2	F_SEL1	F_SEL0	REF_CLK					
0	1	0	24.75	24	8	594	74.25	HDTV
1	1	1	14.8351649	40	8	593.4066	74.1758245	HDTV
1	1	1	16	40	8	640	80	SCSI
1	0	1	19.44	32	4	622.08	155.52	SONET
1	1	0	19.44	32	8	622.08	77.76	SONET
0	1	1	19.44	32	1	622.08	622.08	SONET
1	0	0	19.44	32	2	622.08	311.04	SONET
0	0	1	25	24	4	600	150	SATA
0	1	0	25	24	8	600	75	SATA
0	0	1	26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
1	0	1	19.53125	32	4	625	156.25	10 Gig Ethernet
0	0	0	31.25	18	3	562.5	187.5	12 Gig Ethernet

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC}– 0.12	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				150	mA
I_{CCA}	Analog Supply Current				12	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	nPLL_SEL, nXTAL_SEL, F_SEL0:F_SEL2, MR		-0.3		0.8	V
		REF_CLK		-0.3		1.3	V
I_{IH}	Input High Current	REF_CLK, MR, F_SEL1 nPLL_SEL, nXTAL_SEL	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		F_SEL0, F_SEL2	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, F_SEL1 nPLL_SEL, nXTAL_SEL,	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		F_SEL0, F_SEL2	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		14		37.78	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

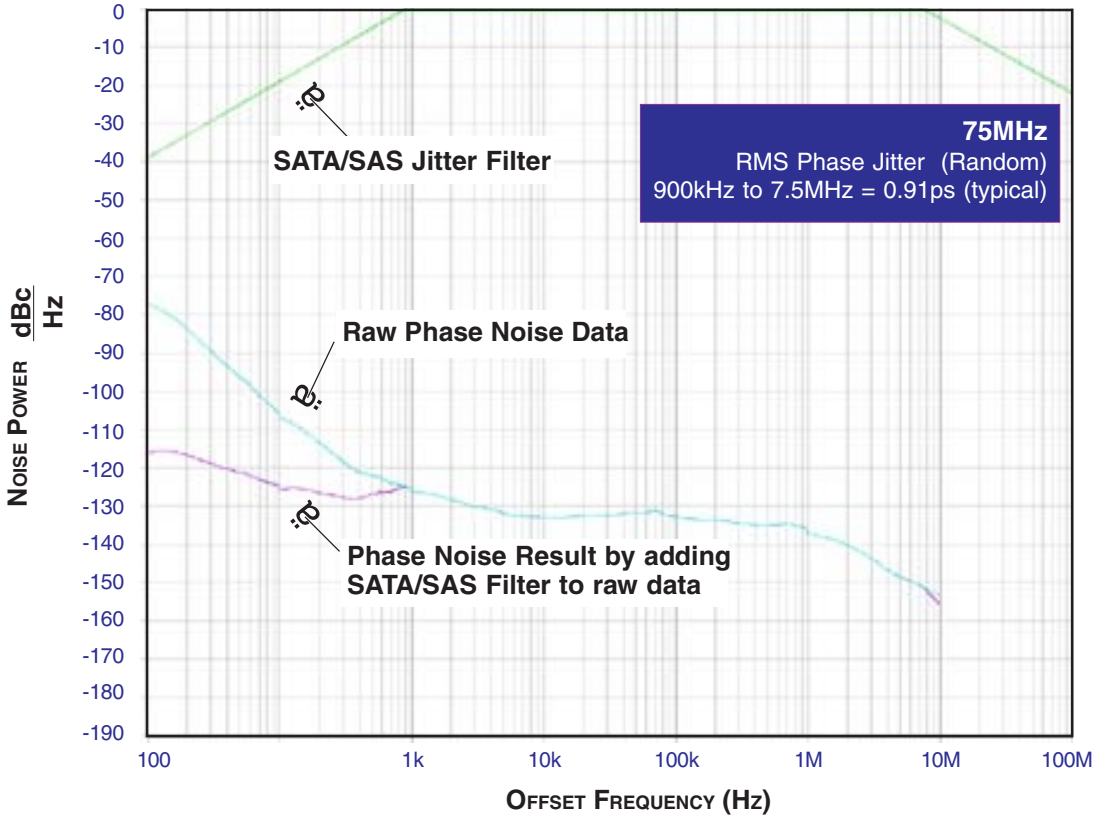
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

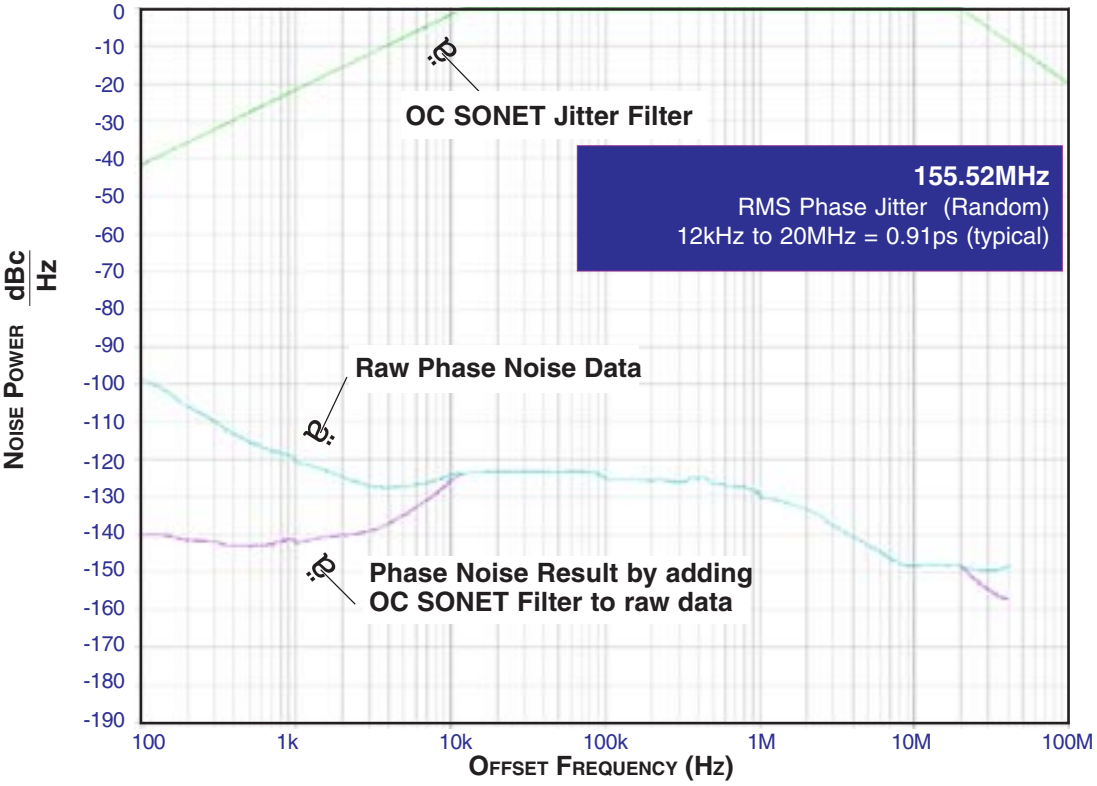
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		70		680	MHz
f_{VCO}	PLL VCO Lock Range	F_SEL{2:0] ≠ 000	560		680	MHz
		F_SEL{2:0] = 000	560		580	MHz
*t*sk(o)	Output Skew; NOTE 1				25	ps
*t*jit(Ø)	RMS Phase Jitter; NOTE 2, 3	155.52MHz, 12kHz -20MHz		0.91		ps
		75MHz, 900kHz -7.5MHz		0.76		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		500	ps
odc	Output Duty Cycle	Odd N Divider	46		54	%
		Even N Divider	48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 2: Phase jitter is measured using the crystal input.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

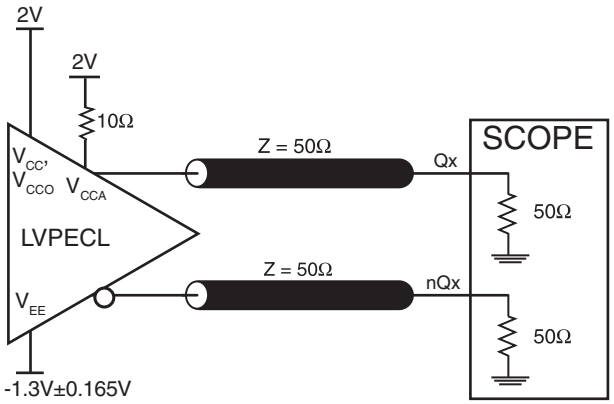
Typical Phase Noise at 75MHz At 3.3V



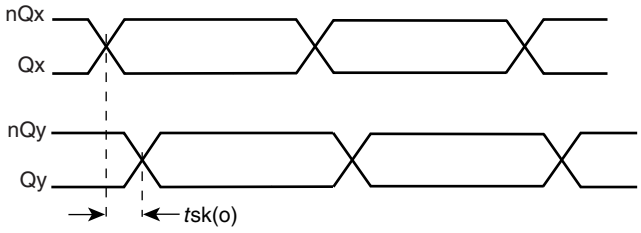
Typical Phase Noise at 155.52MHz At 3.3V



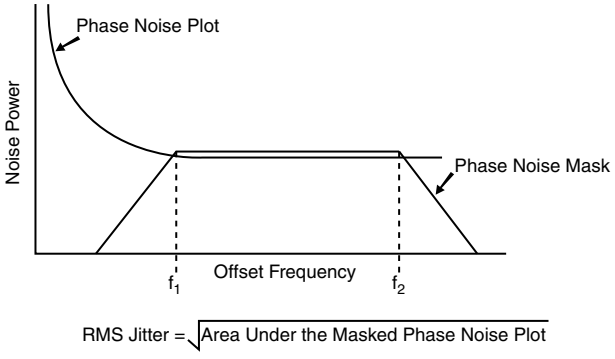
PARAMETER MEASUREMENT INFORMATION



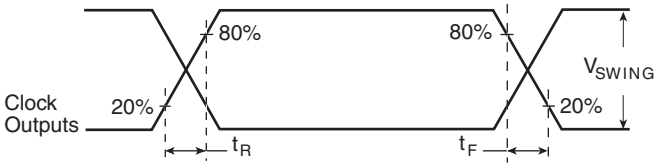
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



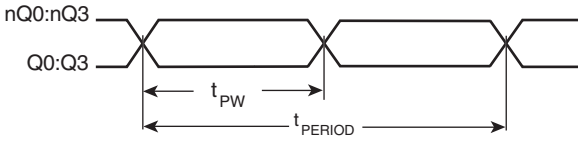
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843004-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

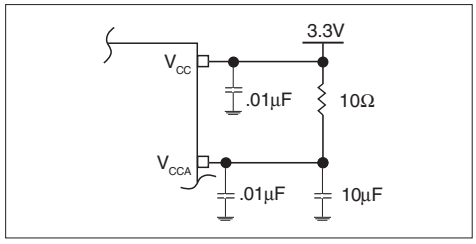


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

SELECT PINS:
All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The ICS843004-02 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

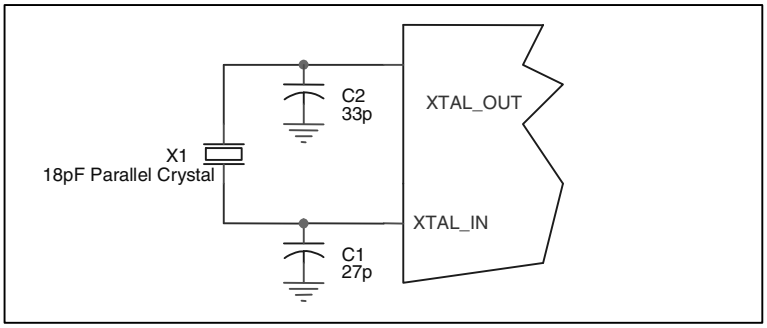


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

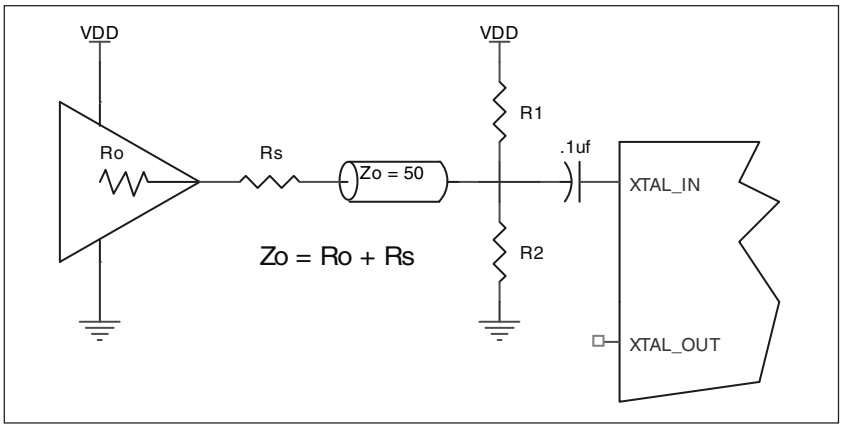


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

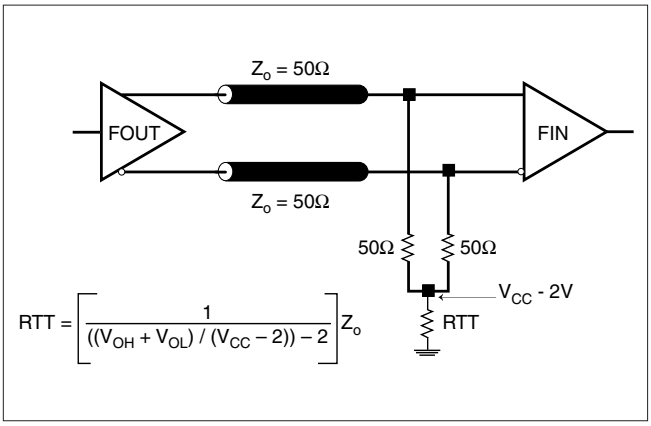


FIGURE 4A. LVPECL OUTPUT TERMINATION

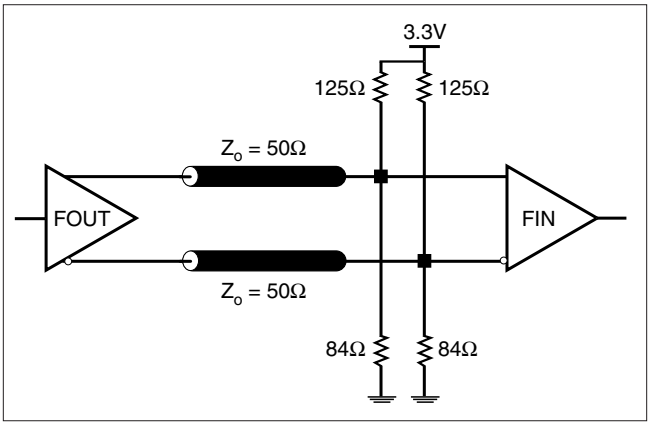


FIGURE 4B. LVPECL OUTPUT TERMINATION

LAYOUT GUIDELINE

Figure 5 shows an example of ICS843004-02 application schematic. In this example, the device is operated at V_{CC} = 3.3V. The decoupling capacitor should be located as close as possible to the power pin. Both input options are shown. The device can either be driven using a quartz crystal or a 3.3V LVCMOS signal. For the LVPECL output drivers, only two termination examples are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

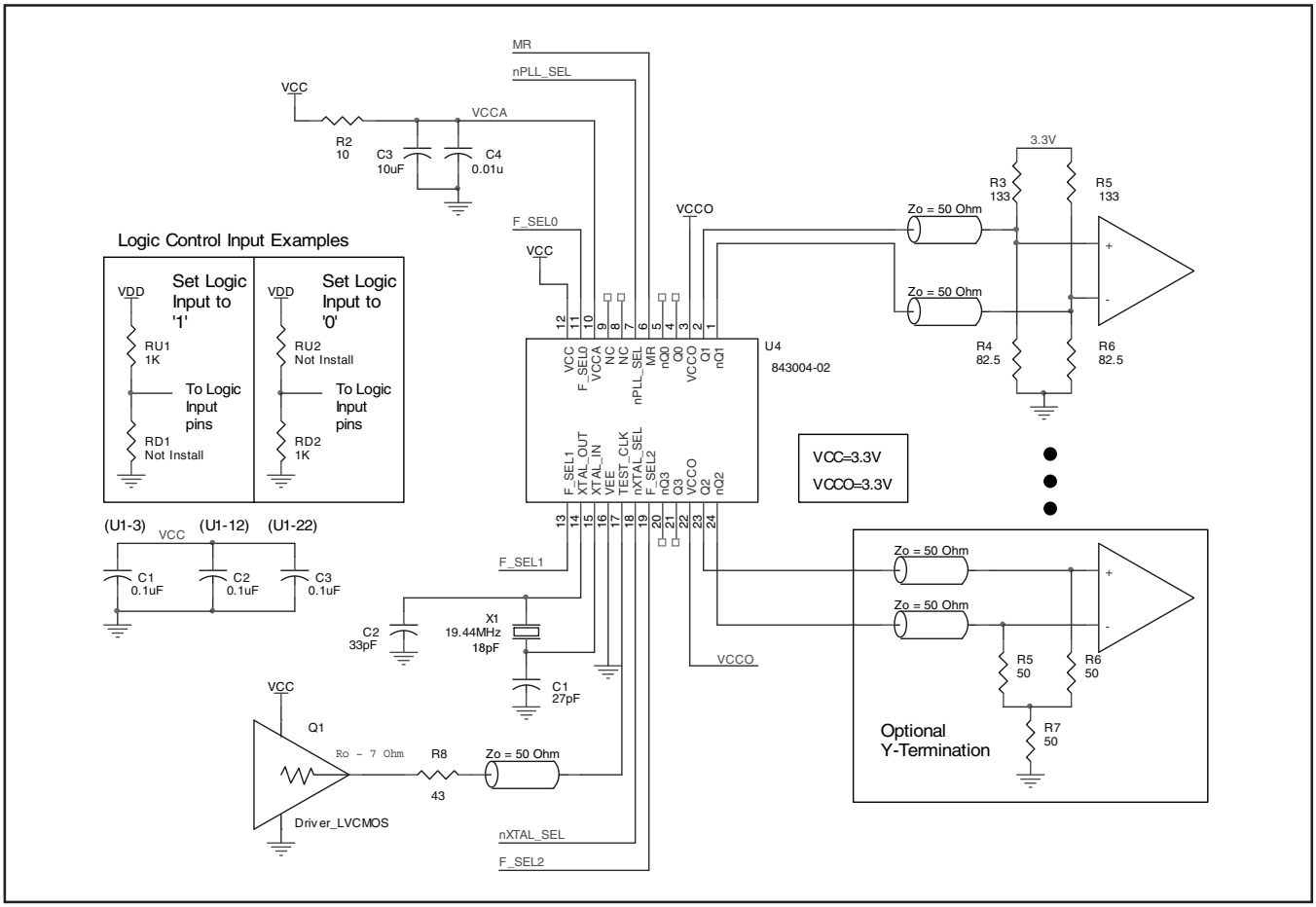


FIGURE 5. ICS843004-02 SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843004-02.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS843004-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 150mA = **519.75mW**
- Power $(outputs)_{MAX}$ = **32.8mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 x 32.8mW = **131.2mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 519.75mW + 131.2mW = **650.95mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 linear meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.651W * 65°C/W = 112.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

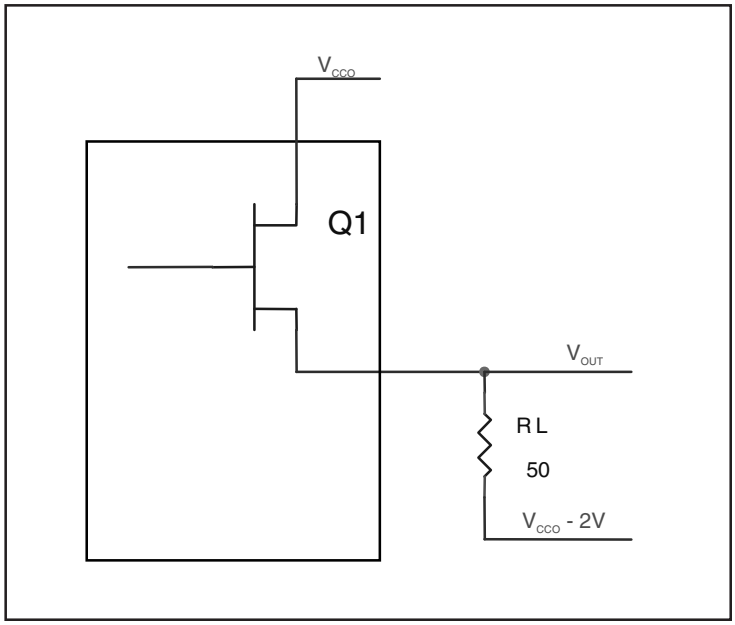


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MIN}/R_L) * (V_{DD\_MAX} - V_{OH\_MIN})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$

Pd_H = (1V/50Ω) * (2V - 1V) = **20mW**
Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.8mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843004-02 is: 3467

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

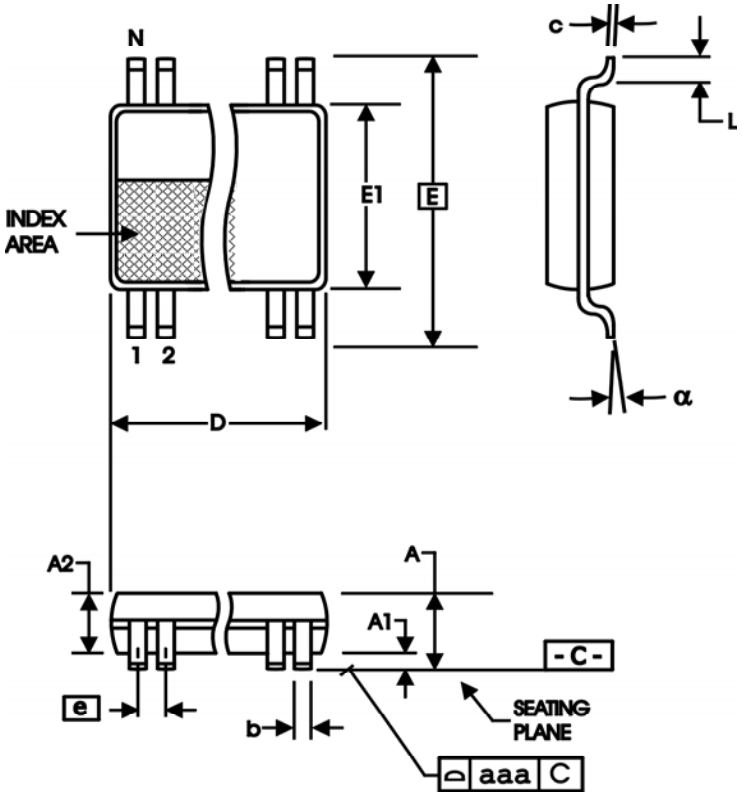


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843004AG-02	ICS843004A02	24 Lead TSSOP	tube	0°C to 70°C
ICS843004AG-02T	ICS843004A02	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS843004AG-02LF	ICS843004A02L	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS843004AG-02LFT	ICS843004A02L	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1	2	Pin Description Table - corrected nPLL_SEL description.	9/25/06
A	T9	16	Ordering Information Table - Added Lead Free Markings	7/30/07

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