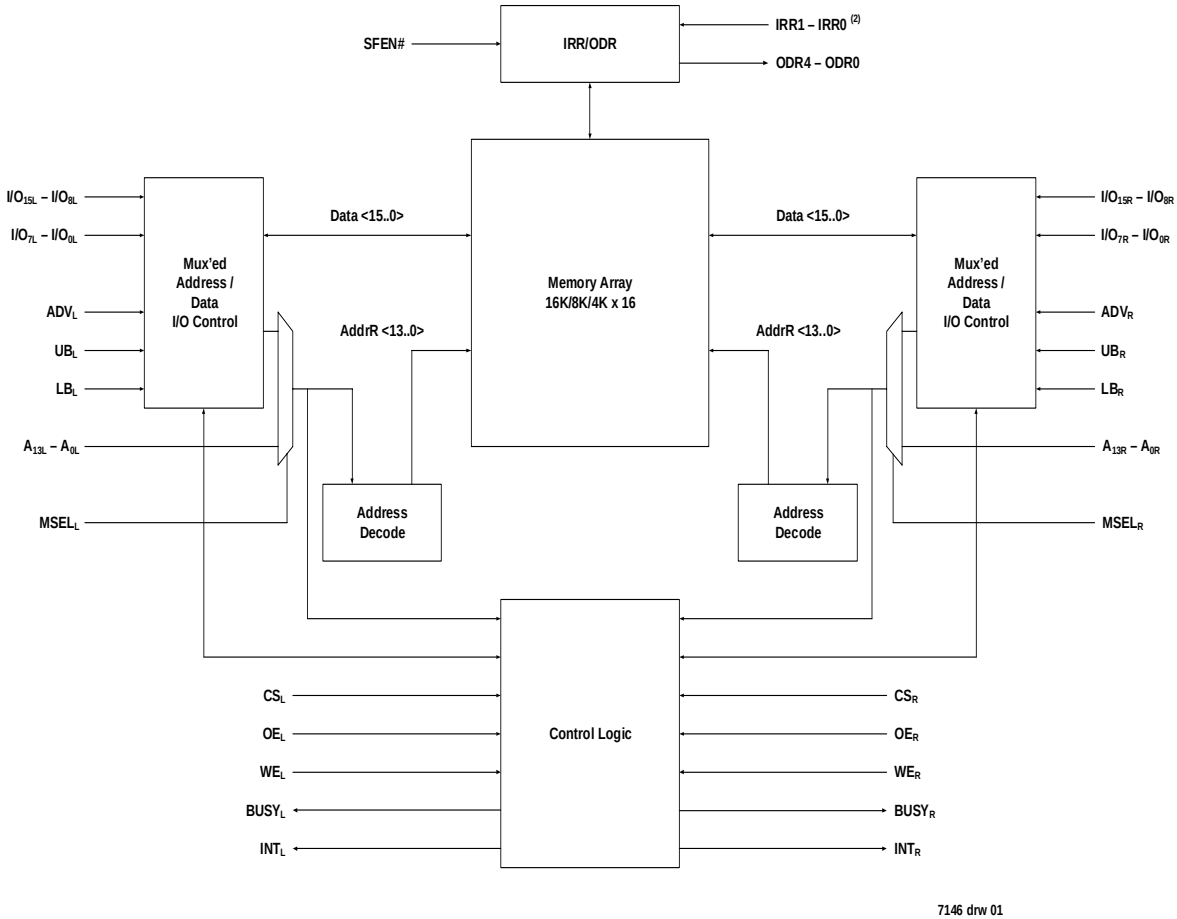
# VERY LOW POWER 1.8V 16K/8K/4K X 16 DUAL-PORT STATIC RAM

**IDT70P269/259/249L**

## Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- Both ports configurable to standard SRAM or time-multiplexed address/data interface
- High-speed access
  - *Industrial: 65ns (max.), ADM mode*
  - *Industrial: 40ns (max.), Standard SRAM mode*
- Low-power operation
  - *IDT70P269/259/249L*
  - *Active: 27mW (typ.)*
  - *Standby: 3.6µW (typ.)*
- Supports 3.0V, 2.5V and 1.8V I/O's
- Power supply isolation functionality to aid system power management
- Separate upper-byte and lower-byte control
- Input Read Register
- Output Drive Register
- $\overline{BUSY}$ and Interrupt Flag
- On-chip port arbitration logic
- Fully asynchronous operation from either port
- Available in 100 Ball 0.5mm-pitch BGA
- Industrial temperature range (-40°C to +85°C)
- Green parts available, see ordering information

## Functional Block Diagram




**NOTES:**

1. $A_{13}$ - $A_0$ for IDT70P269; $A_{12}$ - $A_0$ for IDT70P259; $A_{11}$ - $A_0$ for IDT70P249.
2. IRR0 and IRR1 are not available for IDT70P269.

OCTOBER 2008

## Description

The IDT70P269/259/249 is a very low power 16K/8K/4K x 16 Dual-Port Static RAM. The IDT70P269/259/249 is designed to be used as a stand-alone 256/128/64K-bit Dual-Port SRAM.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CS}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 27mW of power.

The IDT70P269/259/249 is packaged in a 100 ball 0.5mm- pitch Ball Grid Array. The package is a 1mm thick and designed to fit in wireless handset applications.

## Pin Configurations[2,3]

70P269/259/249BY
BYG-100

100-Ball 0.5mm Pitch BGA
Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | $A_{5R}$ | $A_{8R}$ | $A_{11R}$ | $\overline{UB}_R$ | $V_{SS}$ | $\overline{ADV}_R$ | $I/O_{15R}$ | $I/O_{12R}$ | $I/O_{10R}$ | $V_{SS}$ | A |
| B | $A_{3R}$ | $A_{4R}$ | $A_{7R}$ | $A_{9R}$ | $\overline{CS}_R$ | $\overline{WE}_R$ | $\overline{OE}_R$ | $V_{DDIOR}$ | $I/O_{9R}$ | $I/O_{6R}$ | B |
| C | $A_{0R}$ | $A_{1R}$ | $A_{2R}$ | $A_{6R}$ | $\overline{LB}_R$ | $IRR_1$ (1) | $I/O_{14R}$ | $I/O_{11R}$ | $I/O_{7R}$ | $V_{SS}$ | C |
| D | $ODR_4$ | $ODR_2$ | $\overline{BUSY}_R$ | $\overline{INT}_R$ | $A_{10R}$ | $A_{12R}$ (3) | $I/O_{13R}$ | $I/O_{8R}$ | $I/O_{5R}$ | $I/O_{2R}$ | D |
| E | $V_{SS}$ | DNU | $ODR_3$ | $\overline{INT}_L$ | $V_{SS}$ | $V_{SS}$ | $I/O_{4R}$ | $V_{DDIOR}$ | $I/O_{1R}$ | $V_{SS}$ | E |
| F | $\overline{SFEN}$ | $ODR_1$ | $\overline{BUSY}_L$ | $A_{1L}$ | $V_{DD}$ | $V_{SS}$ | $I/O_{3R}$ | $I/O_{0R}$ | $I/O_{15L}$ | $V_{DDIOL}$ | F |
| G | $ODR_0$ | $A_{2L}$ | $A_{5L}$ | $A_{12L}$ (3) | $\overline{OE}_L$ | $I/O_{3L}$ | $I/O_{11L}$ | $I/O_{12L}$ | $I/O_{14L}$ | $I/O_{13L}$ | G |
| H | $A_{0L}$ | $A_{4L}$ | $A_{9L}$ | $\overline{LB}_L$ | $\overline{CS}_L$ | $I/O_{1L}$ | $V_{DDIOL}$ | $MSEL_R$ | $MSEL_L$ | $I/O_{10L}$ | H |
| J | $A_{3L}$ | $A_{7L}$ | $A_{10L}$ | $IRR_0$ (2) | $V_{DD}$ | $V_{SS}$ | $I/O_{4L}$ | $I/O_{6L}$ | $I/O_{8L}$ | $I/O_{9L}$ | J |
| K | $A_{6L}$ | $A_{8L}$ | $A_{11L}$ | $\overline{UB}_L$ | $\overline{ADV}_L$ | $\overline{WE}_L$ | $I/O_{0L}$ | $I/O_{2L}$ | $I/O_{5L}$ | $I/O_{7L}$ | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

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**NOTES:-**
1. This pin is $A_{13R}$ for IDT70P269.
2. This pin is $A_{13L}$ for IDT70P269.
3. This pin is DNU for IDT70P249.
4. DNU pins are "do not use". No trace or power component can be connected to these pins.

## Pin Names

| Left Port | Right Port | Description |
|---|---|---|
| $\overline{CS}_L$ | $\overline{CS}_R$ | Chip Select (Input) |
| $\overline{WE}_L$ | $\overline{WE}_R$ | Read/Write Enable (Input) |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable (Input) |
| $A_{0L}$ - $A_{13L}$ (1) | $A_{0R}$ - $A_{13R}$ (1) | Address (Input) |
| $MSEL_L$(2) | $MSEL_R$(2) | Mode Select (Input) |
| $I/O_{0L}$ - $I/O_{15L}$ | $I/O_{0R}$ - $I/O_{15R}$ | Address/Data (Input/Output) |
| $\overline{ADV}_L$(3) | $\overline{ADV}_R$ (3) | Address Latch Enable (Input) |
| $\overline{UB}_L$ | $\overline{UB}_R$ | Upper Byte Enable (Input) |
| $\overline{LB}_L$ | $\overline{LB}_R$ | Lower Byte Enable (Input) |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag (Output) |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag (Output) |
| $\overline{SFEN}$ | | Special Function Enable (Input) |
| $IRR_0$ - $IRR_1$(4) | | Input Read Register (Inputs) |
| $ODR_0$ - $ODR_4$ | | Output Drive Register (Outputs) |
| VDD | | Core Power Supply (Input) |
| VSS | | Ground (Input) |
| $VDDIO_L$ | | Left Port Power Supply (Input) |
| $VDDIO_R$ | | Right Port Power Supply (Input) |

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**NOTES:**
1. $A_{13}$ - $A_0$ for IDT70P269; $A_{12}$ - $A_0$ for IDT70P259; $A_{11}$ - $A_0$ for IDT70P249.
2. MSEL = 0 for Standard SRAM operation, MSEL = 1 for Address/Data Mux (ADM) operation.
3. ADV is only used when the port is in ADM mode.
4. $IRR_0$ is $A_{13L}$ and $IRR_1$ is $A_{13R}$ for 70P269.

## Truth Table I: ADM Interface Read/Write Control

| Inputs | | | | | | Outputs | |
|---|---|---|---|---|---|---|---|
| $\overline{ADV}$ | $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | $I/O_0$ - $I/O_{15}$ | Mode |
| X | H | X | X | X | X | High-Z | Deselected/Power Down |
| X | X | X | H | X | X | High-Z | Output Disable |
| X | X | X | X | H | H | High-Z | Upper and Lower Bytes Deselected |
| Pulse | L | H | L | L | L | $DATA_{OUT}$ ($I/O_0$ - $I/O_{15}$) | Read Upper and Lower Bytes |
| Pulse | L | H | L | H | L | $DATA_{OUT}$ ($I/O_0$ - $I/O_7$)<br>High-Z ($I/O_8$ - $I/O_{15}$) | Read Lower Byte Only |
| Pulse | L | H | L | L | H | High-Z ($I/O_0$ - $I/O_7$)<br>$DATA_{OUT}$ ($I/O_8$ - $I/O_{15}$) | Read Upper Byte Only |
| Pulse | L | L | X | L | L | $DATA_{IN}$ ($I/O_0$ - $I/O_{15}$) | Write Upper and Lower Bytes |
| Pulse | L | L | X | H | L | $DATA_{IN}$ ($I/O_0$ - $I/O_7$)<br>High-Z ($I/O_8$ - $I/O_{15}$) | Write Lower Byte Only |
| Pulse | L | L | X | L | H | High-Z ($I/O_0$ - $I/O_7$)<br>$DATA_{IN}$ ($I/O_8$ - $I/O_{15}$) | Write Upper Byte Only |

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## Truth Table II: Standard SRAM Interface Read/Write Control

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | $I/O_0$ - $I/O_{15}$ | Mode |
| H | X | X | X | X | High-Z | Deselected/Power Down |
| X | X | H | X | X | High-Z | Output Disable |
| X | X | X | H | H | High-Z | Upper and Lower Bytes Deselected |
| L | H | L | L | L | $DATA_{OUT}$ ($I/O_0$ - $I/O_{15}$) | Read Upper and Lower Bytes |
| L | H | L | H | L | $DATA_{OUT}$ ($I/O_0$ - $I/O_7$)<br>High-Z ($I/O_8$ - $I/O_{15}$) | Read Lower Byte Only |
| L | H | L | L | H | High-Z ($I/O_0$ - $I/O_7$)<br>$DATA_{OUT}$ ($I/O_8$ - $I/O_{15}$) | Read Upper Byte Only |
| L | L | X | L | L | $DATA_{IN}$ ($I/O_0$ - $I/O_{15}$) | Write Upper and Lower Bytes |
| L | L | X | H | L | $DATA_{IN}$ ($I/O_0$ - $I/O_7$)<br>High-Z ($I/O_8$ - $I/O_{15}$) | Write Lower Byte Only |
| L | L | X | L | H | High-Z ($I/O_0$ - $I/O_7$)<br>$DATA_{IN}$ ($I/O_8$ - $I/O_{15}$) | Write Upper Byte Only |

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## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial & Industrial | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to $V_{DDIOX}$ +0.5 | V |
| $T_{BIAS}$(3) | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_{JN}$ | Junction Temperature | +150 | °C |
| $I_{OUT}$ | DC Output Current | 20 | mA |

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**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed $V_{DDIOX}$ + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period over $V_{TERM}$ = $V_{DDIOX}$ + 0.5V.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

## Capacitance

(TA = +25°C, f = 1.0MHz)

| Symbol | Parameter | Conditions[2] | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 9 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 3dV | 10 | pF |

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**NOTES:**
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

## Maximum Operating Temperature and Supply Voltage(1)

| Grade | Ambient Temperature | GND | $V_{DD}$ |
|---|---|---|---|
| Industrial | -40°C to +85°C | 0V | 1.8V ± 100mV<br>2.5V ± 100mV<br>3.0V ± 300mV |

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**NOTE :**
1. This is the parameter $T_A$. This is the "instant on" case temperature.

## DC Electrical Characteristics Over the Operating and Temperature and Supply Voltage Range($V_{DD}$ = 1.8V)

| Symbol | Parameter | P1 I/O Voltage | P2 I/O Voltage | 70P269/259/249 Ind'l Only | | | |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Unit |
| | Output High Voltage ($I_{OH}$ = -100 µA) | 1.8V (any port) | | $V_{DDIO}$ - 0.2 | — | — | V |
| | Output High Voltage ($I_{OH}$ = -2 mA) | 2.5V (any port) | | 2.0 | — | — | V |
| $V_{OH}$ | Output High Voltage ($I_{OH}$ = -2 mA) | 3.0V (any port) | | 2.1 | — | — | V |
| | Output Low Voltage ($I_{OL}$ = 100 µA) | 1.8V (any port) | | — | — | 0.2 | V |
| | Output Low Voltage ($I_{OL}$ = 2 mA) | 2.5V (any port) | | — | — | 0.4 | V |
| $V_{OL}$ | Output Low Voltage ($I_{OL}$ = 2 mA) | 3.0V (any port) | | — | — | 0.4 | V |
| | | 1.8V (any port) | | — | — | 0.2 | V |
| | | 2.5V (any port) | | — | — | 0.2 | V |
| $V_{OL}$ ODR | ODR Output Low Voltage ($I_{OL}$ = 8 mA) | 3.0V (any port) | | — | — | 0.2 | V |
| | | 1.8V (any port) | | 1.2 | — | $V_{DDIO}$ + 0.2 | V |
| | | 2.5V (any port) | | 1.7 | — | $V_{DDIO}$+ 0.3 | V |
| $V_{IH}$ | Input High Voltage | 3.0V (any port) | | 2.0 | — | $V_{DDIO}$ + 0.2 | V |
| | | 1.8V (any port) | | -0.2 | — | 0.4 | V |
| | | 2.5V (any port) | | -0.3 | — | 0.6 | V |
| $V_{IL}$ | Input Low Voltage | 3.0V (any port) | | -0.2 | — | 0.7 | V |
| | | 1.8V | 1.8V | -1 | — | 1 | |
| | | 2.5V | 2.5V | -1 | — | 1 | |
| $I_{OZ}$ | Output Leakage Current | 3.0V | 3.0V | -1 | — | 1 | µA |
| | | 1.8V | 1.8V | -1 | — | 1 | |
| | | 2.5V | 2.5V | -1 | — | 1 | |
| $I_{CEX}$ ODR | ODR Output Leakage Current $V_{OUT}$ = $V_{DDIO}$ | 3.0V | 3.0V | -1 | — | 1 | µA |
| | | 1.8V | 1.8V | -1 | — | 1 | |
| | | 2.5V | 2.5V | -1 | — | 1 | |
| $I_{IX}$ | Input Leakage Current | 3.0V | 3.0V | -1 | — | 1 | µA |

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## DC Electrical Characteristics Over the Operating and Temperature and Supply Voltage Range ($V_{DD}$ = 2.5V)

| Symbol | Parameter | P1 I/O Voltage | P2 I/O Voltage | 70P269/259/249 Ind'l Only | | | |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Unit |
| $V_{OH}$ | Output High Voltage ($I_{0H}$ = -2 mA) | 2.5V (any port) | | 2.0 | — | — | V |
| | Output High Voltage ($I_{0H}$ = -2 mA) | 3.0V (any port) | | 2.1 | — | — | V |
| $V_{OL}$ | Output Low Voltage ($I_{0L}$ = 2 mA) | 2.5V (any port) | | — | — | 0.4 | V |
| | Output Low Voltage ($I_{0L}$ = 2 mA) | 3.0V (any port) | | — | — | 0.4 | V |
| $V_{OL}$ ODR | ODR Output Low Voltage ($I_{0L}$ = 8 mA) | 2.5V (any port) | | — | — | 0.2 | V |
| | | 3.0V (any port) | | — | — | 0.2 | V |
| $V_{IH}$ | Input High Voltage | 2.5V (any port) | | 1.7 | — | $V_{DDIO}$+ 0.3 | V |
| | | 3.0V (any port) | | 2.0 | — | $V_{DDIO}$ + 0.2 | V |
| $V_{IL}$ | Input Low Voltage | 2.5V (any port) | | -0.3 | — | 0.6 | V |
| | | 3.0V (any port) | | -0.2 | — | 0.7 | V |
| $I_{OZ}$ | Output Leakage Current | 2.5V | 2.5V | -1 | — | 1 | µA |
| | | 3.0V | 3.0V | -1 | — | 1 | |
| $I_{CEX}$ ODR | ODR Output Leakage Current $V_{OUT}$ = $V_{DDIO}$ | 2.5V | 2.5V | -1 | — | 1 | µA |
| | | 3.0V | 3.0V | -1 | — | 1 | |
| $I_{IX}$ | Input Leakage Current | 2.5V | 2.5V | -1 | — | 1 | µA |
| | | 3.0V | 3.0V | -1 | — | 1 | |

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## DC Electrical Characteristics Over the Operating and Temperature and Supply Voltage Range ($V_{DD}$ = 3.0V)

| Symbol | Parameter | P1 I/O Voltage | P2 I/O Voltage | 70P269/259/249 Ind'l Only | | | |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Unit |
| $V_{OH}$ | Output High Voltage ($I_{0H}$ = -2 mA) | 3.0V (any port) | | 2.1 | — | — | V |
| $V_{OL}$ | Output Low Voltage ($I_{0L}$ = 2 mA) | 3.0V (any port) | | — | — | 0.4 | V |
| $V_{OL}$ ODR | ODR Output Low Voltage ($I_{0L}$ = 8 mA) | 3.0V (any port) | | — | — | 0.2 | V |
| $V_{IH}$ | Input High Voltage | 3.0V (any port) | | 2.0 | — | $V_{DDIO}$ + 0.2 | V |
| $V_{IL}$ | Input Low Voltage | 3.0V (any port) | | -0.2 | — | 0.7 | V |
| $I_{OZ}$ | Output Leakage Current | 3.0V | 3.0V | -1 | — | 1 | µA |
| $I_{CEX}$ ODR | ODR Output Leakage Current $V_{OUT}$ = $V_{DDIO}$ | 3.0V | 3.0V | -1 | — | 1 | µA |
| $I_{IX}$ | Input Leakage Current | 3.0V | 3.0V | -1 | — | 1 | µA |

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# DC Electrical Characteristics Over the Operating and Temperature and Supply Voltage Range

| Symbol | Parameter | Test Condition [1] | VDD | 70P269/259/249 Ind'l Only | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | 65 ns | | 90 ns | | |
| | | | | Typ. | Max. | Typ. | Max. | |
| $I_{DD}$ | Dynamic Operating Current | $V_{DD}$ = MAX, $I_{OUT}$ = 0mA | 1.8V | 25 | 40 | 15 | 25 | mA |
| | | | 2.5V | 39 | 55 | 28 | 40 | |
| | | | 3.0V | 49 | 70 | 42 | 60 | |
| $I_{SB1}$ | Standby Current (Both Ports Inactive) | $\overline{CS}_R$ and $\overline{CS}_L \geq V_{DDIO}$ - 0.2V, MSELL and MSELR $\leq$ 0.2V or $\geq V_{DDIO}$ - 0.2V, f = $f_{MAX}$ | 1.8V | 2 | 6 | 2 | 6 | µA |
| | | | 2.5V | 6 | 8 | 6 | 8 | |
| | | | 3.0V | 7 | 10 | 7 | 10 | |
| $I_{SB2}$ | Standby Current (One Port Active, One Port Inactive) | $\overline{CS}_R$ or $\overline{CS}_L \geq V_{DDIO}$ - 0.2V, f = $f_{MAX}$ | 1.8V | 8.5 | 18 | 8.5 | 14 | mA |
| | | | 2.5V | 21 | 30 | 18 | 25 | |
| | | | 3.0V | 28 | 40 | 25 | 35 | |
| $I_{SB3}$ | Full Standby Current (Both Ports Inactive - CMOS Level Inputs) | $\overline{CS}_R$ and $\overline{CS}_L \geq V_{DDIO}$ - 0.2V, MSELL and MSELR $\leq$ 0.2V or $\geq V_{DDIO}$ - 0.2V, f = 0 | 1.8V | 2 | 6 | 2 | 6 | µA |
| | | | 2.5V | 4 | 6 | 4 | 6 | |
| | | | 3.0V | 6 | 8 | 6 | 8 | |
| $I_{SB4}$ | Standby Current (One Port Active, One Port Inactive - CMOS Level Inputs) | $\overline{CS}_L$ or $\overline{CS}_R \geq V_{DDIO}$ - 0.2V, f = $f_{MAX}$ | 1.8V | 8.5 | 18 | 8.5 | 14 | mA |
| | | | 2.5V | 21 | 30 | 18 | 25 | |
| | | | 3.0V | 28 | 40 | 25 | 35 | |

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**NOTE :**

1. $f_{MAX}$ = 1/$t_{RC}$ = All inputs cycling at f = 1/$t_{RC}$ (except output enable). f=0 means no address or control lines change. This applied only to inputs at CMOS level standby $I_{SB3}$.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V/GND to 2.5V/GND to 1.8V |
| Input Rise/Fall Times | 3ns Max. |
| Input Timing Reference Levels | 1.5V/1.25V/0.9V |
| Output Reference Levels | 1.5V/1.25V/0.9V |
| Output Load | Figure 1 |

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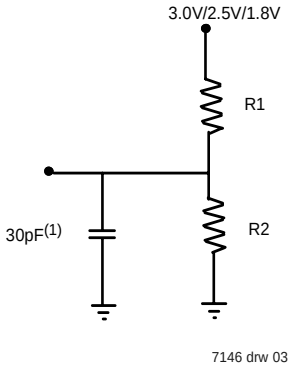


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| | 3.0V/2.5V | 1.8V |
|---|---|---|
| R1 | 1022Ω | 13500Ω |
| R2 | 729Ω | 10800Ω |

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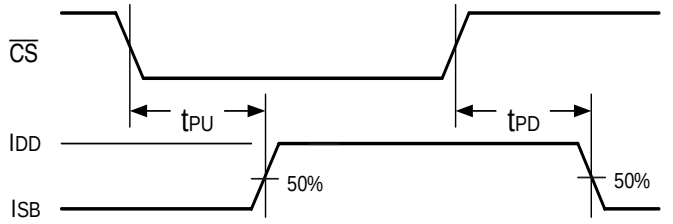
**Figure 1. AC Output Test Load (5pF for $t_{LZ}$, $t_{HZ}$, $t_{WZ}$, $t_{OW}$)**

## Timing of Power-Up Power-Down




7146 drw 04

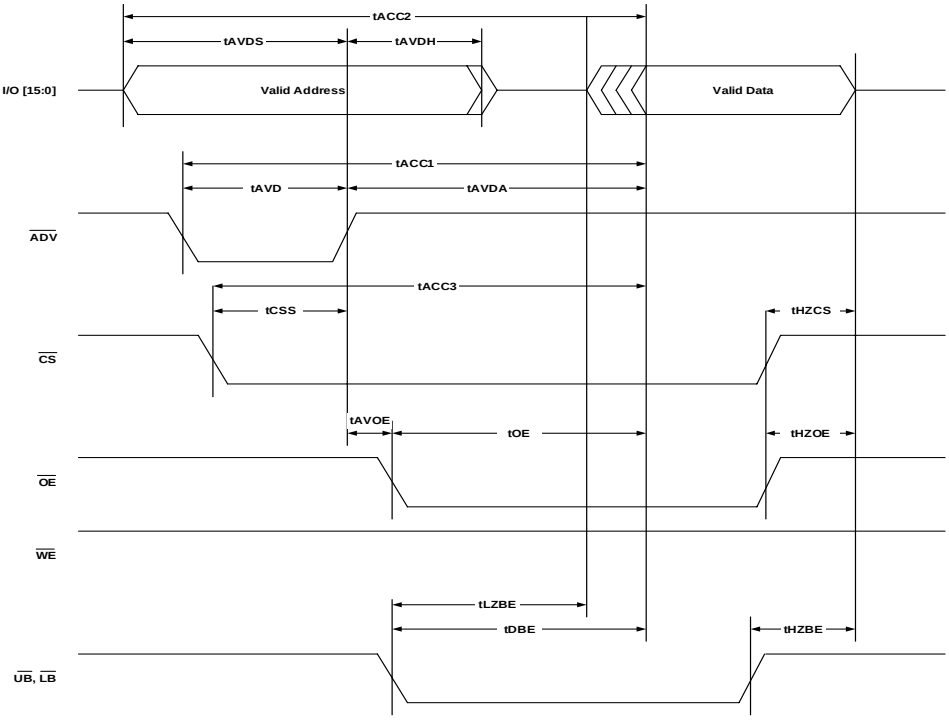
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

| Symbol | Parameter | 70P269/259/249 | | | | Unit |
|---|---|---|---|---|---|---|
| | | 65 ns | | 90 ns | | |
| | | Min. | Max. | Min. | Max. | |
| **ADM Port Read Cycle (2)** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 65 | — | 90 | — | ns |
| $t_{ACC1}$ | Random Access $\overline{ADV}$ Low to Data Valid | — | 65 | — | 90 | ns |
| $t_{ACC2}$ | Random Access Address to Data Valid | — | 65 | — | 90 | ns |
| $t_{ACC3}$ | Random Access $\overline{CS}$ to Data Valid | — | 65 | — | 90 | ns |
| $t_{AVDA}$ | Random Access $\overline{ADV}$ High to Data Valid | — | 35 | — | 50 | ns |
| $t_{AVD}$ | $\overline{ADV}$ Low Pulse | 15 | — | 20 | — | ns |
| $t_{AVDS}$ | Address Set-up to $\overline{ADV}$ Rising Edge | 15 | — | 20 | — | ns |
| $t_{AVDH}$ | Address Hold from $\overline{ADV}$ Rising Edge | 3 | — | 5 | — | ns |
| $t_{CSS}$ | $\overline{CS}$ Set-up to $\overline{ADV}$ Rising Edge | 7 | — | 10 | — | ns |
| $t_{OE}$ | $\overline{OE}$ Low to Data Valid | — | 35 | — | 50 | ns |
| $t_{LZOE}$(3) | $\overline{OE}$ Low to I/O Low-Z | 3 | — | 5 | — | ns |
| $t_{HZOE}$(3) | $\overline{OE}$ High to I/O High-Z | — | 15 | — | 25 | ns |
| $t_{HZCS}$(3) | $\overline{CS}$ High to I/O High-Z | — | 15 | — | 25 | ns |
| $t_{DBE}$ | $\overline{UB}$/$\overline{LB}$ Low to I/O Valid | — | 35 | — | 50 | ns |
| $t_{LZBE}$(3) | $\overline{UB}$/$\overline{LB}$ Low to I/O Low-Z | 3 | — | 5 | — | ns |
| $t_{HZBE}$(3) | $\overline{UB}$/$\overline{LB}$ High to I/O High-Z | — | 15 | — | 25 | ns |
| $t_{AVOE}$ | $\overline{ADV}$ High to $\overline{OE}$ Low | 0 | — | 0 | — | ns |
| $t_{PU}$ | Chip Enable to Power Up Time | 0 | — | 0 | — | ns |
| $t_{PD}$ | Chip Disable to Power Down Time | — | 65 | — | 90 | ns |
| **Standard Port Read Cycle (4)** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 40 | — | 60 | — | ns |
| $t_{AA}$ | Address to Data Valid | — | 40 | — | 60 | ns |
| $t_{OHA}$ | Output Hold from Address Change | 5 | — | 5 | — | ns |
| $t_{ACS}$ | $\overline{CS}$ to Data Valid | — | 40 | — | 60 | ns |
| $t_{DOE}$ | $\overline{OE}$ Low to Data Valid | — | 25 | — | 35 | ns |
| $t_{LZOE}$(3) | $\overline{OE}$ Low to Data Low-Z | 5 | — | 5 | — | ns |
| $t_{HZOE}$(3) | $\overline{OE}$ High to Data High-Z | — | 10 | — | 30 | ns |
| $t_{LZCS}$(3) | $\overline{CS}$ Low to Data Low-Z | 5 | — | 5 | — | ns |
| $t_{HZCS}$(3) | $\overline{CS}$ Low to Data High-Z | — | 10 | — | 30 | ns |
| $t_{LZBE}$(3) | $\overline{UB}$/$\overline{LB}$ Low to Data Low-Z | 5 | — | 5 | — | ns |
| $t_{HZBE}$(3) | $\overline{UB}$/$\overline{LB}$ High to Data High-Z | — | 10 | — | 30 | ns |
| $t_{ABE}$ | $\overline{UB}$/$\overline{LB}$ Access Time | — | 40 | — | 60 | ns |

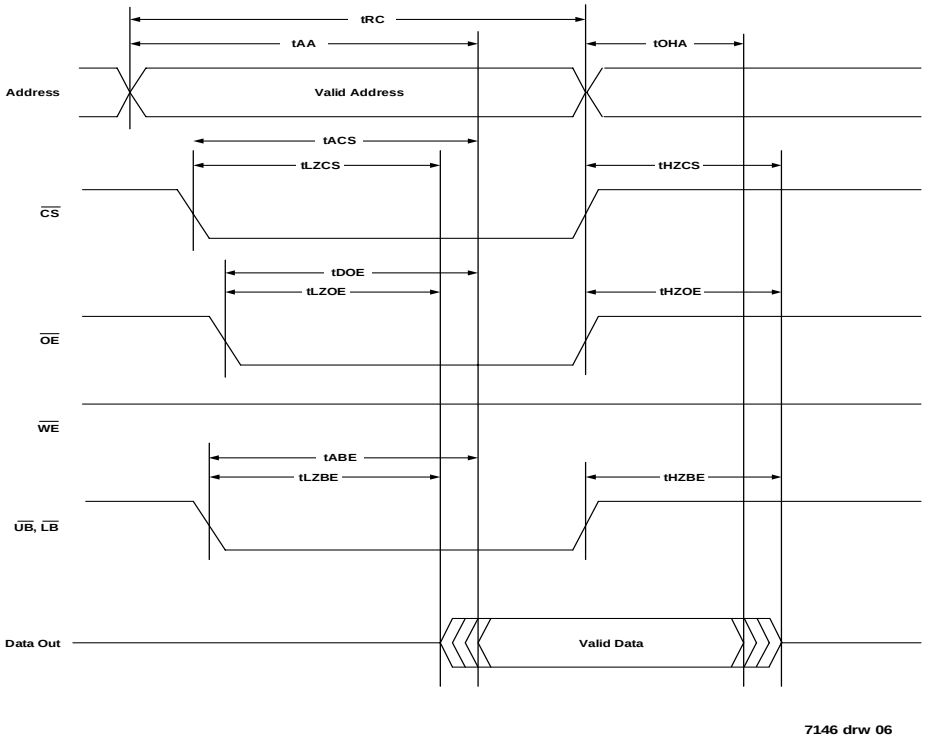
7146 tbl 12

**NOTES:**
1. VDD = 1.8V
2. ADM port timing applies to the left or right port when configured to ADM mode.
3. This parameter is guaranteed by design and is not tested.
4. Standard SRAM port timing applies to the left or right port when configured to standard SRAM mode.

## ADM Port Read Cycle (Either Port Access, $\overline{WE}$ High)




## Standard Port Read Cycle (Right Port Access, $\overline{WE}$ High)



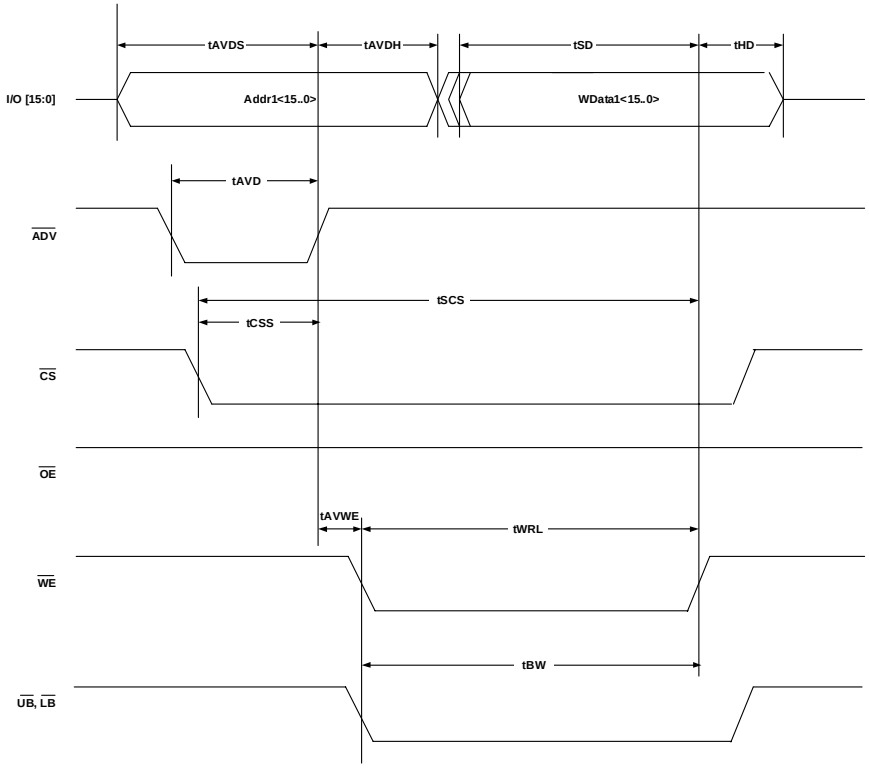
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

| Symbol | Parameter | 70P269/259/249 | | | | Unit |
|---|---|---|---|---|---|---|
| | | 65 ns | | 90 ns | | |
| | | Min. | Max. | Min. | Max. | |
| **ADM Port Write Cycle (2)** | | | | | | |
| $t_{WC}$ | Write Cycle Time | 65 | — | 90 | — | ns |
| $t_{SCS}$ | $\overline{CS}$ Low to Write End | 65 | — | 90 | — | ns |
| $t_{AVD}$ | $\overline{ADV}$ Low Pulse | 15 | — | 20 | — | ns |
| $t_{AVDS}$ | Address Set-up to $\overline{ADV}$ Rising Edge | 15 | — | 20 | — | ns |
| $t_{AVDH}$ | Address Hold from $\overline{ADV}$ Rising Edge | 3 | — | 5 | — | ns |
| $t_{CSS}$ | $\overline{CS}$ Set-up to $\overline{ADV}$ Rising Edge | 7 | — | 10 | — | ns |
| $t_{WRL}$ | $\overline{WE}$ Pulse Width | 28 | — | 45 | — | ns |
| $t_{BW}$ | $\overline{UB}$/$\overline{LB}$ Low to Write End | 28 | — | 45 | — | ns |
| $t_{SD}$ | Data Set-up to Write End | 20 | — | 30 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{LZWE}$(3) | $\overline{WE}$ High to I/O Low-Z | 0 | — | 0 | — | ns |
| $t_{AVWE}$ | $\overline{ADV}$ High to WE Low | 0 | — | 0 | — | ns |
| $t_{WODR}$ | Write End to ODR Valid | — | 40 | — | 60 | ns |
| **Standard Port Write Cycle (4)** | | | | | | |
| $t_{WC}$ | Write Cycle Time | 40 | — | 60 | — | ns |
| $t_{SCS}$ | $\overline{CS}$ Low to Write End | 30 | — | 50 | — | ns |
| $t_{AW}$ | Address Valid to Write End | 30 | — | 50 | — | ns |
| $t_{HA}$ | Address Hold to Write End | 0 | — | 0 | — | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | — | 0 | — | ns |
| $t_{WRL}$ | Write Pulse Width | 25 | — | 45 | — | ns |
| $t_{SD}$ | Data Set-up to Write End | 20 | — | 30 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{HZWE}$(3) | $\overline{WE}$ Low to Data High-Z | — | 15 | — | 25 | ns |
| $t_{LZWE}$(3) | $\overline{WE}$ High to Data Low-Z | 0 | — | 0 | — | ns |
| $t_{WODR}$ | Write End to ODR Valid | — | 40 | — | 60 | ns |

7146 tbl 13

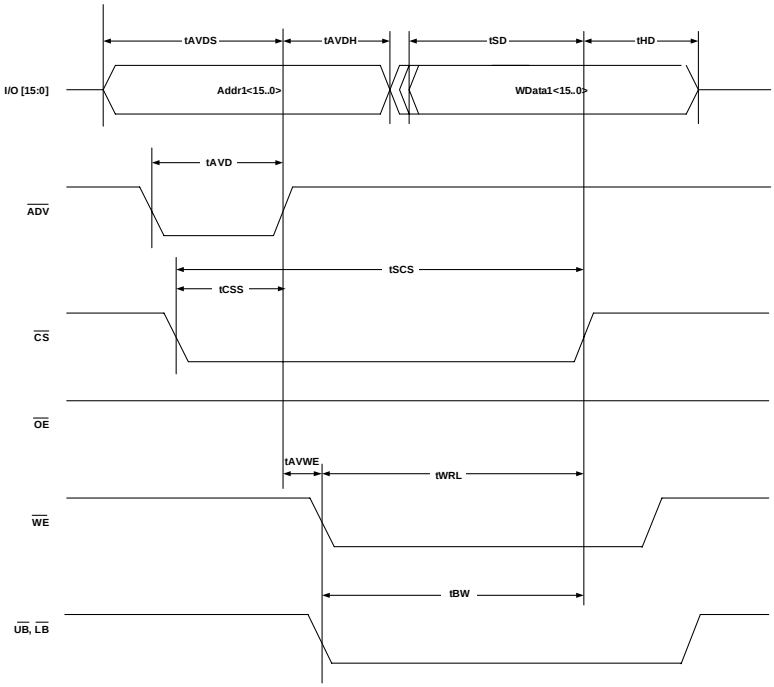
**NOTES:**
1. VDD = 1.8V
2. ADM port timing applies to the left or right port when configured to ADM mode.
3. This parameter is guaranteed by design and is not tested.
4. Standard SRAM port timing applies to the left or right port when configured to standard SRAM mode.

## ADM Port Write Cycle (Either Port Access, $\overline{WE}$ Controlled, $\overline{OE}$ High)



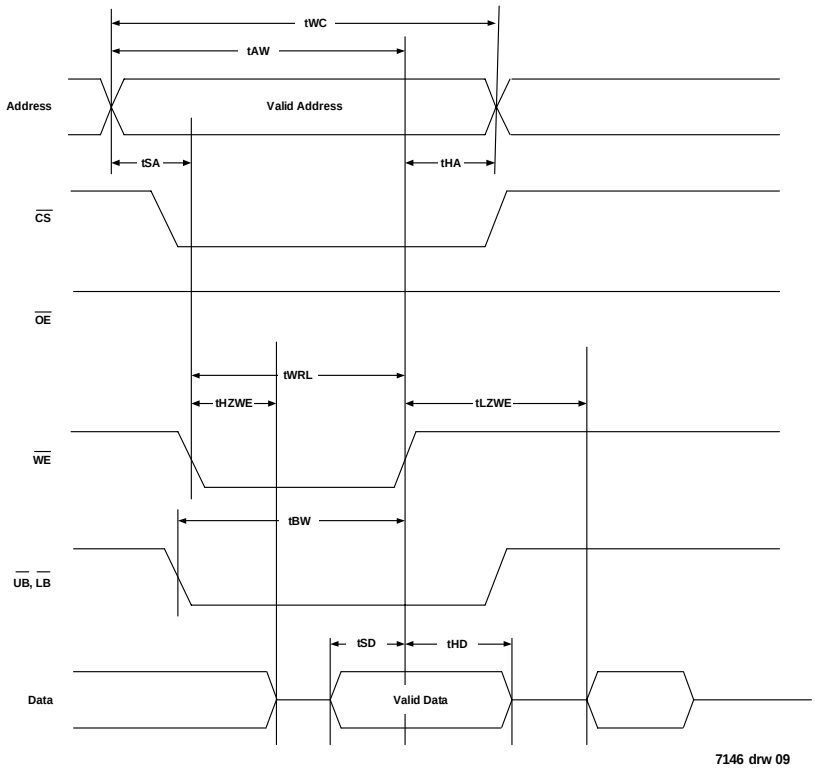

7146 drw 07

## ADM Port Write Cycle (Either Port Access, $\overline{CS}$ Controlled, $\overline{OE}$ High)



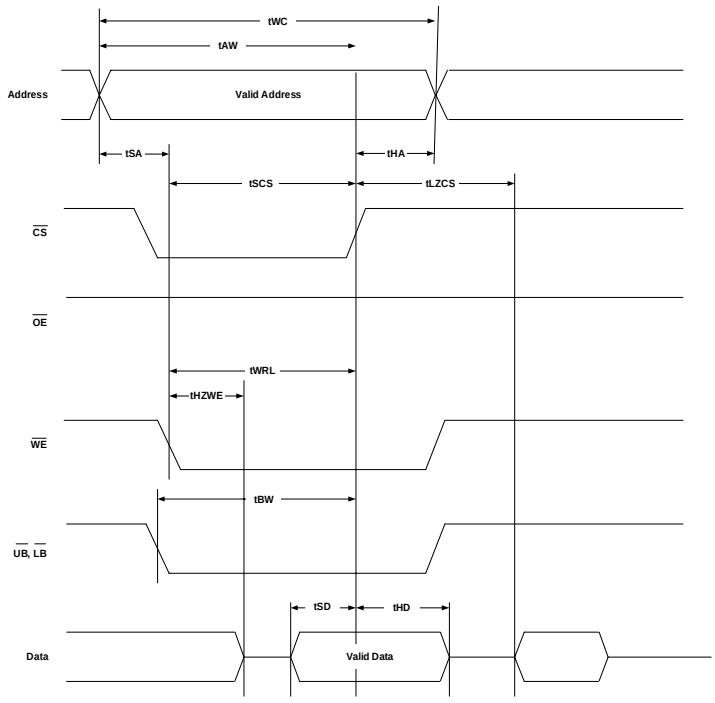

7146 drw 08

## Standard Port Write Cycle (Either Port Access, $\overline{WE}$ Controlled)




7146 drw 09

## Standard Port Write Cycle (Either Port Access, $\overline{CS}$ Controlled)




7146 drw 10

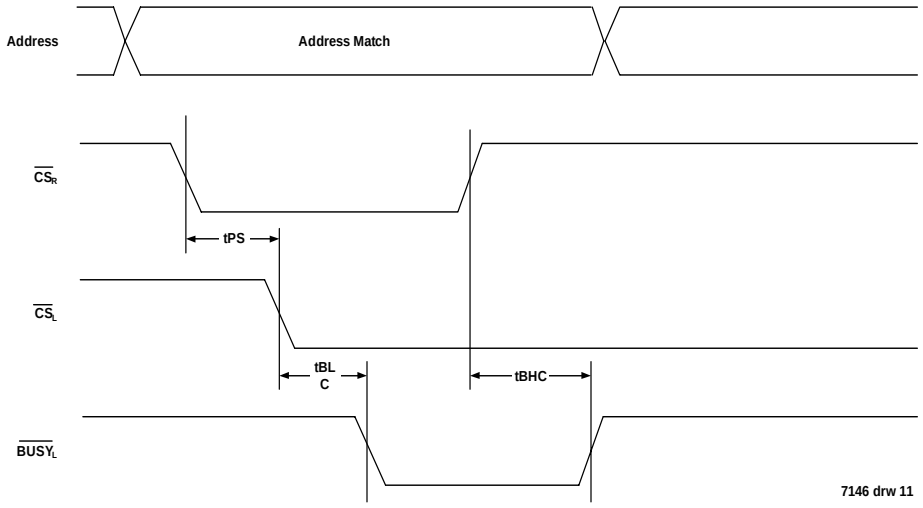
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

| Symbol | Parameter | 70P269/259/249 | | | | Unit |
|---|---|---|---|---|---|---|
| | | 65 ns | | 90 ns | | |
| | | Min. | Max. | Min. | Max. | |
| **Arbitration Timing** | | | | | | |
| $t_{BLA}$ | $\overline{BUSY}$ Low from Address Match | — | 30 | — | 50 | ns |
| $t_{BHA}$ | $\overline{BUSY}$ High from Address Match | — | 30 | — | 50 | ns |
| $t_{BLC}$ | $\overline{BUSY}$ Low from $\overline{CS}$ Low | — | 30 | — | 50 | ns |
| $t_{BHC}$ | $\overline{BUSY}$ High from $\overline{CS}$ High | — | 30 | — | 50 | ns |
| $t_{PS}$(2) | Port Set-up Priority | 5 | — | 5 | — | ns |
| $t_{BDD}$ | $\overline{BUSY}$ High to Data Valid | — | 30 | — | 50 | ns |
| $t_{WDD}$ | Write Pulse to Data Delay | — | 55 | — | 85 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Valid | — | 45 | — | 70 | ns |

7146 tbl 14

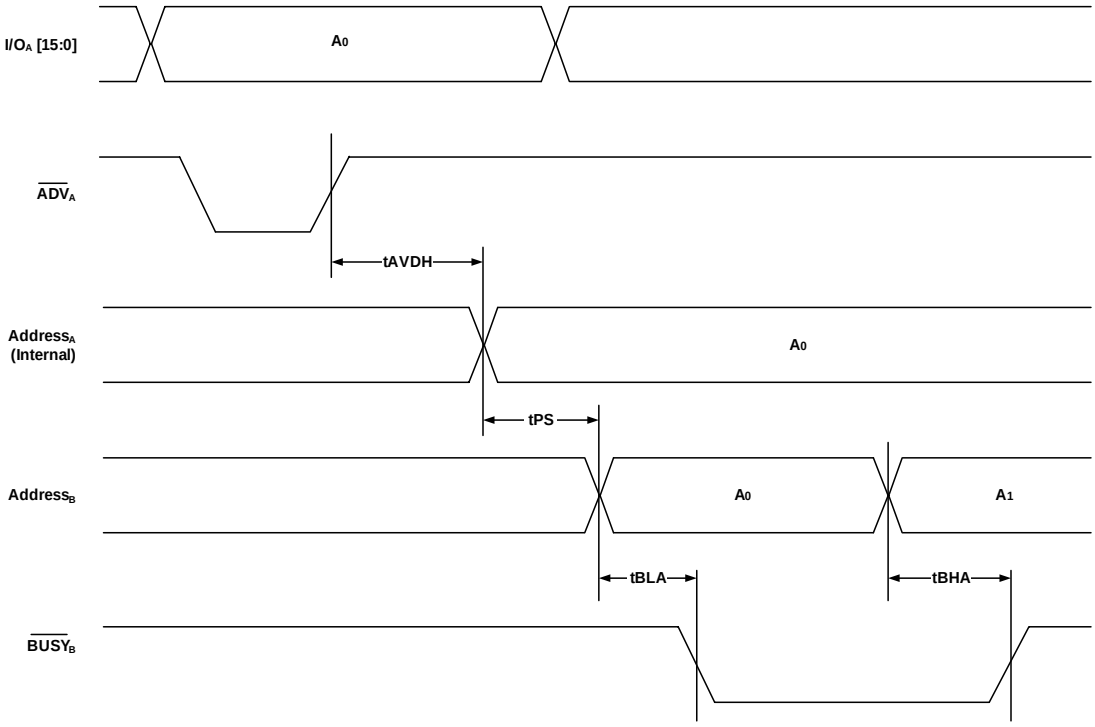
**NOTES:**
1. VDD = 1.8V.
2. Add 2 ns to this parameter if $V_{DD}$ and $V_{DDIOR}$ are <1.8V, and $V_{DDIOL}$ is >2.5V at temperature <0°C.

## Arbitration Timing

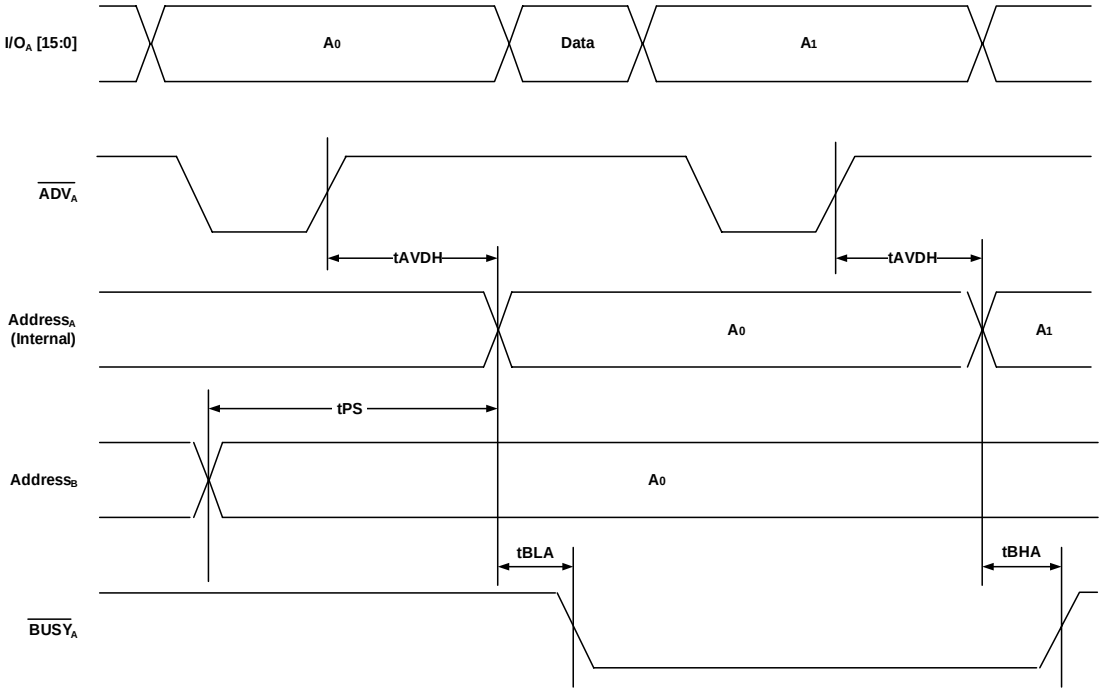


# Arbitration Timing
# (Address Controlled with Port A ADM and Port B STD Configuration)

**Port A Address Valid First**

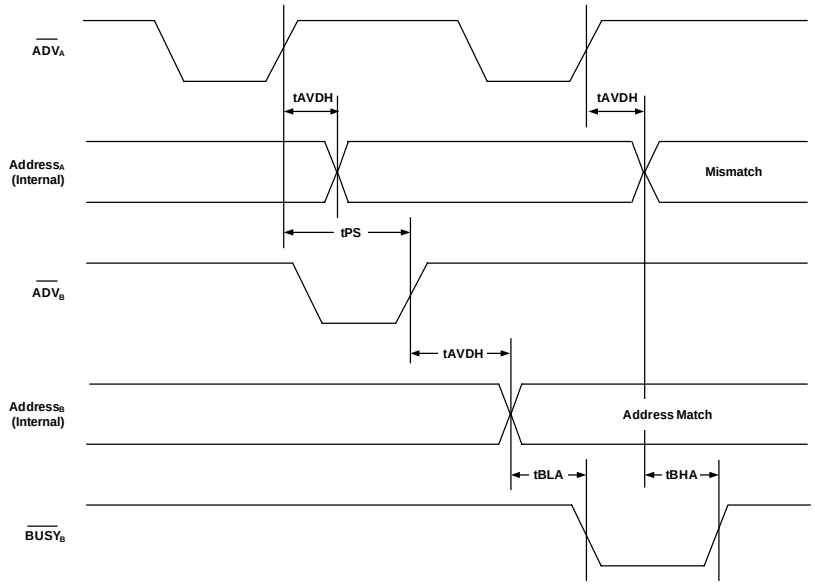



**Port B Address Valid First**




7146 drw 12

## Arbitration Timing
## (Address Controlled with Port A ADM and Port B ADM Configuration)

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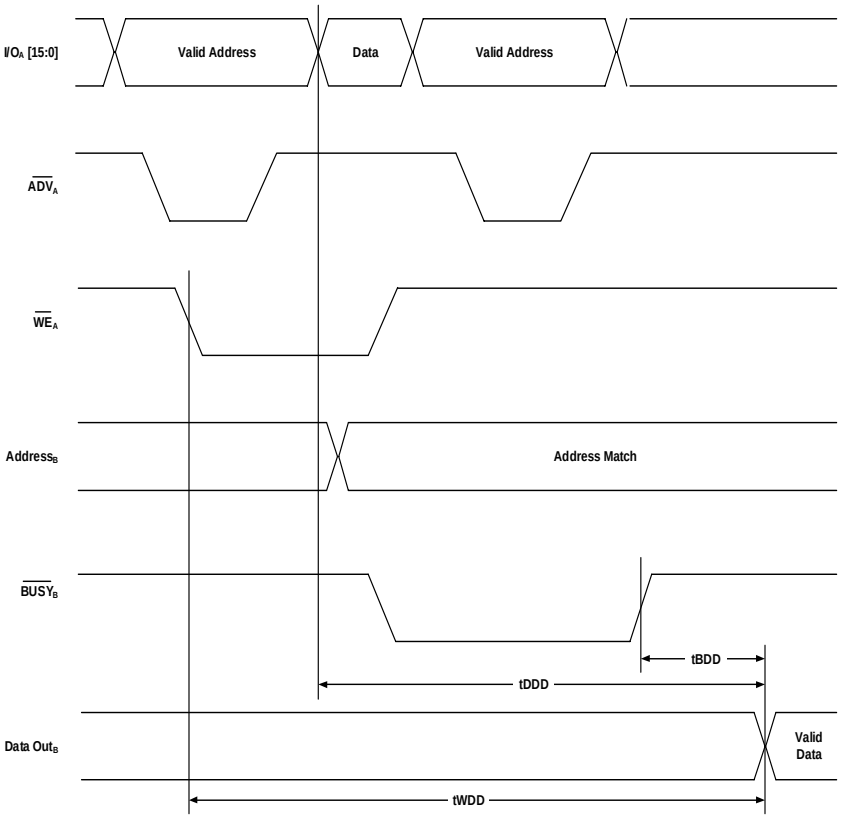
## Read with BUSY Timing

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**NOTES:**
1. $t_{WDD}$ is measured from the time WE goes low on Port A to the beginning of valid data on Port B whether the ports are in ADM or Standard mode.
2. $t_{DDD}$ is measured from the end of valid address on Port A to the beginning of valid data on Port B whether the ports are in ADM or Standard mode.
3. $t_{BDD}$ is measured from the time BUSY goes high on Port B to the beginning of valid data on Port B whether the ports are in ADM or Standard mode.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1)

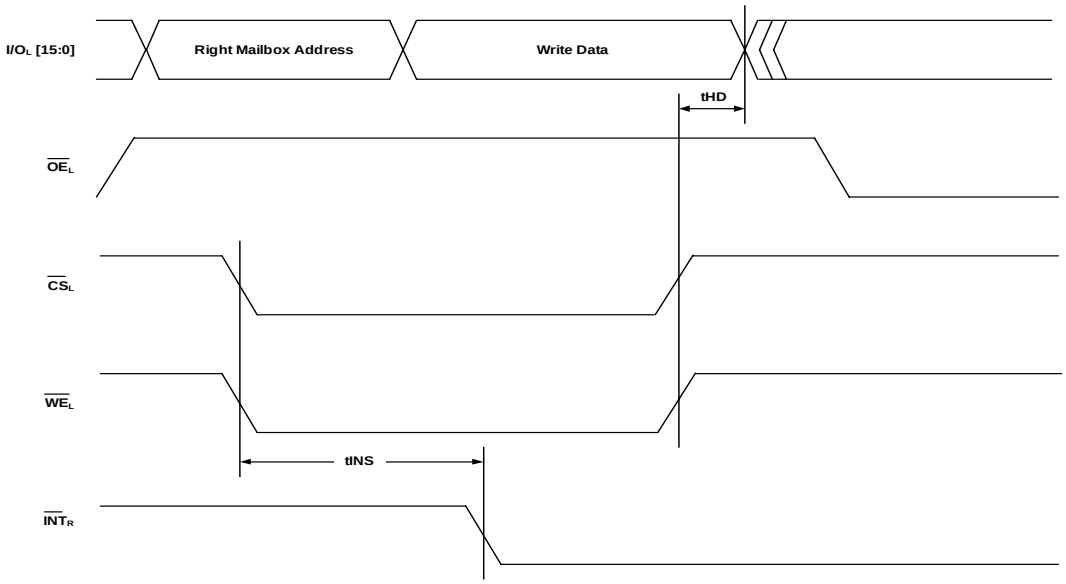
| Symbol | Parameter | 70P269/259/249 | | | | Unit |
|---|---|---|---|---|---|---|
| | | 65 ns | | 90 ns | | |
| | | Min. | Max. | Min. | Max. | |
| **Interrupt Timing** | | | | | | |
| $t_{INS}$ | $\overline{INT}$ Set Time | — | 35 | — | 55 | ns |
| $t_{INR}$ | $\overline{INT}$ Reset Time | — | 35 | — | 55 | ns |

7146 tbl 15

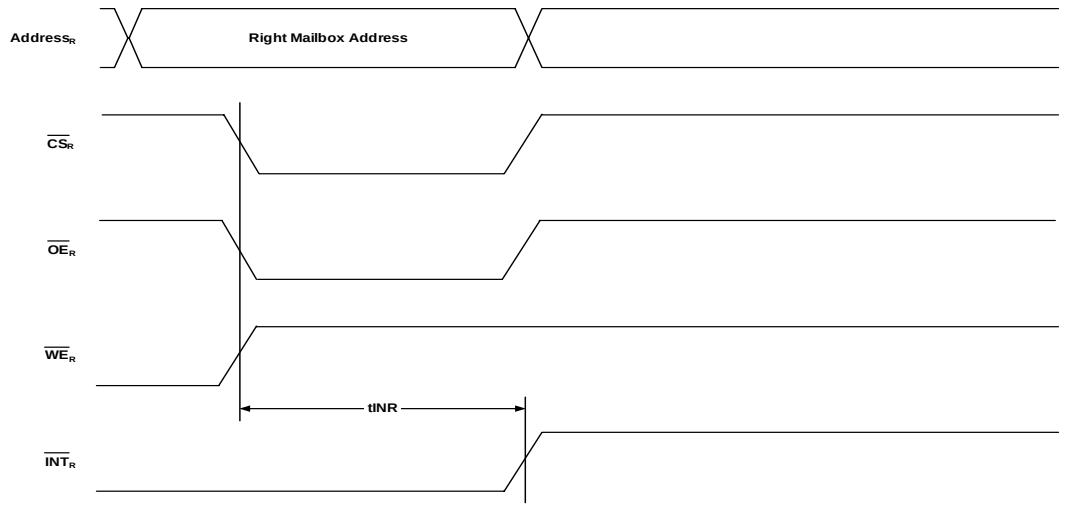
**NOTE:**
1. VDD = 1.8V

## Interrupt Timing

**Left Port Writes to Right Mailbox Setting $\overline{INT}_R$**




**Right Port Reads Right Mailbox Clearing $\overline{INT}_R$**

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## Truth Table III — Interrupt Flag[1]

| Left Port | | | | | Right Port | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{WE}$ | $\overline{CS}$ | $\overline{OE}_L$ | $A_{13L}$-$A_{0L}$ | $\overline{INT}_L$ | $\overline{WE}$ | $\overline{CS}$ | $\overline{OE}_R$ | $A_{13R}$-$A_{0R}$ | $\overline{INT}_R$ | Function |
| L | L | X | 3FFF[2] | X | X | X | X | X | L | Set Right $\overline{INT}_R$ Flag |
| X | X | X | X | X | X | L | L | 3FFF[2] | H | Reset Right $\overline{INT}_R$ Flag |
| X | X | X | X | L | L | L | X | 3FFE[3] | X | Set Left $\overline{INT}_L$ Flag |
| X | L | L | 3FFE[3] | H | X | X | X | X | X | Reset Left $\overline{INT}_L$ Flag |

7146 tbl 16

**NOTES:**
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = $V_{IH}$.
2. 3FFF for 70P269, 1FFF for 70P259, FFF for 70P249.
3. 3FFE for 70P269, 1FFE for 70P259, FFE for 70P249.

## Truth Table IV — Address BUSY Arbitration

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| $\overline{CS}_L$ | $\overline{CS}_R$ | Address Match Left/Right Port | $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Function |
| X | X | NO MATCH | H | H | Normal |
| H | X | MATCH | H | H | Normal |
| X | H | MATCH | H | H | Normal |
| L | L | MATCH | (1) | (1) | Write Inhibit[2] |

7146 tbl 17

**NOTES:**
1. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If $t_{PS}$ is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be LOW simultaneously.
2. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

## Truth Table V — Input Read Register Operation(3)

| $\overline{SFEN}$ | $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | ADDR | $I/O_0$-$I/O_1$ | $I/O_2$-$I/O_{15}$ | Mode |
|---|---|---|---|---|---|---|---|---|---|
| H | L | H | L | L(1) | L(1) | x0000 - Max | VALID(1) | VALID(1) | Standard Memory Access |
| L | L | H | L | X | L | x0000 | VALID(2) | VALID(4) | IRR Read(3) |

7146 tbl 18

**NOTES:**
1. $\overline{UB}$ or $\overline{LB}$ = $V_{IL}$. If $\overline{LB}$ = $V_{IL}$, then $I/O_0$ - $I/O_7$ are VALID. If $\overline{UB}$ = $V_{IL}$, then $I/O_8$ - $I/O_{15}$ are VALID.
2. $\overline{LB}$ must be active ($\overline{LB}$ = $V_{IL}$) for these bits to be valid.
3. $\overline{SFEN}$ = $V_{IL}$ to activate IRR reads.
4. Valid data bits from memory.

## Truth Table VI — Output Drive Register Operation(5)

| $\overline{SFEN}$ | $\overline{CE}$ | R/$\overline{W}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | ADDR | $I/O_0$-$I/O_4$ | $I/O_5$-$I/O_{15}$ | Mode |
|---|---|---|---|---|---|---|---|---|---|
| H | L | H | X(1) | L(2) | L(2) | x0000 - Max | VALID(2) | VALID(2) | Standard Memory Access |
| L | L | L | X | X | L | x0001 | VALID(3) | VALID(4) | ODR Write(4,5) |
| L | L | H | L | X | L | x0001 | VALID(3) | VALID(6) | ODR Read(5) |

7146 tbl 19

**NOTES:**
1. Output enable must be low (OE = Vil) during reads for valid data to be output.
2. $\overline{UB}$ or $\overline{LB}$ = $V_{IL}$. If $\overline{LB}$ = $V_{IL}$, then $I/O_0$ - $I/O_7$ are VALID. If $\overline{UB}$ = $V_{IL}$, then $I/O_8$ - $I/O_{15}$ are VALID.
3. $\overline{LB}$ must be active ($\overline{LB}$ = $V_{IL}$) for these bits to be valid.
4. During ODR writes data will also be written to the memory.
5. $\overline{SFEN}$ = $V_{IL}$ to activate ODR reads and writes.
6. Valid data bits from memory.

## Functional Description

The IDT70P269/259/249 are low-power CMOS 16K/8K/4K x 16 dual-port static RAMs. The two ports support user configurable standard SRAM or time-multiplexed address and data (ADM) interfaces. The two ports provide separate control, address, and I/O pins that permit independent, asynchronous read and write access to any memory location. The IDT70P269/259/249 has an automatic power-down feature controlled by $\overline{CS}$. The $\overline{CS}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CS}$ HIGH).

## Power Supply

The core voltage ($V_{DD}$) can be 1.8V, 2.5V or 3.0V, as long as it is lower than or equal to the I/O voltage. Each port can operate on independent I/O voltages. This is determined by what is connected to the $V_{DDIOL}$ and $V_{DDIOR}$ pins. The supported I/O standards are 1.8V/2.5V LVCMOS and 3.0V LVTTL.

The IDT70P269/259/249 includes power supply isolation functionality which aids system power management. $V_{DD}$, $V_{DDIOR}$ and $V_{DDIOL}$ can all be independently powered up/down which allows either port and/or the core to be powered down when not in use. If $V_{DDIOX}$ is powered down, but $V_{DD}$ remains powered up all inputs to the core will be forced to deasserted states at full swing DC values to minimize leakage current and active power consumption. If $V_{DD}$ is powered down but $V_{DDIOX}$ remain powered up, all outputs for the port(s) in question will remain in the state they were in prior to power down.

## ADM Interface Read/Write Operation

The description of this section is applicable to either port when configured in ADM mode.

Three control signals, $\overline{ADV}$, $\overline{WE}$, and $\overline{CS}$ are used to perform the read/write operation. Address signals are first applied to the I/O bus along with $\overline{CS}$ LOW. The addresses are loaded from the I/O bus in response to the rising edge of the Address Latch Enable ($\overline{ADV}$) signal. It is necessary to meet the set-up ($t_{AVDS}$) and hold ($t_{AVDH}$) times given in the AC specifications with valid address information in order to properly latch the addresses.

Once the address signals are latched in, a read operation is issued when $\overline{WE}$ stays HIGH. The I/O bus becomes HIGH-Z once the address signals meeting $t_{AVDH}$. The read data is driven on the I/O bus $t_{OE}$ after the $\overline{OE}$ is asserted LOW, and held until $t_{HZOE}$ or $t_{HZCS}$ after the rising edge of $\overline{OE}$ or $\overline{CS}$, whichever comes first.

A write operation is issued when $\overline{WE}$ is asserted LOW. The write data is applied to the I/O bus right after address meets the hold time ($t_{AVDH}$). And write data is written with the rising edge of either $\overline{WE}$ or $\overline{CS}$, whichever comes first, and meets data set-up ($t_{SD}$) and hold ($t_{HD}$) times.

A write operation is issued when $\overline{WE}$ is asserted LOW. The write data is applied to the I/O bus right after address meets the hold time ($t_{AVDH}$). And write data is written with the rising edge of either $\overline{WE}$ or $\overline{CS}$, whichever comes first, and meets data set-up ($t_{SD}$) and hold ($t_{HD}$) times.

## Standard SRAM Interface Read/Write Operation

The description of this section is applicable to either port when configured to operate in Standard SRAM mode. Read/write operation with standard SRAM interface configuration is the same as the ADM port except addresses are presented on the address bus. Operation is controlled by $\overline{CS}$, $\overline{OE}$ and $\overline{WE}$. A read operation is issued when WE is asserted HIGH. A write operation is issued when $\overline{WE}$ is asserted LOW. The I/O bus is the destination for read data and the source data for write data when the read operation is issued. However, write data needs to be driven to the I/O when the write operation is issued.

## Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FFE (HEX) (1FFE for IDT70P259 and FFE for IDT70P249), where a write is defined as the $\overline{CS}$=$\overline{WE}$=$V_{IL}$ per Truth Table III. The left port clears the interrupt by accessing address location 3FFE when $\overline{CS}_R$ = $\overline{OE}_R$ = $V_{IL}$, $\overline{WE}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FFF (HEX) (1FFF for IDT70P259 and FFF for IDT70P249) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FFF. The message (16 bits) at 3FFE or 3FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

## Busy Logic

Busy Logic provides a hardware indication that both ports of the SRAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the SRAM is "busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation.

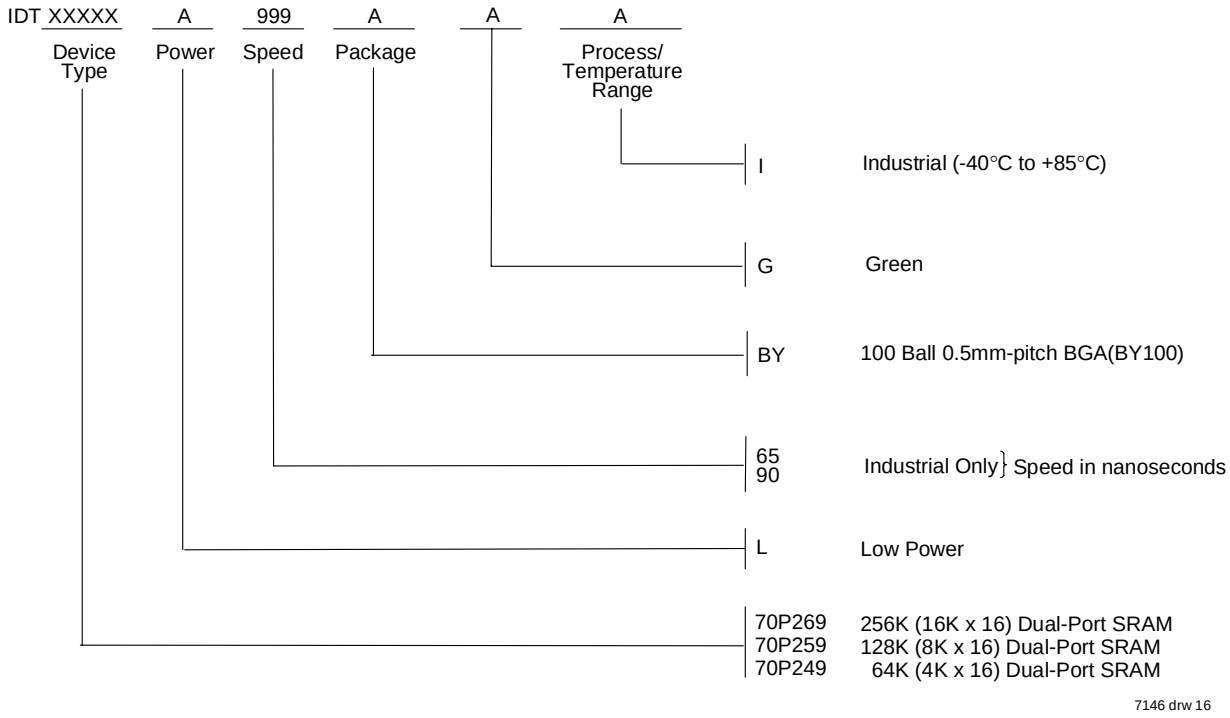
## Input Read Register

The Input Read Register (IRR) of the IDT70P269/259/249 captures the status of two external binary input devices connected to the Input Read pins (e.g. DIP switches). The contents of the IRR are read as a standard memory access to address x0000 from either port and the data is output via the standard I/Os (Truth Table V). During Input Register reads $I/O_0$ - $I/O_1$ are valid bits and $I/O_2$ - $I/O_{15}$ are read from the memory. Writes to address x0000 are normal memory operation. When $\overline{SFEN} = V_{IH}$, the IRR is inactive and address x0000 can be used as part of the main memory. The IRR inputs will be 1.8V/2.5V LVCMOS or 3.0V LVTTL, depending on the core voltage supply. Refer to Truth Table V for Input Read Register operation.

## Output Drive Register

The Output Drive Register (ODR) of the IDT70P269/259/249 determines the state of up to five external binary-state devices by providing a path to $V_{SS}$ for the external circuit. The five external devices supported by the ODR can operate at different voltages ($1.5V \leq V_{SUPPLY} \leq 3.5V$), but the combined current of the devices must not exceed 40 mA (8mA $I_{MAX}$ for each external device). The status of the ODR bits is set using standard write accesses from either port to address x0001 with a "1" corresponding to "on" and a "0" corresponding to "off". The status of the ODR bits can also be read (without changing the status of the bits) via a standard read to address x0001. When $\overline{SFEN} = V_{IL}$, the ODR is active and address x0001 is not available for standard memory operations. When $\overline{SFEN} = V_{IH}$, the ODR is inactive and address x0001 can be used as part of the main memory. During reads and writes to the ODR $I/O_0$ - $I/O_4$ are valid bits and $I/O_5$ - $I/O_{15}$ will not affect the ODR function but they will read from or write to the memory. Refer to Truth Table VI for Output Drive Register operation.

## Ordering Information

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## Datasheet Document History

10/16/08: Initial Datasheet

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