

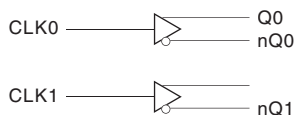
## General Description

The ICS85322I is a Dual LVCMOS / LVTTL-to- Differential 2.5V / 3.3V LVPECL translator. The ICS85322I has selectable single ended clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 2.5V / 3.3V LVPECL levels. The small outline 8-pin SOIC or TSSOP package makes this device ideal for applications where space, high performance and low power are important.

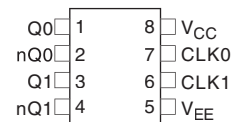
## Features

- Two differential 2.5V/3.3V LVPECL outputs
- Selectable CLK0, CLK1 LVCMOS/LVTTL clock inputs
- CLK0 and CLK1 can accepts the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 267MHz
- Part-to-part skew: 250ps (maximum)
- 3.3V operating supply voltage (operating range 3.135V to 3.465V)
- 2.5V operating supply voltage (operating range 2.375V to 2.625V)
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Block Diagram



## Pin Assignment



**ICS85322I**

**8-Lead SOIC**

**3.90mm x 4.92mm x 1.37mm body package**

**M Package**

**8-Lead TSSOP**

**3.0mm x 3.0mm body package**

**G Package**

**Top View**

## Pin Descriptions and Characteristics

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5	V <sub>EE</sub>	Power		Negative supply pin.
6	CLK1	Input	Pullup	LVCMOS/LVTTL clock input.
7	CLK0	Input	Pullup	LVCMOS/LVTTL clock input.
8	V <sub>CC</sub>	Power		Positive supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	50mA 100mA
Junction Temperature, $T_J$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Positive Supply Current				25	mA

**Table 3B. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	CLK0, CLK1	2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	CLK0, CLK1	-0.3		1.3	V
$I_{IH}$	Input High Current	CLK0, CLK1 $V_{CC} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1 $V_{CC} = V_{IN} = 3.465V$	-150			$\mu A$

**Table 3C. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1	$V_{CC} = V_{IN} = 3.465V$	$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{CC} = V_{IN} = 3.465V$	$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.65		1.0	V

NOTE 1: Outputs terminated with 50 $\Omega$  to  $V_{CC} - 2V$ .

**Table 3D. Power Supply DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				25	mA

**Table 3E. LVCMOS/LVTTL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	CLK0, CLK1		1.6		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	CLK0, CLK1		-0.3		0.9	V
$I_{IH}$	Input High Current	CLK0, CLK1	$V_{CC} = V_{IN} = 2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1	$V_{CC} = V_{IN} = 2.625V$	-150			$\mu A$

**Table 3F. LVPECL DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.65		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Electrical Characteristics

**Table 4A. AC Electrical Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				267	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 267MHz$	0.5		1.9	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				250	ps
$t_R / t_F$	Output Rise/ Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under t

All parameters measured at 133MHz unless noted otherwise.hese conditions.

NOTE 1: Measured from  $V_{CC}/2$  point of the input to the differential output crosspoint.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**Table 4B. AC Electrical Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				215	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 215MHz$	0.7		2.1	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				250	ps
$t_R / t_F$	Output Rise/ Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under t

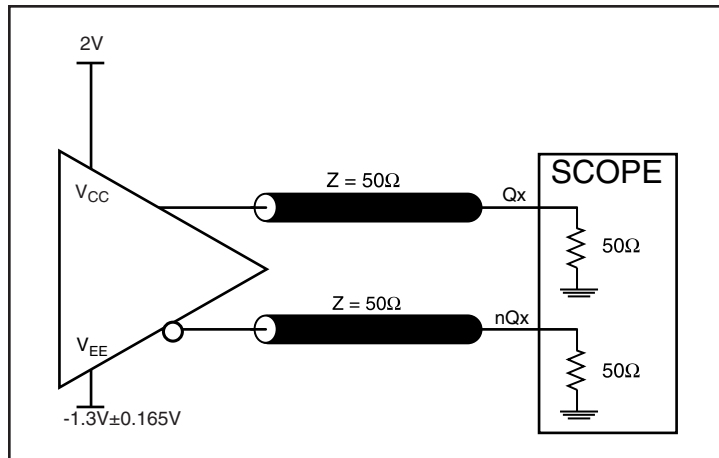
All parameters measured at 133MHz unless noted otherwise.hese conditions.

NOTE 1: Measured from  $V_{CC}/2$  point of the input to the differential output crosspoint.

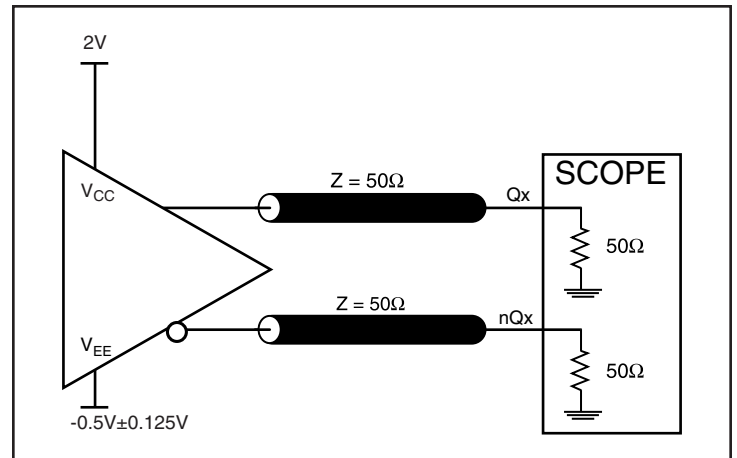
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

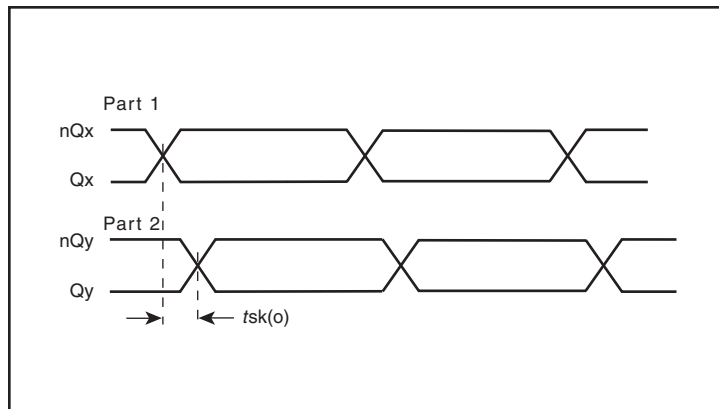
## Parameter Measurement Information



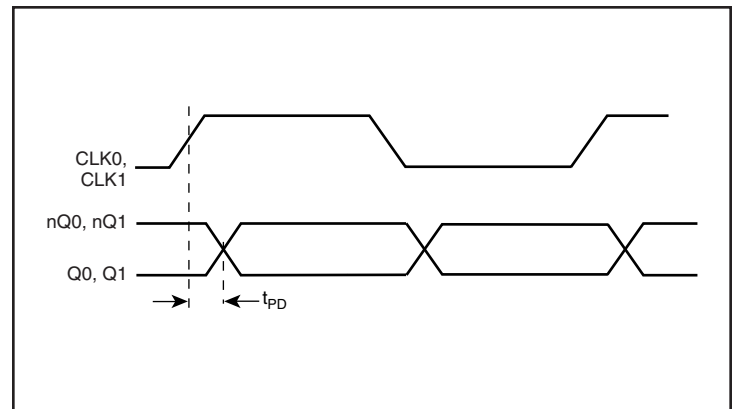
**3.3V LVPECL Output Load AC Test Circuit**



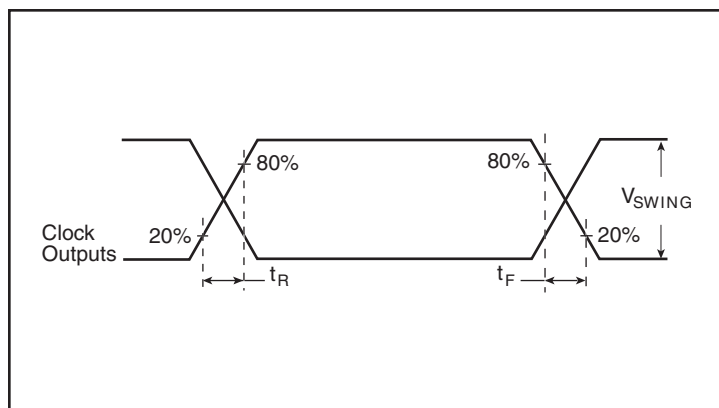
**2.5V LVPECL Output Load AC Test Circuit**



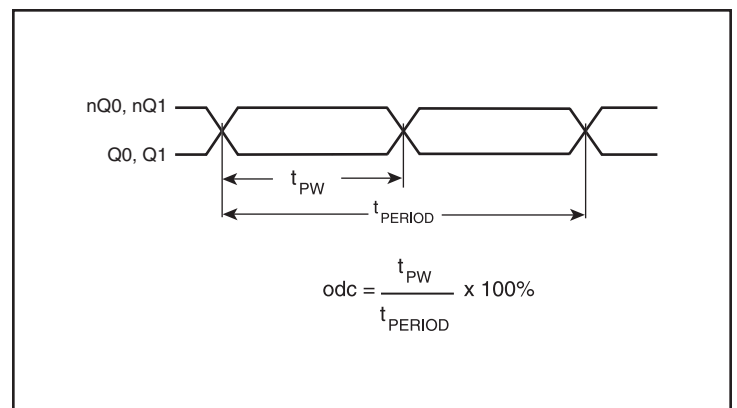
**Part-to-Part Skew**



**PROPAGATION DELAY**



**Output Rise/Fall Time**



**Output Duty Cycle/Pulse Width/Period**

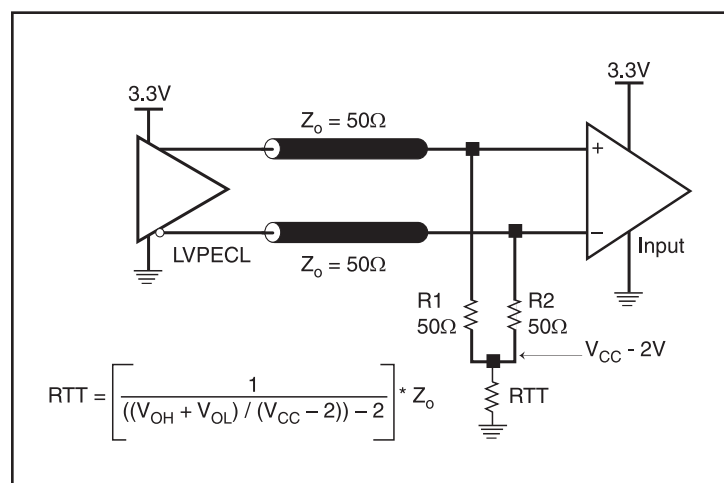
## Applications Information

## Termination for 3.3V LVPECL Outputs

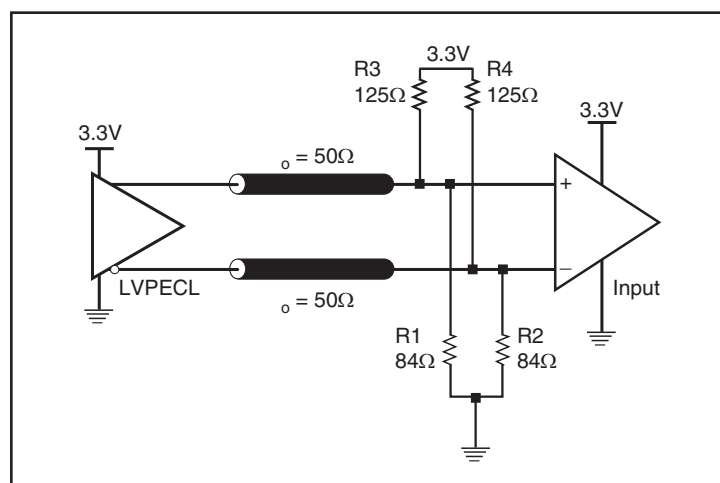
The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



### Figure 1A. 3.3V LVPECL Output Termination



### Figure 1B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 2A and Figure 2B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The R3 in Figure 2B can be eliminated and the termination is shown in Figure 2C.

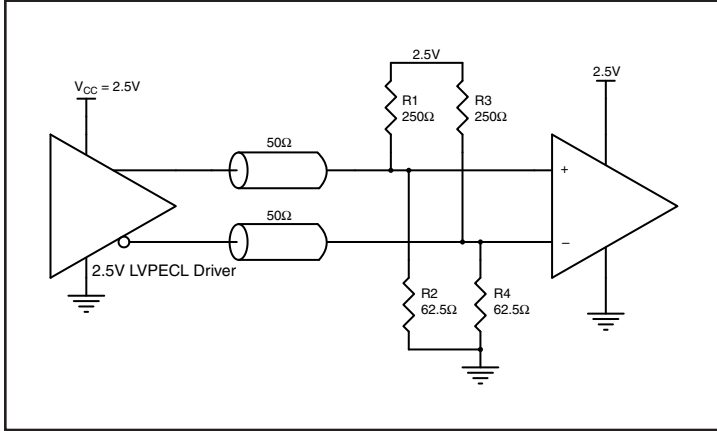


Figure 2A. 2.5V LVPECL Driver Termination Example

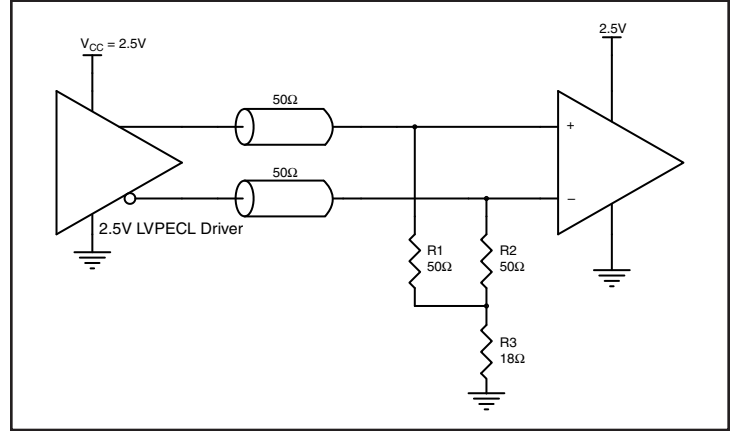


Figure 2B. 2.5V LVPECL Driver Termination Example

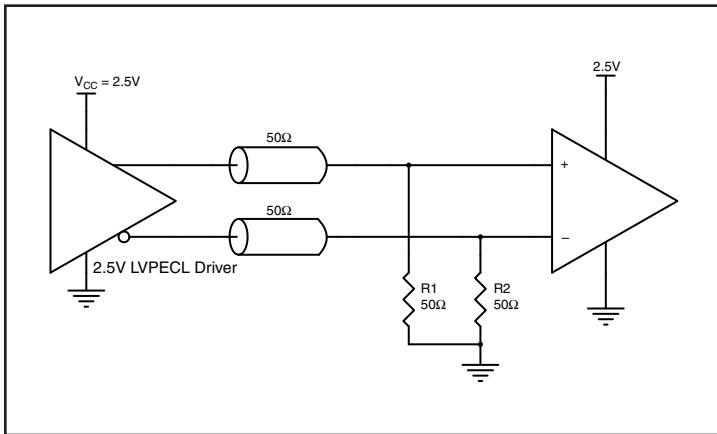


Figure 2C. 2.5V LVPECL Driver Termination Example



## Power Considerations

This section provides information on power dissipation and junction temperature for the IDT85322I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT85322I is the sum of the core power plus the power dissipated at the output(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% \ 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated at the outputs.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 25mA = \mathbf{86.6mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30mW = \mathbf{60mW}$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $86.6mW + 60mW = \mathbf{146.6mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 157°C/W per Table 5 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.147\text{W} * 157^\circ\text{C/W} = 108.1^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 5. Thermal Resistance  $\theta_{JA}$  for 8-Lead TSSOP/SOIC**

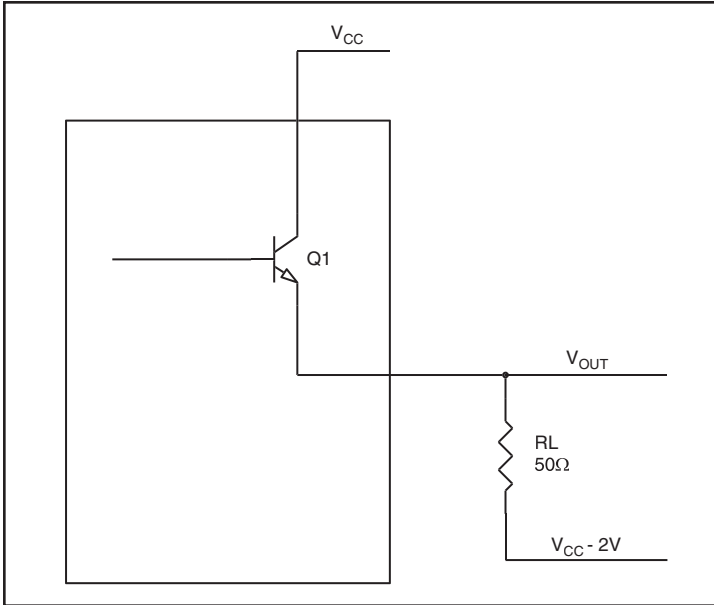
$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2
8-Lead TSSOP	157°C/W	154°C/W	151°C/W
8-Lead SOIC	103°C/W	94°C/W	89°C/W

NOTE: Above  $\theta_{JA}$  values are the simulation result using JEDEC Standard Multi-Layer Test Board.

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation at the output(s).

LVPECL output driver circuit and termination are shown in *Figure 3*.



**Figure 3. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation at the output(s), use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is the power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$\begin{aligned}
 Pd\_H &= [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) \\
 &= [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) \\
 &= [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}
 \end{aligned}$$

$$\begin{aligned}
 Pd\_L &= [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) \\
 &= [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) \\
 &= [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}
 \end{aligned}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{30mW}$$

## Reliability Information

**Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 8-Lead TSSOP/SOIC**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2
8-Lead TSSOP	157°C/W	154°C/W	151°C/W
8-Lead SOIC	103°C/W	94°C/W	89°C/W

NOTE: Above  $\theta_{JA}$  values are the simulation result using JEDEC Standard Multi-Layer Test Board.

## Transistor Count

The transistor count for the ICS85322I is: 269

8-Lead SOIC Package Outline and Dimensions

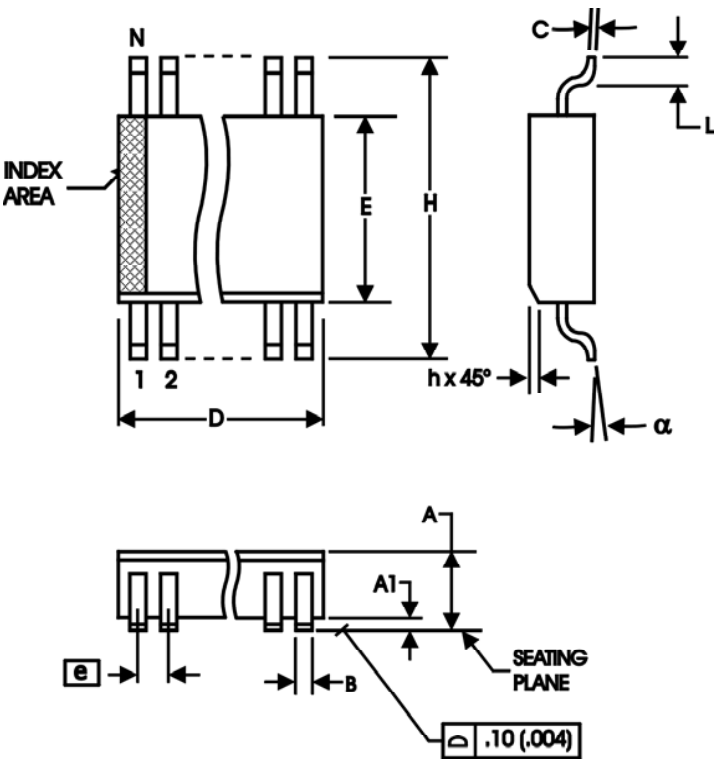


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MO-012

8-Lead TSSOP Package Outline and Dimensions

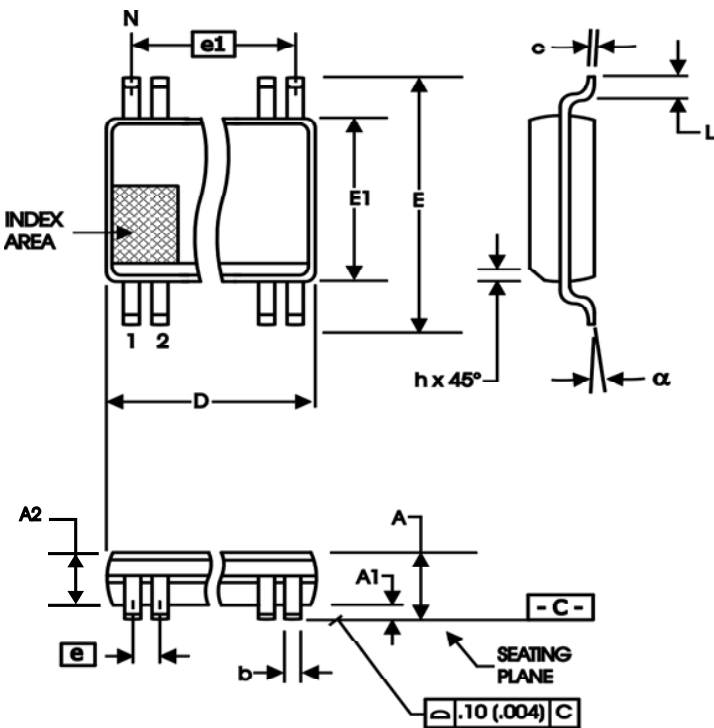


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
A	–	1.10
A1	0	0.15
A2	0.79	1.05
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
L	0.40	0.80
	0°	8°
aaa	–	0.10

Variations

	mm.	
	Minimum	Maximum
N = 8		
b	0.22	0.38
e	0.65 BASIC	
e1	1.95 BASIC	
N = 10		
b	0.17	0.27
e	0.50 BASIC	
e1	2.00 BASIC	

Reference Document: JEDEC Publication 95, MO-187

## Ordering Information

**Table 8. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85322AGILF	2AIL	“Lead-Free” 8-Lead TSSOP	Tube	-40°C to 85°C
85322AGILFT	2AIL	“Lead-Free” 8-Lead TSSOP	Tape & Reel	-40°C to 85°C
85322AMILF	85322AIL	“Lead-Free” 8-Lead SOIC	Tube	-40°C to 85°C
85322AMILFT	85322AIL	“Lead-Free” 8-Lead SOIC	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		8	Added Termination for LVPECL Outputs section.	5/30/02
A		6	3.3V Output Load Test Circuit Diagram, corrected $V_{EE} = -1.3V \pm 0.135V$ to read $V_{EE} = -1.3V \pm 0.165V$ .	8/23/02
		7	Updated Output Rise/Fall Time Diagram.	
B	T2	2	Pin Characteristics Table - changed $C_{IN}$ 4pF max. to 4pF typical.	10/7/03
		3	Absolute Maximum Ratings, updated Inputs ratings.	
		6	Updated 3.3V LVPECL Output Termination Diagrams.	
		7	Added Termination for 2.5V LVPECL Outputs. Updated format throughout data sheet.	
C	T2	1	Features Section - added lead-free bullet.	4/11/07
	T3C	2	Pin Characteristics Table - deleted RPulldown row.	
	T3F	3	LVPECL 3.3V DC Characteristics Table -corrected $V_{OH}$ max. from $V_{CC} - 1.0V$ to $V_{CC} - 0.9V$ ; and $V_{SWING}$ max. from 0.85V to 1.0V.	
		4	LVPECL 2.5V DC Characteristics Table -corrected $V_{OH}$ max. from $V_{CC} - 1.0V$ to $V_{CC} - 0.9V$ ; and $V_{SWING}$ max. from 0.85V to 1.0V.	
	T8	8 - 9	Power Considerations - corrected power dissipation to reflect $V_{OH}$ max in Table 3C & 3F.	
D	T8	12	Updated datasheet's header/footer with IDT from ICS.	7/28/10
		12	Removed ICS prefix from Part/Order Number column.	
		14	Added Contact Page.	
D	T5 T6	1	Added TSSOP package information.	3/10/14
		3	Changed 'Package Thermal Impedance, $\theta_{JA} - 112.7^{\circ}C/W$ (0 lfpm)' to 'Junction Temperature, $T_J - 125^{\circ}C$ '.	
		8	Updated Power Considerations.	
			Replaced Thermal Resistance $\theta_{JA}$ table with 8-Lead TSSOP/SOIC.	
		10	Replaced $\theta_{JA}$ vs. Air Flow table with 8-Lead TSSOP/SOIC.	
		12	Added Package drawing for 8-Lead TSSOP.	

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