

### Introduction

The ISL59448EVAL1Z is a RoHS compliant evaluation board that contains all the circuitry needed to characterize critical performance parameters of the ISL59448 triple 2:1 MUX-amplifier, over a variety of applications.

The ISL59448 contains 3 separate 2 input multiplexers, each followed by a gain of 2 buffer controlled by common set of logic inputs (Figure 1, Table 1). Control features include a high speed (20ns) HIZ output control for individual selection of MUX amps that share a common video output line. A control logic latch ( $\overline{LE}$ ) enables multiple devices to share a common input control logic bus. The  $\overline{ENABLE}$  control can be used to save power by powering the device down.

The evaluation board circuit and layout is optimized for either 50 $\Omega$  or 75 $\Omega$  terminations, and implements a basic R-G-B video 2 input MUX-amp. The board is supplied with 75 $\Omega$  input signal terminations and a 75 $\Omega$  back-termination resistor on each of the 3 outputs, making it suitable for driving video cable with a throughput gain of 0dB. The user has the option of replacing the 75 $\Omega$  resistors with 50 $\Omega$  resistors for other applications. SPDT switches are included to manually control each logic input as well as selecting on-board logic signal termination resistors of 50 $\Omega$  or 5k $\Omega$ .

The layout contains component options that include an output capacitor to ground, a series resistor ( $R_S$ ) followed by a parallel resistor ( $R_L$ ) capacitor ( $C_L$ ) network to ground. This option allows the user to select several different output configurations and to examine frequency domain and time domain response under a variety of different layout parasitic conditions. Examples are shown in Figures 2A, 2B, and 2C. The evaluation board is supplied with the 75 $\Omega$  back termination resistors for video cable driving as shown in Figure 2C.

### Amplifier Performance and Output Configurations

The ISL59448 output amplifiers are designed for high impedance inter-stage use as well as lower impedance video cable driver applications. For example, in an inter-stage application (Figure 2A) where the ISL59448 is driving a high impedance amplifier or buffer, the output amplifiers can be load over a resistance range of 150 $\Omega$  to 1k $\Omega$  or higher. They achieve their best performance with a 500 $\Omega$  load and an output capacitance to ground of 1.1pF or less. For video cable driving applications, the optimum performance is achieved using the 75 $\Omega$  back terminated output configuration shown in Figure 2C. Consult the device data sheet for the performance parameters in the application.

### High Frequency Layout Considerations

At frequencies of 500MHz and higher, circuit board layout may limit performance. The following layout guidelines are implemented on the evaluation board;

- Signal I/O lines are the same lengths and widths to match propagation delay and trace parasitics,
- No series connected vias are used in signal I/O lines, as they can add unwanted inductance,
- Input and output traces use 50 $\Omega$  controlled impedance, and their lengths are minimized to reduce transmission line effects.
- High frequency decoupling caps are placed as close to the device power supply pin as possible - without series vias between the capacitor and the device pin.

These layout methods are difficult to achieve in practice. The evaluation board contains additional unpopulated resistor and capacitor pads for use as a breadboarding tool to examine the effects of PCB layout parasitics on amplifier performance.

### Power Sequencing

Proper power supply sequencing is -V first, then +V. In addition, the +V and -V supply pin voltage rate-of-rise must be limited to  $\pm 1V/\mu s$  or less. The evaluation board contains parallel-connected low Von Schottky diodes on each supply terminal to minimize the risk of latch up due to incorrect sequencing. In addition, extra 10 $\mu F$  decoupling capacitors are added to each supply to aid in reducing the applied voltage rate-of-rise.

### Reference Documents

1. ISL59448 Data Sheet, FN6160

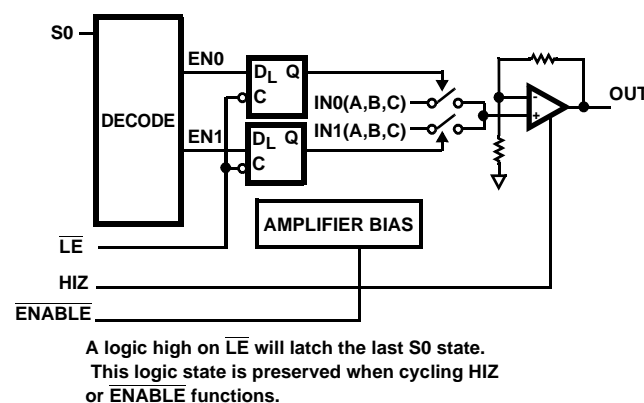
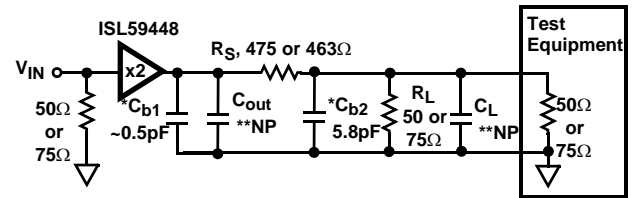


FIGURE 1. ISL59448 FUNCTIONAL BLOCK DIAGRAM  
(1 OF 3 CHANNELS)

# Application Note 1250

TABLE 1. LOGIC TABLE

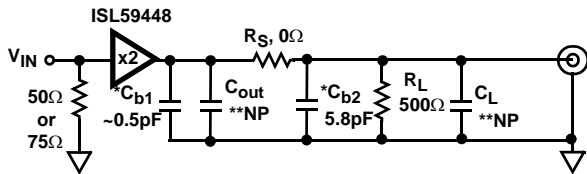
S0	HIZ	ENABLE	LE	OUTA, B, C
0	0	0	0	IN0A, B, C
1	0	0	0	IN1A, B, C
-	1	0	-	Hi Z
-	-	1	-	Power down
-	0	0	1	Last S0 selection



\* Cb1, Cb2 are approximate trace capacitances

\*\* NP = Not populated

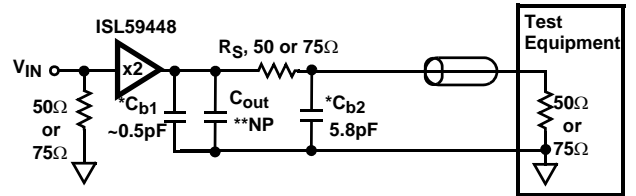
FIGURE 2B. TEST CIRCUIT FOR 50Ω OR 75Ω TERMINATIONS.



\* Cb1, Cb2 are approximate trace capacitances

\*\* NP = Not populated

FIGURE 2A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

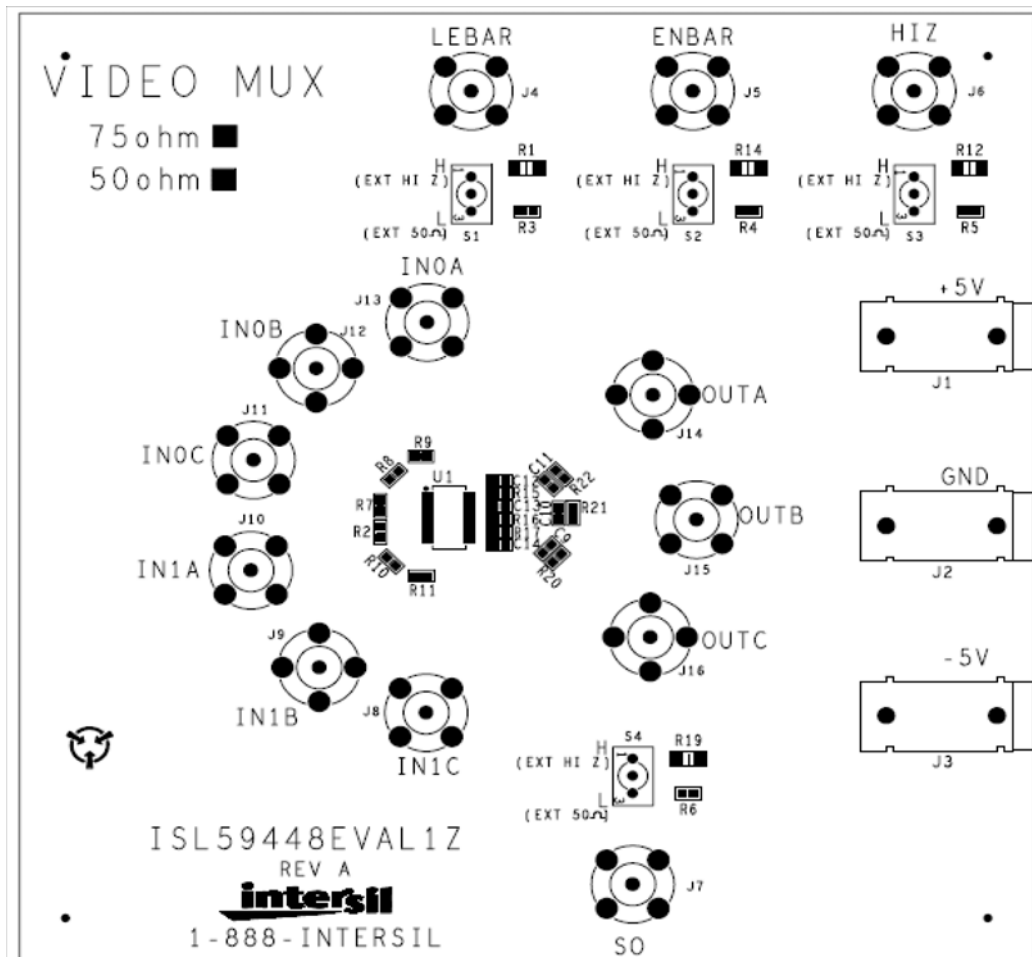


\* Cb1, Cb2 are approximate trace capacitances

\*\* NP = Not populated

FIGURE 2C. BACK-TERMINATED TEST CIRCUIT FOR CABLE APPLICATION

## ISL59448EVAL1Z Top View



# ISL59448EVAL1Z Schematic Diagram and Parts List

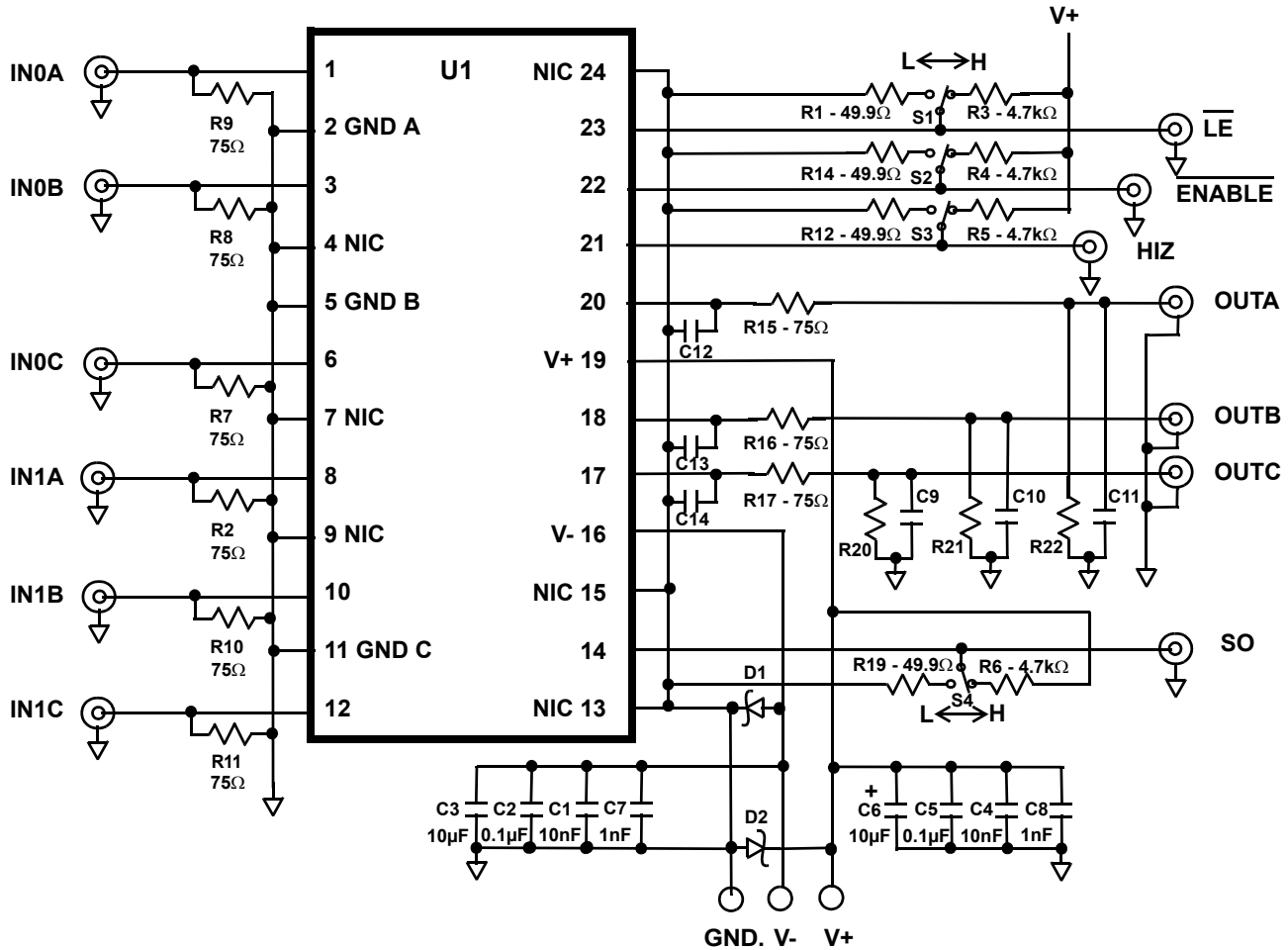


TABLE 2. ISL59448EVAL1Z COMPONENTS PARTS LIST

DEVICE #	DESCRIPTION	COMMENTS
C7, C8	CAP, SMD, 0603, 1000PF, 25V, 10%, X7R	Power Supply De-coupling
C1, C4	CAP, SMD, 0603, 0.01μF, 25V, 10%, X7R	Power Supply De-coupling
C2, C5	CAP, SMD, 0603, 0.1μF, 25V, 10%, X7R	Power Supply De-coupling
C3, C6	CAP, SMD, 0805, 10μF, 6.3V, 10%, X5R	Power Supply De-coupling
D1, D2	DIODE-Shottky, 2PIN, 45V, 7.5A	MBR0550T (Motorola) Reverse Polarity Protection
R2, R7-R11, R15-R17	RESISTOR, SMD,0603, 75Ω, 1/10W, 1%	Signal Input/output Termination
R1, R12, R14, R19	RESISTOR, SMD,0603, 49.9Ω, 1/16W, 1%	Logic Input Termination
R3 - R6	RESISTOR, SMD,0603, 4.7kΩ, 1/16W, 1%	Logic Input Pull-up
R20, R21, R22	RESISTOR, SMD, 0603	Optional, Not Populated
C9, - C14	CAP, SMD, 0603	Optional, Not Populated
S1 - S4	SWITCH, SPDT	Logic Input Control
U1	ISL59448IA -500MHz MULTIPLEXING AMPLIFIER, 24P, QSOP	Device Under Test

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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