Before Getting Started

This document supplements the ISL55110, ISL55111 Specification **FN6228**. Evaluation board users should review that document to obtain information on the parts' basic functionality and power requirements. A most important note is **before powering up the board, review the Power Up Sequence in that specification.** There are two DC sources utilized, so a user may inadvertently mis-apply the power sources causing damage to the part.

Take time to review the ISL55110, ISL55111 Data Sheet (FN6228) and become familiar with the part's basic functions and power options. Note also that FN6228 supersedes this document with respect to updates and modifications. Always refer to that document if discrepancies occur.

All ISL55110, ISL55111 QFN and TSSOP boards are designed essentially in the same fashion. This document provides the user with the information regarding the evaluation board design, circuitry layout and driver load options.

Scope Probe Connections

Another topic to cover before getting started is the evaluation board physical connections for waveform observations. On each schematic version you will see a component with pins designated as DIF+ and DIF-. This is not an active component but a dual pin header physically designed to accommodate leadless connection of active differential or FET Probes. This will minimize ground lead inductance and capacitive loading while making waveform observations. However, the user must also be mindful of max voltage limitations when using these types of probes. The ISL55110, ISL55111 drivers cover a large voltage range, so double check the probe's specifications.

Scope Probe Test Points (TP) are provisioned across all inputs, outputs and VDD/VH to ground.

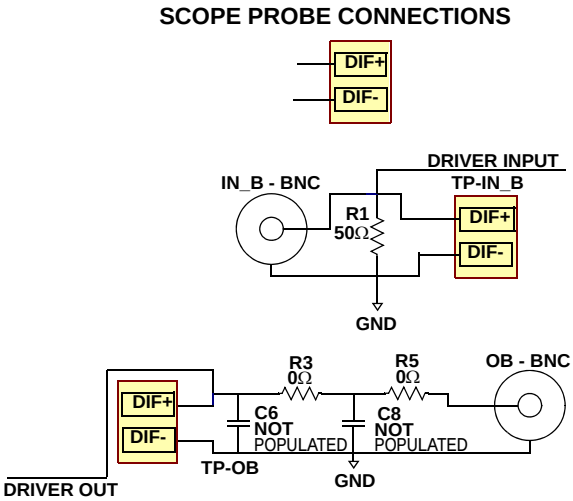

FIGURE 1. DUAL.1" SPACED PINS ARE PLACED ON THE EVALUATIONS BOARDS FOR LEADLESS ACTIVE PROBE CONNECTIONS

BNC Connections

This series of evaluation boards also provides BNC connections for Input and Output signals. A key point to remember is the ISL55110, ISL55111 Driver Outputs (OA/OB) operate with the VH voltage as a High and Ground as a Low. These connectors are laid out to accommodate SMD connectors as well as BNC's. Also note that the Driver Inputs have 50Ω terminations that you may need to remove for your application.

Power Down Feature

All boards provide the same capability for testing the Power Down Feature. A SPDT- Center OFF switch is provided for manual testing of the feature. In one position the PD input is connected to VDD (Power Down Enabled). In the other position the PD Input is connected to Ground.

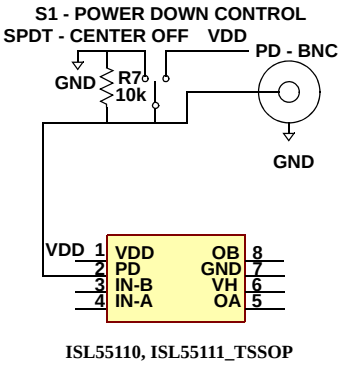

FIGURE 2. TSSOP AND QFN EVALUATION BOARDS HAVE THE SAME POWER DOWN CIRCUITRY

Finally the center off position provides a means of connecting a repetitive signal source to the PD input. This is so that the user can observe Power Down Enable/Disable timing. An important note to remember when using the PD - BNC: 1) Place the switch in Center-Off position. 2) The PD input is referenced to VDD and ground.

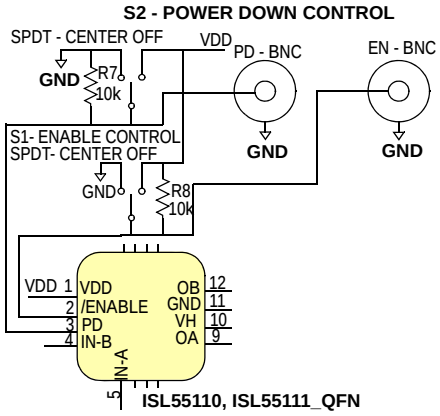

FIGURE 3. QFN PACKAGES HAVE BOTH POWER DOWN AND OUTPUT ENABLE DIGITAL INPUTS

Initial Power Up

Please refer to the device specification for power up sequencing and current requirements. Also note that the frequency of operation of each driver will determine the current needed. There are graphs in the specification regarding current characteristics.

When first powering up the device, set all power bus inputs to minimum current levels needed for quiescent operation. Check the device out statically with DC inputs on the IN_A/IN_B pins and observe that the OA/OB outputs toggle when the Input pins rise above and below the logic thresholds. Please note that these inputs are intended for use by high speed logic. Avoid slow DC ramps.

VDD current should be ~3.6mA and VH should be less then 100µAmps with no DC loads on the outputs.

Once static observations check out, you can then increase power current limits for VCC/VH and apply higher frequency inputs to the IN_A/IN_B pins.

Layout Information

All evaluation boards have complete silk-screen information regarding Test points, Jumpers and Component placements.

Schematic Information

Schematics are drawn with physical location in mind. Any changes in electrical circuitry will be updated in this document as needed.

Included below are two schematics. ISL55110, ISL55111: TSSOP dual driver device and ISL55110, ISL55111 QFN dual driver. Both packages have the Power Down Control, while the QFN has both Power Down and $\overline{\text{Enable}}$ inputs.

Driver Loads

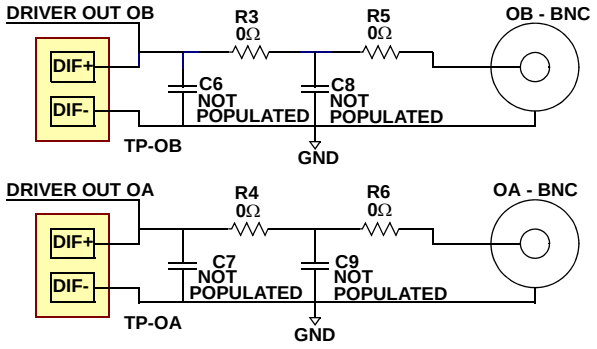

FIGURE 4. CUSTOM LOAD COMPONENTS

Component locations C6 to C7 and R3 to R6 are surface mount locations provided so the user can experiment with various load configurations.

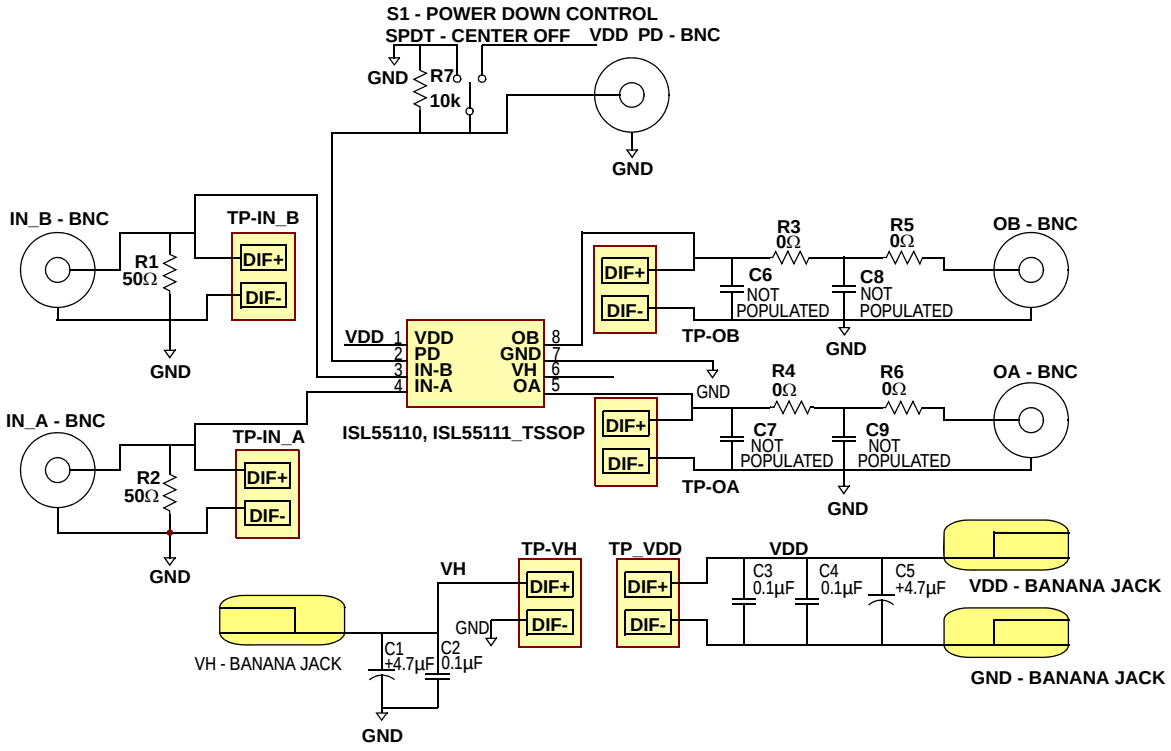

FIGURE 5. TSSOP EVALUATION BOARD SCHEMATIC

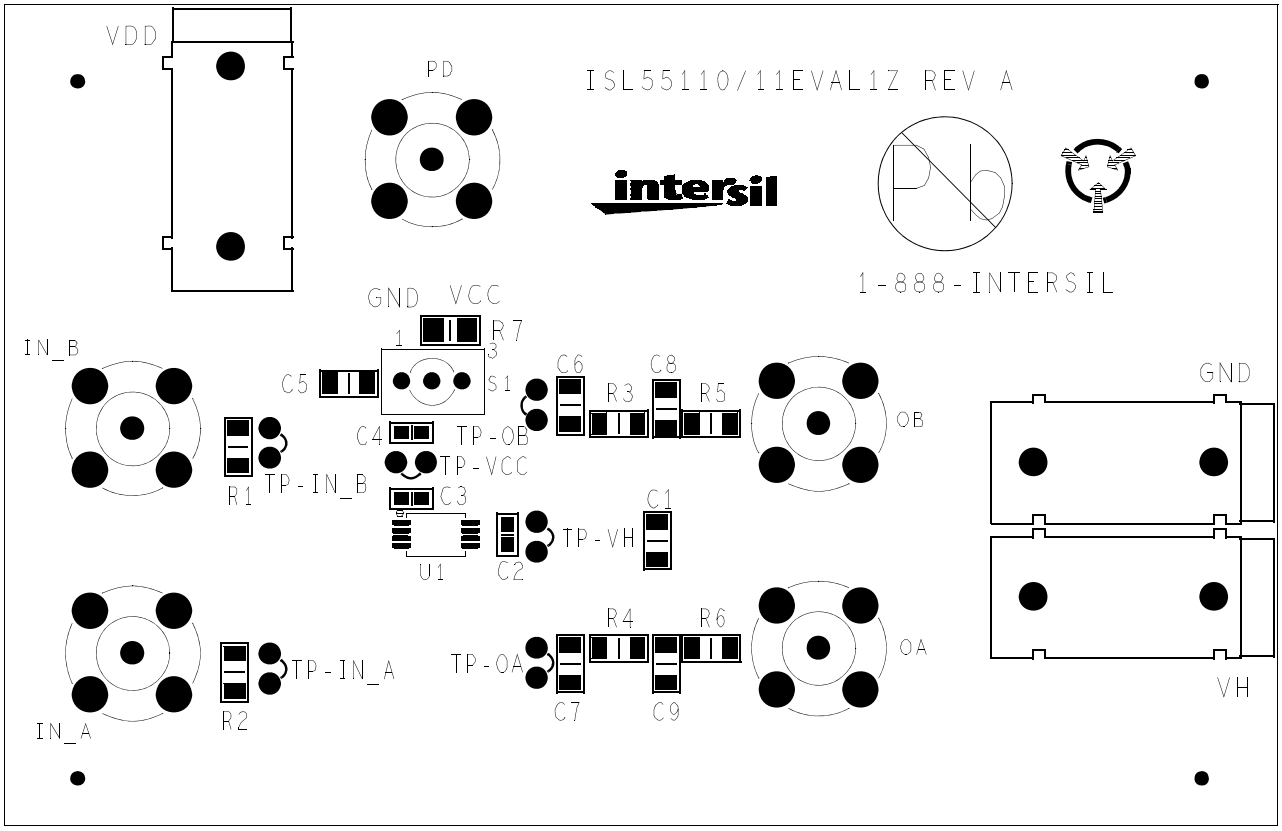

FIGURE 6. TSSOP LAYOUT

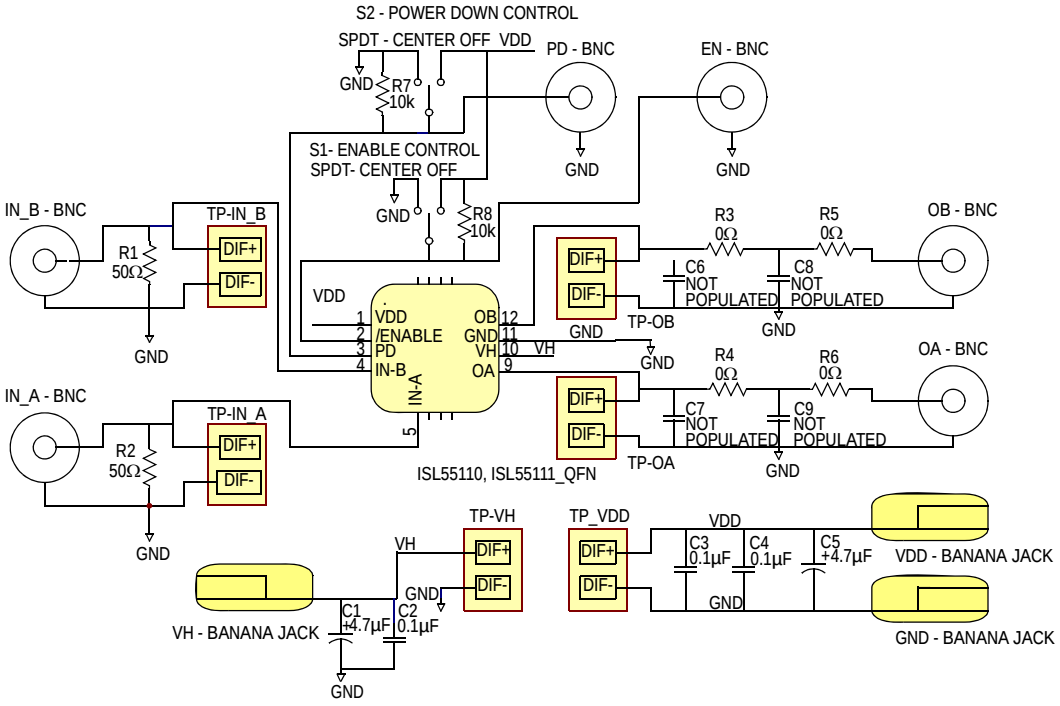

FIGURE 7. QFN EVALUATION BOARD SCHEMATIC

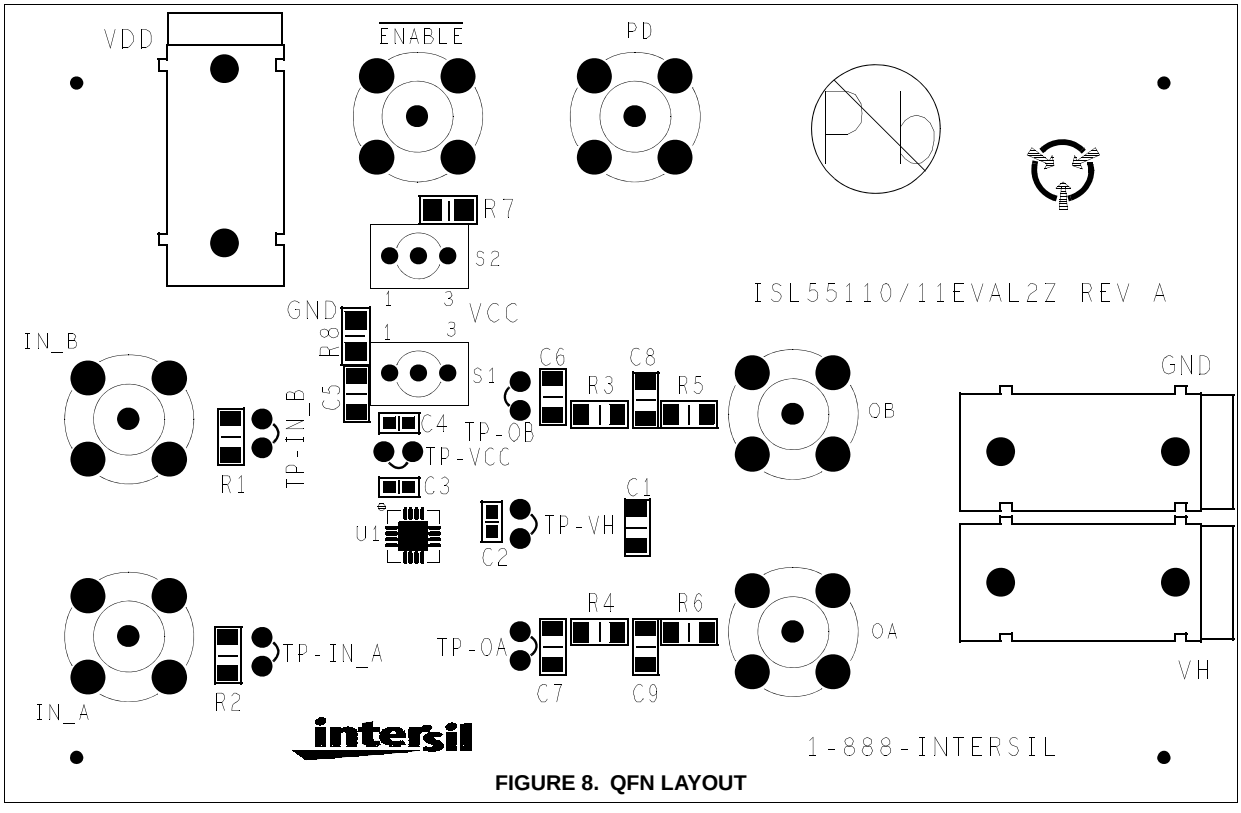

FIGURE 8. QFN LAYOUT