## Introduction

The ISL8105B is a simple single-phase PWM controller for a synchronous buck converter that operates from +5 V or +12 V bias supply voltage. With integrated linear regulator, boot diode, and gate drivers, the ISL8105B reduces external component count and board space requirements.
The ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board highlights the operations of the controller in a DC/DC application.

## ISL8105BEVAL1Z, ISL8105BEVAL2Z Reference Design

The ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board is designed to optimize for the output voltage and current specifications shown in Table 1.

TABLE 1. ISL8105BEVAL1Z, ISL8105BEVAL2Z EVALUATION BOARD DESIGN PARAMETERS

| PARAMETER | MIN | TYP | MAX |
| :--- | :---: | :---: | :---: |
| Input Voltage (VIN) | 9.6 V | 12 V | 14.4 V |
| Output Voltage ( $\left.\mathrm{V}_{\text {OUT }}\right)$ |  | 1.8 V |  |
| Output Voltage Ripple ( $\left.\mathrm{V}_{\text {RIPPLE }}\right)$ |  | $30 \mathrm{mV} \mathrm{V}_{\mathrm{P}-\mathrm{P}}$ |  |
| Continuous Load Current |  |  | 15 A |
| Efficiency |  | 90 |  |

Two versions of the evaluation board, based on the package type, are listed in Table 2.

TABLE 2. EVALUATION BOARDS

| BOARD NAME | IC | PACKAGE |
| :--- | :---: | :---: |
| ISL8105BEVAL1Z | ISL8105BIBZ | 8 Ld SOIC |
| ISL8105BEVAL2Z | ISL8105BIRZ | 10 Ld DFN |

## Design Procedure

The following sections illustrate simple design steps and component selections for a converter using the ISL8105BEVAL1Z, ISL8105BEVAL2Z.

## Output Inductor Selection

The output inductor is chosen by the desired inductor ripple current, which is typically set to be approximately $40 \%$ of the rated output current. The desired output inductor can be calculated using Equation 1:
$\mathrm{L}=\frac{\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}}{\Delta \mathrm{I}} \times \frac{\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {IN }}} \times \frac{1}{\mathrm{~F}_{\text {SW }}}$

$$
\begin{gathered}
=\frac{14.4-1.8}{0.4 \cdot 15} \times \frac{1.8}{14.4} \times \frac{1}{300 \times 10^{3}} \\
=0.875 \mu \mathrm{H}
\end{gathered}
$$

In the evaluation board, a $1 \mu \mathrm{H}$ inductor with $1.87 \mathrm{~m} \Omega$ DCR (Cooper Bussmmann's HC9-1R0-R) is employed. This yields approximately 0.44 W conduction loss in the inductor.

## Output Capacitor Selection

The output capacitors are generally selected by the output voltage ripple and load transient response requirements. ESR and capacitor charge are major contributions to the output voltage ripple. Assuming that the total output capacitance is sufficient, then the output voltage ripple is dominated by the ESR, which can be calculated using Equation 2.
$\mathrm{V}_{\text {RIPPLE }}=\Delta \mathrm{I}_{\mathrm{L}} \cdot \mathrm{ESR}$
To meet the $30 \mathrm{mV} \mathrm{P}_{\mathrm{P}-\mathrm{P}}$ output voltage ripple requirement, the effective ESR should be less than $5 \mathrm{~m} \Omega$.

The output voltage response to a transient load is contributed from ESL, ESR and the amount of output capacitance. With $\mathrm{V}_{\text {IN }} \gg \mathrm{V}_{\text {OUT }}$, the amplitude of the voltage excursions can be approximated using Equation 3:

$$
\begin{equation*}
\Delta \mathrm{V}=\frac{\mathrm{L} \cdot \mathrm{I}_{\text {tran }}^{2}}{\mathrm{C}_{\mathrm{OUT}} \cdot \mathrm{~V}_{\mathrm{OUT}}} \tag{EQ.3}
\end{equation*}
$$

With $1 \mu \mathrm{H}$ inductor and 0 A to 15 A step load, the total output capacitance of $1560 \mu \mathrm{~F}$ is required for 80 mV output voltage transient. In the ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board, four of Sanyo's 2R5TPF470ML are employed.

## Input Capacitor Selection

The input bulk capacitors selection criteria are based on the capacitance and RMS current capability. The RMS current rating requirement for the input capacitor is approximated in Equation 4:
$I_{I N, R M S}=\sqrt{I_{O}^{2}\left(D-D^{2}\right)+\frac{\Delta I^{2}}{12} D} \quad D=\frac{V_{O}}{V I N}$
In this application, the RMS current for the input capacitors is 5.4A; therefore, three of Sanyo's 35ME330AX are used.

Small ceramic capacitors for high frequency decoupling are also required to control the voltage overshoot across the MOSFETs.

## MOSFET Selection

The ISL8105B requires two N-Channel power MOSFETs as the main and the synchronous switches. These should be selected based in $r_{\text {DS(ON }}$, gate supply requirements and thermal management requirements.

The total power loss in MOSFET consists of conduction loss and switching loss, as shown in Equation 5:
$\mathrm{P}_{\text {MOSFET(TOT) }}=\mathrm{P}_{\text {cond }}+\mathrm{P}_{\text {SW }}$
In this relatively small duty cycle design, the low-side MOSFET conducts current most of the time. To optimize the converter efficiency, select the high-side MOSFET with low gate charge for fast switching transition and low-side MOSFET with low $r_{\text {DS(ON) }}$.

To achieve the target efficiency, the budget power losses in high-side and low-side MOSFETs are 0.5 W and 1 W , respectively.

## LOW-SIDE MOSFET SELECTION

The low-side MOSFET's RMS current is approximated in Equation 6:
$\mathrm{I}_{\mathrm{L}(\mathrm{RMS})}=\mathrm{I}_{\mathrm{OUT}} \cdot \sqrt{1-\mathrm{D}} \cdot \sqrt{1+\frac{1}{12} \cdot\left(\frac{\Delta \mathrm{I}_{\mathrm{L}}}{\mathrm{I}_{\mathrm{OUT}}}\right)^{2}} \approx 13.9 \mathrm{~A}$
Therefore, the ON-resistance of the low-side MOSFET must be less than $5 \mathrm{~m} \Omega$. Infineon's BSC030N03LS is employed in the ISL8105BEVAL1Z, ISL8105BEVAL2Z evaluation board. The conduction loss in the low-side MOSFET is calculated using Equation 7:
$P_{\text {LFET(cond) })}=\left.1_{\mathrm{L}(\mathrm{RMS})}^{2} \cdot r_{\mathrm{DS}(\mathrm{ON})}\right|_{\mathrm{LFET}}=0.58 \mathrm{~W}$
The switching loss in the low-side MOSFET is dominated by the loss in body diode which can be calculated using Equation 8:
$P_{\text {diode }}=I_{O} \cdot \mathrm{t}_{\mathrm{D}} \cdot \mathrm{V}_{\mathrm{F}} \cdot \mathrm{F}_{\mathrm{SW}}=0.3 \mathrm{~W}$
Where $t_{D}$ is the total dead time in each switching period $(\sim 60 \mu \mathrm{~s})$ and $\mathrm{V}_{\mathrm{F}}$ is the forward voltage drop of MOSFET's body diode.

The total power dissipation in the low-side MOSFET is calculated using Equation 9:
$\mathrm{P}_{\text {LFET }(\mathrm{TOT})}=0.88 \mathrm{~W}$

## HIGH-SIDE MOSFET SELECTION

For the high-side MOSFET selection, first we assume that the conduction loss and the switching loss contribute evenly to the total power dissipation.
The high-side MOSFET's RMS current is approximated using Equation 10 :
$\mathrm{I}_{\mathrm{H}(\mathrm{rms})}=\mathrm{I}_{\mathrm{OUT}} \cdot \sqrt{\mathrm{D}} \cdot \sqrt{1+\frac{1}{12} \cdot\left(\frac{\Delta \mathrm{I}_{\mathrm{L}}}{\mathrm{I}_{\mathrm{OUT}}}\right)^{2}} \approx 5.85 \mathrm{~A}$

Hence, the required ON-resistance of the high-side MOSFET is $7.3 \mathrm{~m} \Omega$. Infineon's BSC080N03LS is selected. The conduction loss in the high-side MOSFET is calculated using Equation 11:

$$
\begin{equation*}
\mathrm{P}_{\mathrm{HFET}(\text { cond })}=\left.\mathrm{I}_{\mathrm{H}(\mathrm{RMS})}^{2} \cdot \mathrm{r}_{\mathrm{DS}(\mathrm{ON})}\right|_{\mathrm{HFET}}=0.27 \mathrm{~W} \tag{EQ.11}
\end{equation*}
$$

The switching loss in the high-side MOSFET can be approximated using Equation 12:

$$
\begin{gather*}
\mathrm{P}_{\mathrm{HFET}(\mathrm{SW})}=\frac{1}{2} \cdot \mathrm{I}_{\mathrm{O}} \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{t}_{\mathrm{tr}} \cdot \mathrm{~F}_{\mathrm{SW}}+\frac{1}{2} \cdot \mathrm{C}_{\mathrm{OSS}} \cdot \mathrm{~V}_{\mathrm{IN}}^{2} \cdot \mathrm{~F}_{\mathrm{SW}} \\
=0.17 \mathrm{~W} \tag{EQ.12}
\end{gather*}
$$

where $t_{t r}$ is the combined ON and OFF MOSFET transition times.

The total power dissipation in high-side MOSFET is shown in Equation 13:

$$
\begin{equation*}
\mathrm{P}_{\mathrm{HFET}(\mathrm{TOT})}=0.44 \mathrm{~W} \tag{EQ.13}
\end{equation*}
$$

## Overcurrent Protection Setting

The overcurrent function protects the converter from a shorted output by using the low-side MOSFET's $\mathrm{r}_{\mathrm{DS}(\mathrm{ON})}$ to monitor the current. A resistor, $\mathrm{R}_{\mathrm{BSOC}}$, programs the overcurrent trip level. If overcurrent is detected, the output immediately shuts off, it cycles the soft-start function in a hiccup mode (2 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely.
The overcurrent function will trip at a inductor current $\left(l_{\text {trip }}\right)$ is determined using Equation 14 :
$\mathrm{I}_{\text {trip }}=\frac{2 \bullet \mathrm{I}_{\mathrm{OCSET}} \bullet \mathrm{R}_{\mathrm{BSOC}}}{\mathrm{r}_{\mathrm{DS}(\mathrm{ON})}}$
where $\mathrm{I}_{\text {OCSET }}$ is the internal $21.5 \mu \mathrm{~A}$ (typ.) OCSET current source.

The OC trip point varies mainly due to the MOSFET's r ${ }^{\mathrm{DS}}(\mathrm{ON})$ variations. To avoid overcurrent tripping in the normal operating load range, calculate the $\mathrm{R}_{\text {BSOC }}$ resistor from Equation 14 using:

1. The maximum $r_{\mathrm{DS}(\mathrm{ON})}$ at the highest junction temperature.
2. The minimum lOCSET from the specification table of the datasheet.
Determine $I_{\text {trip }}$ for $I_{\text {trip }}>I_{\text {OUT(MAX }}+(\Delta I) / 2$, where $\Delta I$ is the output inductor ripple current.

With Infineon's BSC030N03LS as the low-side MOSFET and $\mathrm{R}_{\mathrm{BSOC}}$ of $1.74 \mathrm{k} \Omega$. The overcurrent trip point on the evaluation board has been set to 21 A for $12 \mathrm{~V}_{\text {BIAS }}\left(17 \mathrm{~A}\right.$ for $\left.5 \mathrm{~V}_{\mathrm{BIAS}}\right)$.


FIGURE 1. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

## Feedback Compensator

Type-III network is recommended for compensating the feedback loop. Figure 1 shows Type-III compensation configuration for ISL8105B.

With the inductor and output capacitor selected as described in the previous sections, the poles and zero of the power stage can be summarized in Equation 15:

$$
\begin{align*}
\mathrm{F}_{0} & =\frac{1}{2 \times \pi \times \sqrt{\mathrm{L} \mathrm{\times C}}}=3.7 \mathrm{kHz} \\
\mathrm{~F}_{\mathrm{ESR}} & =\frac{1}{2 \times \pi \times \mathrm{C} \times \mathrm{ESR}}=33.9 \mathrm{kHz} \tag{EQ.15}
\end{align*}
$$

1. With a value of $11.8 \mathrm{k} \Omega$ for $\mathrm{R}_{1}$, select $\mathrm{R}_{4}$ for the target output voltage of 1.8 V using Equation 16 :
$R_{4}=R_{1} \times \frac{V_{\text {ref }}}{V_{\text {OUT }}-V_{\text {ref }}}$
2. With the desired feedback loop bandwidth of $30 \mathrm{kHz}, \mathrm{R}_{2}$ can be calculated using Equation 17:
$R_{2}=\frac{V_{O S C} \cdot R_{1} \cdot F_{0}}{d_{\max } \cdot V_{I N} \cdot F_{L C}}$
$=12 \mathrm{k} \Omega$
3. Select $\mathrm{C}_{1}$ such that $\mathrm{F}_{\mathrm{Z1}}$ is located at $1.5 \mathrm{kHz}(\sim 50 \%$ of $\mathrm{F}_{\mathrm{LC}}$ ):

$$
\begin{gather*}
C_{1}=\frac{1}{2 \pi \cdot R_{2} \cdot 1.5 \times 10^{3}}  \tag{EQ.18}\\
\approx 10 \mathrm{nF}
\end{gather*}
$$

4. Select $\mathrm{C}_{2}$ such that $\mathrm{F}_{\mathrm{P} 1}$ is located at $\mathrm{F}_{\mathrm{ESR}}$ :

$$
\begin{gather*}
C_{2}=\frac{C_{1}}{2 \pi \cdot R_{2} \cdot C_{1} \cdot F_{E S R}-1}  \tag{EQ.19}\\
\approx 390 \mathrm{pF}
\end{gather*}
$$

5. Select $R_{3}$ such that $F_{Z 2}$ is located at $F_{L C}$ :

$$
\begin{gather*}
\mathrm{R}_{3}=\frac{\mathrm{R}_{1}}{\frac{150 \times 10^{3}}{\mathrm{~F}_{\mathrm{LC}}}-1} \approx 301 \Omega  \tag{EQ.20}\\
\mathrm{C}_{3}=\frac{1}{2 \pi \cdot \mathrm{R}_{3} \cdot 150 \times 10^{3}} \approx 3.3 \mathrm{nF}
\end{gather*}
$$

A more detailed explanation of designing compensation networks for buck converters with voltage mode control can be found in TB417 entitled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators".

## Evaluation Board Performance

Figure 2 shows a photograph of the ISL8105BEVAL1Z.


FIGURE 2. ISL8105BEVAL1Z

## Power and Load Connections

Terminals J 1 and J 2 are connected to the input of the power stage. The IC bias supply and the converter input supply can be together through pin 2 and 3 of the Jumper $J 7$ to provide single rail supply application. When using separate supplies, provide the IC bias voltage to terminal J 2 with pin 2 and pin 1 of $J 7$ connected together. The load can be connected to terminal J4 and J5. TP6 and TP3 can be used for DMM to measure output voltage. The scope probe terminal (TPV01) can be used to monitor $\mathrm{V}_{\text {OUT }}$ with an oscilloscope. The push switch, SW1, can be used to disable the controller.

## Start-up

The ISL8105B starts up when $V_{\text {BIAS }}$ rises above POR threshold and the COMP/EN rises above $V_{\text {DISABLE }}$ level. The entire start-up time sequence from POR typically takes up to 23.8 ms ; up to 10.2 ms for the delay and the Overcurrent Protection (OCP) sample and hold operation. The initial delay is added to allow the bias voltage to rise/exceed 6.5 V , so that the internal bias regulator can turn on cleanly. When the OCP sampling and hold operations are done, the soft-start function internally ramps the reference on the non-inverting terminal of the error amp from 0 V to 0.6 V in 13.6 ms (typ).

Figure 3 shows the start-up profile of the ISL8105BEVAL1Z, ISL8105BEVAL2Z in relation to the start-up of the 12 V input supply and the bias supply.


FIGURE 3. SOFT-START

## Soft-Start with Pre-Biased Output

If the output is pre-biased to a voltage less than the expected value, the ISL8105BEVAL1Z, ISL8105BEVAL2Z will detect that condition. Neither MOSFETs will turn on until the soft-start ramp voltage exceeds the FB voltage; V $\mathrm{V}_{\text {OUT }}$ starts seamlessly ramping from there.


FIGURE 4. SOFT-START WITH PRE-BIASED OUTPUT

## Output Ripple

Figure 5 shows the ripple voltage on the output of the regulator.


FIGURE 5. OUTPUT RIPPLE ( 20 MHz BW)

## Verifying Loop Gain

Figure 6 shows the measurement of loop gain of the converter with feedback network design in the previous sections.



S1

FIGURE 6. LOOP GAIN MEASUREMENT AT $+25^{\circ} \mathrm{C}$

## Transient Performance

Figures 7, 8, and 9 show the response of the output when subjected to transient loading from 0 A to 15 A at $1 \mathrm{~A} / \mu \mathrm{s}$.


FIGURE 7. TRANSIENT RESPONSE


FIGURE 8. TRANSIENT RESPONSE


FIGURE 9. TRANSIENT RESPONSE

## Efficiency

ISL8105BEVAL1Z, ISL8105BEVAL2Z based regulators enable the design of highly efficient systems. The efficiency of the evaluation board using a 12 V input supply is shown in Figure 10.


FIGURE 10. EVALUATION BOARD EFFICIENCY ( $\mathrm{V}_{\mathrm{OUT}}=1.8 \mathrm{~V}$ )


FIGURE 11. EVALUATION BOARD LINE REGUALTION

## References

For Intersil documents available on the web, go to http://www.intersil.com/.

1. ISL8105, ISL8105B Data Sheet, FN6306, "+5V or +12 V Single-Phase Synchronous Buck Converter PWM Controller with Integrated MOSFET Gate Drivers", Intersil Corporation
2. Tech Brief TB417, "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators", Intersil Corporation

ISL8105BEVAL1Z Schematic


ISL8105BEVAL1Z Bill of Materials

| ID | REFERENCE | QTY | PART NUMBER | PART TYPE | DESCRIPTION | PACKAGE | VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | U1 | 1 | ISL8105BIBZ | IC, Linear | IC, Single PWM Controller | 8 LD SOIC | Intersil |
| 2 | Q1 | 1 | BSC080N30LS G | MOSFET | 30V N-Channel MOSFET | TDSON-08 | Infineon |
| 3 | Q3 | 1 | BSC030N03LS G | MOSFET | 30 V - Channel MOSFET | TDSON-08 | Infineon |
| 4 | Q2, Q4, Q5, Q6 | DNP |  | MOSFET |  |  |  |
| 5 | L1 | 1 | HC9-1R0-R | Inductor | $1.0 \mu \mathrm{H}$, high current inductor | SMD | Cooper Bussmann |
| 6 | SW1 | 1 | EVQ-PAD04M | Push Switch | SWITCH-PUSH, TH, 6 mm , 1P, PUSHB MOM-SPST |  | PANASONIC |
| CAPACITORS |  |  |  |  |  |  |  |
| 7 | C1 | 1 |  | Capacitor, Ceramic, X7R | 10nF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 8 | C2 | 1 |  | Capacitor, Ceramic, X7R | 390pF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 9 | C3 | 1 |  | Capacitor, Ceramic, X7R | 3.3nF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 10 | C4, C9, C10 | 3 |  | Capacitor, Ceramic, X7R | $1 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%, \mathrm{X} 7 \mathrm{R}, \mathrm{ROHS}$ | SM_0805 | TDK/Generic |
| 11 | C5, C27, C28 | 3 |  | Capacitor, Ceramic, X7R | 0.1 $\mu \mathrm{F}, 16 \mathrm{~V}, 10 \%, \mathrm{ROHS}$ | SM_0603 | TDK/Generic |
| 12 | C8 | 1 |  | Capacitor, Ceramic, X7R | 680pF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 13 | C11, C12, C13 | 3 | 35ME330AX | Aluminum Capacitor | $330 \mu \mathrm{~F}, 35 \mathrm{~V}$ | RAD 10x20 | Sanyo |
| 14 | C18, C19, C20, C21 | 4 | 2R5TPF470ML | Organic Alumium Capacitor | $470 \mu \mathrm{~F}, 2.5 \mathrm{~V}, 20 \%$, ROHS | Case D3L | Sanyo |
| 15 | $\begin{aligned} & \text { C6, C7, C14, C15, C16, C17, } \\ & \text { C22, C23, C24, C25, C26 } \end{aligned}$ | DNP |  |  |  |  |  |
| RESISTORS |  |  |  |  |  |  |  |
| 16 | R1 | 1 |  | Resistor, Film | 11.8k $\Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 17 | R2 | 1 |  | Resistor, Film | 12k $\Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 18 | R3 | 1 |  | Resistor, Film | 301ת, 1\%, 1/16W | SM_0603 | Panasonic/Generic |
| 19 | R4 | 1 |  | Resistor, Film | 5.9k $\Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 20 | R5 | 1 |  | Resistor, Film | $1.74 \mathrm{k} \Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 21 | R6 | 1 |  | Resistor, Film | 4.7 $\Omega$, 1\%, 1/16W | SM_0603 | Panasonic/Generic |
| 22 | R7, R8 | DNP |  |  |  | SM_0603 |  |
| OTHERS |  |  |  |  |  |  |  |
| 23 | TPVO1 | DNP |  | Terminal, Scope Probe | CONN-PIN RECEPTACLE, 0.086 DIA, 0.200 L , ROHS |  | MILL-MAX |
| 24 | J1, J4 | 2 | 111-0702-001 | Blinding Post | CONN-GEN, BIND. POST, RED, THMBNUT-GND |  | JOHNSON COMPONENTS |
| 25 | J3, J5 | 2 | 111-0703-001 | Blinding Post | CONN-GEN, BIND. POST, BLACK, THMBNUT-GND |  | JOHNSON COMPONENTS |
| 26 | J2, J6 | 2 | 1514-2 | Turrett Post | CONN-TURRET, TERMINAL POST, TH, ROHS |  | Keystone |
| 27 | J7 | 1 | 68000-236-1X3 |  | 3-pin Jumper |  | Berg/FCI |
| 28 | TP3, TP6, TP9, TP10 | 4 | 5002 | Test Point | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS |  | Keystone |
| 29 | TP2, TP4, TP7, TP8 | DNP | 5002 | Test Point | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS |  | Keystone |

ISL8105BEVAL1Z Printed Circuit Board Layers


FIGURE 12. ISL8105BEVAL1Z - TOP LAYER (SILKSCREEN)


FIGURE 14. ISL8105BEVAL1Z - LAYER 2


FIGURE 16. ISL8105BEVAL1Z - BOTTOM LAYER


FIGURE 13. ISL8105BEVAL1Z - TOP LAYER (COMPONENT SIDE)


FIGURE 15. ISL8105BEVAL1Z - LAYER 3


FIGURE 17. ISL8105BEVAL1Z - BOTTOM LAYER (SOLDER SIDE)

ISL8105BEVAL2Z Schematic


ISL8105BEVAL2Z Bill of Materials

| ID | REFERENCE | QTY | PART NUMBER | PART TYPE | DESCRIPTION | PACKAGE | VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | U1 | 1 | ISL8105BIRZ | IC, Linear | IC, Single PWM Controller | 10 LD DFN | Intersil |
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| 3 | Q3 | 1 | BSC030N03LS G | MOSFET | 30 V - Channel MOSFET | TDSON-08 | Infineon |
| 4 | Q2, Q4, Q5, Q6 | DNP |  | MOSFET |  |  |  |
| 5 | L1 | 1 | HC9-1R0-R | Inductor | $1.0 \mu \mathrm{H}$, high current inductor | SMD | Cooper Bussmann |
| 6 | SW1 | 1 | EVQ-PAD04M | Push Switch | SWITCH-PUSH, TH, 6 mm , 1P, PUSHB MOM-SPST |  | PANASONIC |
| CAPACITORS |  |  |  |  |  |  |  |
| 7 | C1 | 1 |  | Capacitor, Ceramic, X7R | 10nF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 8 | C2 | 1 |  | Capacitor, Ceramic, X7R | 390pF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 9 | C3 | 1 |  | Capacitor, Ceramic, X7R | 3.3nF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 10 | C4, C9, C10 | 3 |  | Capacitor, Ceramic, X7R | $1 \mu \mathrm{~F}, 25 \mathrm{~V}, 10 \%, \mathrm{X} 7 \mathrm{R}, \mathrm{ROHS}$ | SM_0805 | TDK/Generic |
| 11 | C5, C27, C28 | 3 |  | Capacitor, Ceramic, X7R | 0.1 $\mu \mathrm{F}, 16 \mathrm{~V}, 10 \%, \mathrm{ROHS}$ | SM_0603 | TDK/Generic |
| 12 | C8 | 1 |  | Capacitor, Ceramic, X7R | 680pF, 50V, 10\%, ROHS | SM_0603 | TDK/Generic |
| 13 | C11, C12, C13 | 3 | 35ME330AX | Aluminum Capacitor | $330 \mu \mathrm{~F}, 35 \mathrm{~V}$ | RAD 10x20 | Sanyo |
| 14 | C18, C19, C20, C21 | 4 | 2R5TPF470ML | Organic Alumium Capacitor | $470 \mu \mathrm{~F}, 2.5 \mathrm{~V}, 20 \%$, ROHS | Case D3L | Sanyo |
| 15 | $\begin{aligned} & \text { C6, C7, C14, C15, C16, C17, } \\ & \text { C22, C23, C24, C25, C26 } \end{aligned}$ | DNP |  |  |  |  |  |
| RESISTORS |  |  |  |  |  |  |  |
| 16 | R1 | 1 |  | Resistor, Film | 11.8k $\Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 17 | R2 | 1 |  | Resistor, Film | 12k $\Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 18 | R3 | 1 |  | Resistor, Film | 301ת, 1\%, 1/16W | SM_0603 | Panasonic/Generic |
| 19 | R4 | 1 |  | Resistor, Film | 5.9k $\Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 20 | R5 | 1 |  | Resistor, Film | $1.74 \mathrm{k} \Omega, 1 \%, 1 / 16 \mathrm{~W}$ | SM_0603 | Panasonic/Generic |
| 21 | R6 | 1 |  | Resistor, Film | 4.7 $\Omega$, 1\%, 1/16W | SM_0603 | Panasonic/Generic |
| 22 | R7, R8 | DNP |  |  |  | SM_0603 |  |
| OTHERS |  |  |  |  |  |  |  |
| 23 | TPVO1 | DNP |  | Terminal, Scope Probe | CONN-PIN RECEPTACLE, 0.086 DIA, 0.200 L , ROHS |  | MILL-MAX |
| 24 | J1, J4 | 2 | 111-0702-001 | Blinding Post | CONN-GEN, BIND. POST, RED, THMBNUT-GND |  | JOHNSON COMPONENTS |
| 25 | J3, J5 | 2 | 111-0703-001 | Blinding Post | CONN-GEN, BIND. POST, BLACK, THMBNUT-GND |  | JOHNSON COMPONENTS |
| 26 | J2, J6 | 2 | 1514-2 | Turrett Post | CONN-TURRET, TERMINAL POST, TH, ROHS |  | Keystone |
| 27 | J7 | 1 | 68000-236-1X3 |  | 3-pin Jumper |  | Berg/FCI |
| 28 | TP3, TP6, TP9, TP10 | 4 | 5002 | Test Point | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS |  | Keystone |
| 29 | TP2, TP4, TP7, TP8 | DNP | 5002 | Test Point | CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS |  | Keystone |

ISL8105BEVAL2Z Printed Circuit Board Layers


FIGURE 18. ISL8105BEVAL2Z - TOP LAYER (SILKSCREEN)


FIGURE 20. ISL8105BEVAL2Z - LAYER 2


FIGURE 22. ISL8105BEVAL2Z - BOTTOM LAYER


FIGURE 19. ISL8105BEVAL2Z - TOP LAYER (COMPONENT SIDE)


FIGURE 21. ISL8105BEVAL2Z - LAYER 3


FIGURE 23. ISL8105BEVAL2Z - BOTTOM LAYER (SOLDER SIDE)

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