# RENESAS

# APPLICATION NOTE

## Designing with ISL6752DBEVAL1Z and ISL6754DBEVAL1Z Control Cards

AN1619 Rev 1.00 May 19, 2011

# Introduction

The ISL6752DBEVAL1Z and ISL6754DBEVAL1Z are DC-DC power supply controllers on plug-in daughter cards. Both cards utilize Intersil's ZVS resonant switching full bridge topology specifically intended for off-line, 500W or greater applications.

These two controllers are basically the same except for the method used for current limiting. The ISL6752DBEVAL1Z uses pulse by pulse current limiting while the ISL6754DBEVAL1Z uses Intersil's patented average current limiting technique. Both control cards have secondary referenced voltage error amplifiers with a linear opto-isolator used to transition the primary to secondary boundary.

These cards also provide control signals to drive Synchronous Rectifiers (SRs). An optional control circuit is provided for diode emulation.

This design guide references the power topology of the ISL6752\_54EVAL1Z power supply which comes complete with both of these daughter cards. The daughter cards are also available as stand alone evaluation boards to be used with customer provided power stages. Reviewing the ISL6752\_54EVAL1Z ZVS DC-DC Power Supply with Synchronous Rectifiers-User Guide, <u>AN1603</u>, is highly recommended.

#### Scope

This application note will cover the methods for compensating the voltage error amplifier using current mode control. Biasing the peak current limit of the ISL6752 and ISL6754 is also reviewed. It is assumed that the reader has fundamental understanding of the peak current mode control. Familiarity with application note, AN1262, "Designing with the ISL6752, ISL6753 ZVS Full-bridge Controllers" is also recommended.

Also covered is the compensation of the average current limit error amplifier of the ISL6754.

Another subject covered by this application note is implementation requirements for proper operation of the ISL6754 when transitioning from voltage regulation to current regulation.

### **Basic Design Considerations**

The ISL6754DBEVAL1Z uses two error amplifiers. One error amplifier is used to regulate the output voltage when the output load current is below the current limit value. The other error amplifier is used to regulate the output current when the output current is equal to the average current limit value. In this design example, the current amplifier is internal to the ISL6754. An external op-amp is used as the voltage amplifier.

The output of the two error amplifiers are connected together with an OR-ing diode, as shown in the simplified schematic of Figure 1. When the voltage amplifier is in control of the output, the output of the amplifier is within the control range of the PWM comparator (~ 0V to 5V). The output of the current amplifier is at the positive rail because it is demanding for more current on the output. Because the output of the current amplifier is more positive than the voltage amplifier, the OR-ing diodes block the current amplifier from controlling the output and is effectively operating open loop.



#### FIGURE 1. TWO AMPLIFIERS CONNECTED TO ONE PWM COMPARATOR

When the output load current exceeds the average current limit value, the output of the current amplifier slews rapidly down to the control range of the PWM comparator to regulate the output current. Because the output load current is being limited, the output voltage sags resulting with the output of the voltage error amplifier increasing towards the positive rail voltage. The voltage error amplifier is now operating open loop. Because only one or the other amplifier is in control of the output, it is sufficient to compensate each amplifier independently of the other.

The designer does have to decide how rapidly he or she wants the transition from voltage control to current control to occur. Usually the load transient performance specification determines the compensation for the voltage error amplifier.

There are other considerations for the compensation of the current amplifier. If it is desirable to allow momentary high amplitude load transients that exceed the current limit value, then the current amplifier should be compensated to respond slowly to the load transient. Because it is still necessary to limit the peak load transient current to some safe level, the pulse by pulse current limit of the ISL6754 should be biased to allow the highest acceptable load transient amplitude.

In applications where it is desirable to rapidly limit the output current to the current limit value, the current amplifier can be compensated to provide nearly instantaneous limiting to the current limit value. The transition can be made so fast that the pulse by pulse current may never activate.

With both fast and slow transitions between voltage and current regulation, it is necessary to insure that the minimum input voltage of -0.3V is not exceeded on the FB pin of the ISL6754. When the output of the voltage amplifier is slewing down towards the control range of the PWM comparator, the negative dv/dt on the VERR pin will cause current to flow through the compensation capacitor of the current error



amplifier resulting with a negative transient on the FB pin. A similar effect can occur on the external amplifier.



FIGURE 2. VOLTAGE CLAMPS TO PREVENT EXCESSIVE NEGATIVE TRANSIENTS ON FB

A simple solution to the problem is to implement a negative voltage clamp on this pin, as shown in Figure 2. It may also be necessary to have a similar clamp on the negative input pin of the external amplifier depending on how it responds to excessively negative transients.

### **About this Analysis**

The following design procedure is available in a native MathCad file created with MathCad ver. 14. This file may work with older versions of MathCad but it has not been evaluated with any version other than 14. New MathCad versions, when available, will probably maintain backwards compatibility.

The topology used for this analysis is the ISL6752\_54EVAL1Z, which uses a current doubler secondary. This analysis does not consider the center tap rectification topology. Calculations for the CT topology must be derived by the user.

For those readers who are not familiar with MathCad, the following symbols are defined as follows:

- := Assignment operator. The variable on the left side is assigned the value on the right side
- = This is the usual equals operator. The value of a symbol on the left is displayed on the right
- This operator is used to assign any expression to a
   (bold type) symbol. It is used most frequently when variables of multiple independent equations are evaluated using the find() function

In most cases, this analysis uses ordinary math rules for precedence and can be understood by readers who are not familiar with MathCad. For detailed help with features and functions of MathCad that are incorporated in this analysis, please refer to the <u>MathCad 14 Users Guide</u>.

Included at the end of this application note are the schematics and the PCB layouts of the ISL6752DBEVAL1A and the ISL6754DBEVAL1Z control cards.

#### **Related Literature**

- 1. <u>AN1262</u>, "Designing with the ISL6752, ISL6753 ZVS Full Bridge Controllers", Application Note
- 2. <u>AN1603</u>, "ISL6752\_54EVAL1Z ZVS DC-DC Power Supply with Synchronous Rectifiers-User Guide", Application Note
- 3. <u>FN6754</u>, "ZVS Full-Bridge PWM Controller with Adjustable Synchronous Rectifier Control", Data Sheet
- 4. <u>FN9181</u>, "ZVS Full-Bridge Current-Mode PWM with Adjustable Synchronous Rectifier Control", Data Sheet
- 5. <u>"ISL6752\_54DBEVAL1Z Board Design.mcdx"</u>, Native MathCad Design File

#### References

- [1] MathCad 14 Users Guide
- [2] <u>Unitrode Application Note U-97</u>" Modelling, Analysis and Compensation of the Current-mode Converter"



Author: Richard.Garcia@intersil.com

# intersil

# Biasing the ISL6752\_54EVAL1Z Using Current Mode Control

#### © Intersil Americas Inc. 2011. All Rights Reserved.

You may use this copyrighted Mathcad data sheet solely in conjunction with Intersil products. You may modify and distribute this data sheet. However, the preceding grants of rights are subject to your agreements with the following terms:

Your exploitation of the foregoing rights indicates your agreement to such terms. The copyright notice and the text following it may not be modified or removed from the Mathcad data sheet. This material is provided "as is". Intersil specifically disclaims all warranties, including without limitation the warranties of fitness for a particular purpose and merchantability. To the extent permitted by law, you indemnify Intersil Corporation and its direct and indirect subsidiaries with respect to any claims arising from your use of this Mathcad data sheet.

There are seven major design steps in this analysis:

- 1. Set the oscillator frequency.
- 2. Calculate the value of the current sensing resistor, Rs, for peak current limit.
- 3. Set the slope compensation ratio for peak current mode control for the voltage error amplifier.
- 4. Establish the DC biasing of the average current limit amplifier (ISL6754 only).
- 5. Determine the small signal gain of the peak current mode power stage for bode analysis.
- 6. Compensate the voltage error amplifier.
- 7. Compensate the current error amplifier (ISL6754 only)

Unless otherwise specified, the following analysis applies to both the ISL6752 and the ISL6754 evaluation daughter cards (ISL6752DBEVAL1Z and ISL16754DBEVAL1Z). Because these two boards use different reference designators, this analysis uses designators as defined by the equivalent schematics shown in this document. When applicable, a cross reference table is included to identify the specific parts on each board vs. the reference designator used in this analysis.

The following parameters are for the ISL6752\_54EVAL1Z power supply. With appropriate changes to power components, these parameters can be modified to satisfy a custom application.

Input and output parameters:

Component parameters:

$V_{bus\_max} := 450V$	maximum input operating voltage	$L_{ind} := 3.3 \cdot \mu H$	output inductance	
$V_{bus\_nom} := 400V$	nominal input operating voltage	$N_t := 13$	turns ratio of the power transformer	
$V_{o\_nom} := 12V$	max output voltage	$N_{ct} := 50$	turns ratio of the current sensing transformer	
$V_{o\_min} := 0V$	min output voltage (short circuit)	$V_{CL} := 1V$	Peak Current Limit voltage	
$I_{out\_PK} := 65A$	max for pulse by pulse current limit	$L_{pri} := 3200 \ \mu H$	primary magnetizing inductance of the power transformer	
$I_{out\_min} := 0A$	no load	$C_T := 180 pF$	Oscillator timing capacitor	
$I_{out\_avg} := 60A$	Average current limit	RTD := $6.65 K\Omega$	Timing capacitor discharge resistor (used to set dead time)	

### Step 1) Setting the Oscillator Frequency

$T_C \coloneqq 11.5 \cdot K\Omega \cdot C_T = 2.07 \cdot \mu s$	Charge time for CT as defined in the data sheet. Note that $T_C$ is increased by the presence of the CT slope transistor			
	Q1. To minimize the loading on the CT pin, the beta of Q1 should be greater than 200.			
$T_D := 0.06 \cdot RTD \cdot C_T + 50ns = 122 \cdot ns$	Discharge time for CT (as defined in the data sheet). This is also the dead time between the two FETs on one side of the full bridge.			
$P := T_C + T_D = 2.192 \cdot \mu s$	Calculated PWM period for one half cycle			
Freq := $(2 \cdot P)^{-1} = 228.121 \cdot KHz$	This is the frequency of the full bridge and of each output current doubler inductor. Note that the actual switching frequency of the ISL6752 54EVAL1Z is 200KHz because of the loading effects of Q1 on the CT pin.			
$D_{\max} \coloneqq \frac{P - 1_D}{P} = 0.944$	This is the maximum duty cycle			
$V_{bus\_min} \coloneqq \frac{2}{D_{max}} \cdot N_t \cdot V_{o\_nom} = 330.361 V$	This is the input voltage at which the output begins regulation.			



## Step 2) Rs for pulse by pulse current limit

The nominal Duty cycle for each current doubler inductor:

$$D_{nom\_ind} := \frac{V_{o\_nom}}{V_{bus\_nom}} \cdot N_t = 0.390$$

The nominal on period for  $\,V_{o\_nom} = 12\,V\,$  and  $\,V_{bus\_nom} = 400\,V\,$  :

$$T_{on} := 2 \cdot P \cdot D_{nom\_ind} = 1.71 \cdot \mu s$$

 ${\rm I}_{upramp} \text{ is the } \Delta \text{ i of the current in one output} \\ \text{inductor of the current doubler topology.}$ 

$$I_{upramp} := \left(\frac{\frac{V_{bus\_nom}}{N_t} - V_{o\_nom}}{L_{ind}}\right) \cdot T_{on} = 9.724 \text{ A}$$

 $I_{pri\ mag}$  is the  $\Delta$  i of the primary side magnetizing current.

$$I_{\text{pri}\_\text{mag}} \coloneqq \frac{V_{\text{bus}\_\text{nom}}}{L_{\text{pri}}} \cdot T_{\text{on}} = 0.214 \,\text{A}$$

 $I_{sense,p}$  is the peak output current referenced to the output of the current sensing transformer.

$$I_{sense.p} := \frac{\frac{I_{out\_PK}}{2}}{N_t \cdot N_{ct}} + \frac{\frac{I_{upramp}}{2}}{N_t \cdot N_{ct}} + \frac{\frac{I_{pri\_mag}}{2}}{N_{ct}} = 59.617 \cdot mA$$

 $v_{CT,s} \, \mbox{is the rising slope of the CT signal}$ 

$$V_{\text{CT.s}} \coloneqq \frac{2V}{T_{\text{C}}} = 0.966 \cdot \frac{V}{\mu s}$$

 $v_{\mbox{CTE},p}$  is the peak voltage as seen on the emitter of Q1 at the end of the on period:

$$\begin{split} v_{CTE,p} &\coloneqq v_{CT,s} \cdot \big( T_{on} \big) + .2 V = 1.852 \, V \\ @ \ T_{on} = 1.71 \cdot \mu s \end{split}$$

 $V_{CS}$  is the voltage that is seen on the CS input (calculated using superposition). Peak current limit occurs when  $V_{CS}$  = 1

$$V_{CS} = \frac{R_s}{R_a + R_b + R_s} \cdot V_{CTE,p} + \frac{I_{sense,p}}{R_s^{-1} + (R_a + R_b)^{-1}} = 1V_{CS}$$

#### Period for each current doubler inductor is 2P







### Step 3) Slope compensation

slope compensation ratio definition:

$$M = \frac{V_{ramp.s}}{V_{down.s}} = 1 \quad \text{or} \quad V_{ramp.s} = V_{down.s}$$

Output Inductor current down slope current scaled to the output of the current sensing transformer :

$$I_{down.s} \coloneqq \frac{V_{o_nom}}{L_{ind} \cdot N_t \cdot N_{ct}} \qquad I_{down.s} = 0.006 \cdot \frac{A}{\mu s}$$
$$V_{down.s} = \left[\frac{I_{down.s}}{R_s^{-1} + (R_a + R_b)^{-1}} \cdot \frac{R_b}{R_a + R_b}\right] = \frac{I_{down.s} \cdot R_b \cdot R_s}{R_a + R_b + R_s}$$

Primary side magnetizing up slope current,  $V_{mag.s}$ , scaled to the output of the current sensing transformer:

$$I_{mag.s} := \frac{V_{bus\_nom}}{L_{pri} \cdot N_{ct}} = 0.003 \cdot \frac{A}{\mu s}$$

V<sub>CT.s</sub> and I<sub>mag.s</sub> both contribute to the slope compensation.

$$V_{ramp.s} = \frac{R_a + R_s}{R_a + R_s + R_b} \cdot V_{CT.s} + \frac{R_b \cdot R_s}{R_a + R_b + R_s} \cdot I_{mag.s}$$

substituting (c) and (d) into (b):

$$M = \frac{\frac{R_a + R_s}{R_a + R_s + R_b} \cdot V_{CT.s} + \frac{R_b \cdot R_s}{R_a + R_b + R_s} \cdot I_{mag.s}}{\frac{I_{down.s} \cdot R_b \cdot R_s}{R_a + R_b + R_s}}$$

Simplifying:

$$M = \frac{I_{mag.s}}{I_{down.s}} + \frac{V_{CT.s} \cdot (R_a + R_s)}{I_{down.s} \cdot R_b \cdot R_s}$$

Solving for Rb:

(eq 2) 
$$R_b = -\frac{V_{CT.s} \cdot (R_a + R_s)}{R_s \cdot (I_{mag.s} - I_{down.s} \cdot M)}$$

$$\begin{array}{ll} \mbox{Given} & R_a \coloneqq 499\Omega & R_b \coloneqq 10000\Omega & R_s \coloneqq 20\Omega & M \coloneqq 2 \\ R_s = \frac{1 V \cdot \left(R_a + R_b\right)}{V_{CTE.p} - 1 V + I_{sense.p} \cdot R_a + I_{sense.p} \cdot R_b} \\ R_b = -\frac{V_{CT.s} \cdot \left(R_a + R_s\right)}{R_s \cdot \left(I_{mag.s} - I_{down.s} \cdot M\right)} \\ \begin{pmatrix} R_s \\ R_b \end{pmatrix} \coloneqq Find \left(R_s, R_b\right) = \begin{pmatrix} 16.713 \\ 3431.248 \end{pmatrix} \Omega \\ R_a = 499\,\Omega & R_b = 3.43 \cdot K\Omega & R_s = 16.71\,\Omega \end{array}$$

M = 1 is the optimal slope compensation ratio.  $V_{ramp.s}$  is the ramp added to the current sense scaled to the ramp pin of the ISL6752. V<sub>down.s</sub> is the effective down slope ramp that is proportional to the down slope current of the output inductor also scaled to the ramp pin of the ISL6752. (reference Unitrode app note U-97)

Note that I<sub>down.s</sub> does not actually appear on the output of the current sensing transformer. This value is only used to scale V<sub>ramp.s</sub>

Note that M is composed of two components.

 $\frac{I_{mag.s}}{T}$  is the slope compensation that is contributed by Idown.s

the magnetizing current of the power transformer

and  $\frac{V_{CT,s} \cdot (R_a + R_s)}{I_{down,s} \cdot R_b \cdot R_s}$  is the injected compensation.

This is the second of two equations required to solve for two Resistor variables (Rs and Rb)

Initial estimated values (note that M can be made larger than the optimal value of 1 to overcome noise problems on the ramp input).

The following values are for the actual reference designators on the ISL6752 and ISL6754 daughter cards.

 $R13 := R_a = 499 \Omega$  $R4 := R_s \cdot 2 = 33.4 \Omega$  $R6 := R4 = 33.4 \Omega$  $R17 := R_b = 3431 \Omega$ 

note that R4 and R6

are in parallel Note that the portion of slope compensation ratio contributed

Confirming the slope compensation ratio, M: (-

- )

$$\frac{I_{\text{mag.s}}}{I_{\text{down.s}}} + \frac{V_{\text{CT.s}} \cdot (R_a + R_s)}{I_{\text{down.s}} \cdot R_b \cdot R_s} = 2 \qquad \qquad \frac{I_{\text{mag.s}}}{I_{\text{down.s}}} = 0.447$$

I<sub>mag.s</sub>

by  $\frac{I_{mag.s}}{I_{down.s}}$  can be significant. If  $L_{pri}$  is small enough, Idown.s by itself can be be greater than 1.



### Step 4) Average Current limit (ISL6754 only)

In the above calculations, the value of Rs is calculated for pulse by pulse current limiting for  $I_{out\_PK} = 65 \,\text{A}$ . The average current limit is set to a lower value ( $I_{out\_avg} = 60 \,\text{A}$ ) to prevent the peak current limiting from interfering with the average current limit control loop.

$$V_{Iout} := \frac{I_{out\_avg}}{2 \cdot N_t \cdot N_{ct}} \cdot R_s \cdot 4 = 3.085 V$$

This is the output voltage on the lout pin of the ISL6754 when  $I_{out\_avg}=60\,\mathrm{A}$  .

To limit the output current to  $I_{out_avg}$ , the resistor divider of R25 and R26 are chosen so that the voltage on FB (pin 7) is .6V when  $V_{Iout} = 3.085 V$ . For accurate performance, the maximum load on the lout pin should also be limited to approximately 100 uA.

$$R26 := 6K\Omega \qquad R25 := 10K\Omega$$
$$\frac{R26}{R25 + R26} \cdot V_{Iout} = .6V$$
$$\frac{V_{Iout}}{R25 + R26} = 100 \cdot \mu A$$
$$\binom{R25}{R26} := Find(R25, R26) = \binom{24.9}{6.0} \cdot K\Omega$$

These are the actual values used on the ISL6754DBEVAL1Z control board:

 $R25 := 22100\Omega$ 



# Step 5) Small Signal Gain of the Current Mode Power stage (lout/Verr)

The input to the positive side of the PWM comparator (using superposition):

 $R26 := 6650\Omega$ 

$$V_{pwm\_pos} = \frac{I_{sense} \cdot R_b \cdot R_s}{R_a + R_b + R_s} + \frac{R_a + R_s}{R_s + R_a + R_b} \cdot \left(V_{CT,s} \cdot D \cdot 2P - .6V\right) + 80mV$$

where  $I_{sense}$  and D are variables

The input to the negative side of the PWM comparator:

$$V_{pwn_neg} = \frac{Verr - 2 \cdot V_{diode}}{3}$$
 where Verr is a variable

The duty cycle terminates when  $V_{pmw_pos} = V_{pwm_neg}$ :

$$(eq A) \quad \frac{I_{sense} \cdot R_b \cdot R_s}{R_a + R_b + R_s} + \frac{R_a + R_s}{R_s + R_a + R_b} \cdot \left(V_{CT.s} \cdot D \cdot 2P - .6V\right) + 80mV = \frac{V_{err} - 2 \cdot .6V}{3}$$

Peak Current sense:

(eq B) 
$$I_{\text{sense}} = \frac{I_{\text{out}}}{2 \cdot N_t \cdot N_{\text{ct}}} + \frac{V_{\text{bus}} \cdot N_t^{-1} - V_o}{L_{\text{ind}} N_t \cdot N_{\text{ct}}} \cdot D \cdot P + \frac{V_{\text{bus}}}{L_{\text{pri}} \cdot N_{\text{ct}}} \cdot D \cdot P$$

Duty cycle:

$$(eq C) \quad D = \frac{V_o}{V_{bus}} \cdot N_t$$



The first term of eq. B is the average current of one current doubler output inductor. The 2nd term is the up slope current of one output inductor. The 3rd term is the up slope current of the primary referenced magnetizing inductance (Lpri) of the power transformer.

Substituting definitions of duty cycle D, eq C, and  $I_{sense}$ , eq b, into eq A and simplifying:

$$\frac{R_b \cdot R_s}{R_a + R_b + R_s} \cdot \left( \frac{I_{out}}{2 \cdot N_t \cdot N_{ct}} + \frac{V_{bus} \cdot N_t^{-1} - V_o}{L_{ind} N_t \cdot N_{ct}} \cdot D \cdot P + \frac{V_{bus}}{L_{pri} \cdot N_{ct}} \cdot D \cdot P \right) + \frac{R_a + R_s}{R_s + R_a + R_b} \cdot \left( \frac{2 \cdot N_t \cdot P \cdot V_o \cdot V_{CT,s}}{V_{bus}} - .6V \right) + 80mV = \frac{V_{err} - 2 \cdot .6V}{3}$$

solving for  $\mathrm{I}_{out}\,$  and isolating  $\mathrm{V}_{err}$ 

(eq E)

$$I_{out} = \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{\left(R_a + R_b + R_s\right)}{\left(R_b \cdot R_s\right)} \cdot V_{err} + \frac{N_t \cdot N_{ct'} \cdot V \cdot \left(0.24 \cdot R_a - 0.96 \cdot R_b + 0.24 \cdot R_s\right)}{R_b \cdot R_s} \dots + \frac{-2 \cdot N_t \cdot P \cdot V_o \cdot V_{CT.s}}{V_{bus}} \cdot \frac{2 \cdot N_t \cdot N_{ct'} \left(R_a + R_s\right)}{R_b \cdot R_s} - \frac{P \cdot V_o \cdot \left(V_{bus} - N_t \cdot V_o\right)}{L_{ind'} \cdot N_t \cdot N_{ct'} \cdot V_{bus}} \cdot \left(2 \cdot N_t \cdot N_{ct}\right) - \frac{2 \cdot N_t^2 \cdot P \cdot V_o}{L_{pri}}$$

(eq E) is formatted as y=mx+b format where m is the slope and b is the offset of a line equation.

where:

$$\begin{aligned} \mathbf{x} &= \mathrm{V}_{err} \\ m &= \frac{2 \cdot \mathrm{N}_{t} \cdot \mathrm{N}_{ct}}{3} \cdot \frac{\left(\mathrm{R}_{a} + \mathrm{R}_{b} + \mathrm{R}_{s}\right)}{\left(\mathrm{R}_{b} \cdot \mathrm{R}_{s}\right)} \\ \text{and} \\ b &= \\ \frac{\mathrm{N}_{t} \cdot \mathrm{N}_{ct} \cdot \mathrm{V} \cdot \left(0.24 \cdot \mathrm{R}_{a} - 0.96 \cdot \mathrm{R}_{b} + 0.24 \cdot \mathrm{R}_{s}\right)}{\mathrm{R}_{b} \cdot \mathrm{R}_{s}} - \frac{2 \cdot \mathrm{N}_{t} \cdot \mathrm{P} \cdot \mathrm{V}_{o} \cdot \mathrm{V}_{CT.s}}{\mathrm{V}_{bus}} \cdot \frac{2 \cdot \mathrm{N}_{t} \cdot \mathrm{N}_{ct} \cdot \left(\mathrm{R}_{a} + \mathrm{R}_{s}\right)}{\mathrm{R}_{b} \cdot \mathrm{R}_{s}} - \frac{\mathrm{P} \cdot \mathrm{V}_{o} \cdot \left(\mathrm{V}_{bus} - \mathrm{N}_{t} \cdot \mathrm{V}_{o}\right)}{\mathrm{L}_{ind} \cdot \mathrm{N}_{t} \cdot \mathrm{N}_{ct} \cdot \mathrm{V}_{bus}} \cdot \left(2 \cdot \mathrm{N}_{t} \cdot \mathrm{N}_{ct}\right) - \frac{2 \cdot \mathrm{N}_{t}^{2} \cdot \mathrm{P} \cdot \mathrm{V}_{o}}{\mathrm{L}_{pri}} \end{aligned}$$

For AC analysis,  $V_o$  and  $V_{bus}$  are constants. The slope, m, is the small signal gain,  $g_t$ , used for the bode analysis of the peak current mode power stage



These values are repeated here for reference.

To validate the above calculations,  $\rm I_{out}$  is redefined as a function of  $\rm V_o$  ,  $\rm V_{bus}$  and  $\rm V_{err}$ 

$$I_{out}(V_{o}, V_{bus}, V_{err}) := \begin{bmatrix} \frac{2 \cdot N_{t} \cdot N_{ct}}{3} \cdot \frac{(R_{a} + R_{b} + R_{s})}{(R_{b} \cdot R_{s})} \cdot V_{err} + \frac{N_{t} \cdot N_{ct} \cdot V \cdot (0.24 \cdot R_{a} - 0.96 \cdot R_{b} + 0.24 \cdot R_{s})}{R_{b} \cdot R_{s}} \dots \\ + \frac{2 \cdot N_{t} \cdot P \cdot V_{o'} \cdot V_{CT,s}}{V_{bus}} \cdot \frac{2 \cdot N_{t} \cdot N_{ct} (R_{a} + R_{s})}{R_{b} \cdot R_{s}} - \frac{P \cdot V_{o'} (V_{bus} - N_{t'} \cdot V_{o})}{L_{ind} \cdot N_{t'} \cdot N_{ct} + V_{bus}} \cdot (2 \cdot N_{t} \cdot N_{ct}) - \frac{2 \cdot N_{t}^{2} \cdot P \cdot V_{o}}{L_{pri}} \end{bmatrix}$$

$$V_{error} := 0.5V, 1V \dots 5V \quad V_{o_{n}om} := 12V \quad V_{o_{min}} := 6V \quad V_{bus_{max}} = 450V \quad V_{bus_{n}om} = 400V \quad V_{bus_{min}} = 330.361V$$

$$I_{out}(V_{o_{n}om}, V_{bus_{max}}, V_{error}) = 80.0 \quad I_{out}(V_{o_{min}}, V_{bus_{min}}, V_{error}) = 60.0 \quad I_{out}(V_{o_{min}}, V_{bus_{max}}, V_{error}) = 60.0 \quad I_{out}(V_{o_{min}}, V_{bus_{max}}, V_{error}) = 50.0 \quad I_{out}(V_{o_{min}}, V_{bus_{min}}, V_{error}) = 60.0 \quad I_{out}(V_{o_{min}}, V_{bus_{max}}, V_{error}) = 60.0 \quad I_{out}(V_{o_{min}}, V_{bus_{min}}, V_{error}) = 60.0 \quad I_{out}(V_{o_{min}}, V_{out}, V_{out}, V_{out}, V_{out}, V_{out}, V_{out}, V_{out}, V_{out}, V_{ou$$



The slope of these lines is the small signal gain  $\frac{i_{out}}{v_{err}} = g_t$ 

These plots illustrate how lout varies as  $V_{error}$ ,  $V_{bus}$ , and  $V_o$  are changed. For constant  $V_{o\_nom} = 12V$  (solid lines) or constant  $V_{o\_min} = 6V$  (dotted lines), Vbus exhibits minimal influence on  $I_{out}$  as expected. For  $V_{bus\_min} = 330.4V$  to  $V_{bus\_max} = 450V$  (the operating input voltage range),  $I_{out}$  changes very little for a constant  $V_{error}$ .

As  $V_o$  is varied, between  $V_{o\_nom}$  and  $V_{o\_min}$ ,  $g_t$  remains constant. This is also expected because the slope compensation does not changed as  $V_o$  deviates from the nominal output voltage of 12V. When  $V_o$  decreases, as it will during current limit, the down slope current of the output inductors also decreases effectively increasing the slope compensation because the injected slope compensation from Vct does not change.



This gain function is used in the bode analysis for the ISL6752 and ISL6754.



 $X_{pwm}$  is the gain of the PWM current mode power stage.  $v_{out}$  is the small signal output voltage and  $v_{err}$  is the small signal control voltage from the error amplifier.

 $\mathbf{g}_t$  is the transconductance of the PWM current mode stage.

 $z_{out}$  is the load impedance on the output of the current mode power stage.  $R_L$  is the output load,  $C_{out}$  is the output capacitance and  $R_{esr}$  is the ESR of the output capacitance.

note: the impedance of two parallel components is

$$\frac{1}{z} = \frac{1}{z^1} + \frac{1}{z^2}$$
 or  $z = (z^{-1} + z^{-1})^{-1}$ 

The small signal gain has a pole at 1/2 the switching frequency (refer to Unitrode application note U-97)



# Step 6) Compensation of the Voltage Error Amplifier

#### **Functions for Bode Analysis**

 $db(G, f) \coloneqq 20 \log(|G(2\pi f \cdot j)|)$  $\phi(\mathbf{G},\mathbf{f}) \coloneqq \operatorname{mod}\left(\arg\left(\mathbf{G}\left(2\pi\,\mathbf{f}\cdot\mathbf{j}\right)\right)\cdot\frac{180}{\pi},360\right)$  $f_{\text{UnityGain}}(G) := \left| \text{root}(db(G, f), f, 100, 10^8) \right|$  $\phi_{\text{margin}}(G) \coloneqq \phi(G, f_{\text{UnityGain}}(G)) + 0$  $V_{db2V} \big( db_v \big) \coloneqq 10^{\left( db_v \cdot 20^{-1} \right)}$  $\underbrace{F}(f_0,f_N,N,i) \coloneqq \quad \text{for } i \in 0 .. N$  $f_{i} \leftarrow f_{0} \cdot \left(\frac{f_{N}}{f_{0}}\right)^{\frac{i}{N}}$ 

$$\begin{split} & \underbrace{\mathbf{N}}_{i} := 200 \qquad i := 0.. \, \mathrm{N} \\ & \mathbf{f} := \mathbf{F} \Big( .01 \, , 1 \times 10^{8} \, , \mathrm{N} \, , i \Big) \qquad \mathbf{f}_{0} = 0.01 \qquad \mathbf{f}_{\mathrm{N}} = 100 \times 10^{6} \end{split}$$

Gain in decibels of a Laplace gain function G for frequency f

Phase in degrees of a Laplace gain function G

Unity gain frequency of function G

Unity gain phase margin of function G

db to voltage function

Equidistant frequency data points for plotting:

This function generates N equidistant frequency data points on the log X scale with starting frequency  $f_0$  and ending frequency f<sub>N</sub>

### Open loop gain of the LMV431



The open loop transfer function of the LMV431 is created here by inserting poles as necessary to recreate the Gain/Phase plot found in the data sheet. Note that the phase shift is relative to the input.





### Gain of the Voltage Amplifier

For an Inverting Opamp the gain function, X(s), can be simplified to:

$$X_{\text{Verror.Amp}}(s) = \frac{\text{Vo}}{\text{Vi}} = \frac{\text{H1}(s) \cdot \text{G}_{\text{LMV431}}(s)}{1 - \text{H2}(s) \cdot \text{G}_{\text{LMV431}}(s)}$$
  

$$\text{H1}_{\text{U1}}(s, \text{R3}, \text{R4}, \text{R5}, \text{Rx}, \text{Cx}) := \frac{\left[\left(\frac{1}{\text{Cx} \cdot s} + \text{Rx}\right)^{-1} + \frac{1}{\text{R5}}\right]^{-1}}{\left[\left(\frac{1}{\text{Cx} \cdot s} + \text{Rx}\right)^{-1} + \frac{1}{\text{R5}}\right]^{-1} + (\text{R3} + \text{R4})}$$
  

$$\text{H2}_{\text{U1}}(s, \text{R3}, \text{R4}, \text{R5}, \text{Rx}, \text{Cx}) := \frac{\left[\frac{1}{(\text{R3} + \text{R4})} + \frac{1}{\text{R5}}\right]^{-1}}{\left[\frac{1}{(\text{R3} + \text{R4})} + \frac{1}{\text{R5}}\right]^{-1} + \left[\left(\frac{1}{\text{Cx} \cdot s} + \text{Rx}\right)^{-1}\right]^{-1}}$$



gain block diagram for an inverting amplifier



These values are used here only to illustrate and confirm the gain/phase functions

 $R3 := 18 \cdot 10^{3} \qquad Cx := .1 \cdot 10^{-9} \qquad R4 := 649 \qquad R5 := 2.15 \cdot 10^{3} \qquad Rx := 0$  $X_{Verror.Amp}(s) := \frac{H1_{U1}(s, R3, R4, R5, Rx, Cx) \cdot G_{LMV431}(s)}{1 - H2_{U1}(s, R3, R4, R5, Rx, Cx) \cdot G_{LMV431}(s)}$ 



### Open loop gain of EL5111

(note: some earlier releases of the ISL6752DBEVAL1Z and ISL6754DVEVAL1A use the EL5120 instead of the EL5111. The EL5120 has been obsoleted and is not recommended for new designs. In this application, the EL5120 and EL5111 are interchangeable.)



Note that the phase of this graph is the output referenced to the negative input of the opamp.

The open loop transfer function of the EL5111 is created here by inserting poles as necessary to recreate the gain/phase plot found in the data sheet.





#### Gain of the EL5111 Compensation amplifier



The compensation amplifier provides two functional advantages. First, the optocoupler, D2, is biased with a constant voltage across the collector and emitter. The closed DC feedback loop around U2 keeps the negative input virtually at the same voltage as the positive input resulting with a constant DC voltage (VDD - 5V) across the optocoupler. The advantage of this cascode configuration is that there is no regenerative AC feed back through Ccb of the opto transistor. Consequently, the pole introduced by the optocoupler is greatly increased in frequency. The improved bandwidth of the opto removes its detrimental influence on the voltage feedback loop.

Note that R13 is the same value in the ac model as it is in the actual circuit. This is the consequence of the optocoupler having a nominal ctr = 1. Also, note the negative value of Vin in the equivalent AC Model. This is necessary because in the actual circuit, Vin and Vout at low frequencies are in phase. In the equivalent AC Model, because the opamp is an inverting configuration, Vin must be negated to preserve the correct phase of the actual circuit.

The second advantage of this opamp is that the loop compensation network is on the secondary side. Traditionally, the compensation network is applied around the LMV431. The problem is that when the average current regulator takes control of the loop to regulate the output current (by controlling the PWM input), the voltage regulator loop is opened causing the LMV431 output to saturate to the positive rail (Vout). If the voltage loop compensation is around the LMV431, the feedback network will greatly slow the slew rate (~ msecs) of the output of the LMV431. If the load is quickly reduced below the current regulation value (the current limit), the output voltage will overshoot until the output of the LMV431 slews down to the voltage necessary to regulate the output voltage (taking control away from the current regulator). This effect is especially bad for a short circuit load dump. If the loop compensation is not located around the LMV431, the output of the LMV431 will still saturate when the current regulator is in control of the PWM input, but the output is not now impeded by the local feedback and will recover very quickly minimizing the output voltage overshoot.

Note that the compensation network around U2 is decoupled from the output of U2 by the series diode on the output. This diode prevents the feedback network capacitor from charging up to the rail voltage. This same technique is used on the output of the current regulator opamp (internal to the ISL6754). In a manner similar to the voltage control loop, the output of the current regulator is saturated when the voltage loop has control. Without the diode on its output, the current regulator would also be slow to respond to an over current for the same reason as stated for the voltage regulator loop.

The voltage gain function for an Inverting Opamp:

gain block diagram for an inverting amplifier



These values are used here only to illustrate and confirm the compensation around the EL5111 amplifier:

R23 := 4000 R24 :=  $10 \cdot 10^{126}$  R13 := 2200 Cx :=  $100 \cdot 10^{-123}$  C9 :=  $.01 \cdot 10^{-6}$ 

$$X_{\text{Comp.Amp}}(s) := \frac{-(\text{H1}_{\text{U2}}(s, \text{R13}, \text{R24}, \text{R23}, \text{C9}, \text{Cx}) \cdot \text{G}_{5111}(s))}{1 - \text{H2}_{\text{U2}}(s, \text{R13}, \text{R24}, \text{R23}, \text{C9}, \text{Cx}) \cdot \text{G}_{5111}(s)}$$



#### Current mode PWM power stage gain with output loads

The derivation of this small signal gain for the PWM power stage is found in step 5).

$$g_{t} = \frac{2 \cdot N_{t} \cdot N_{ct}}{3} \cdot \frac{(R11 + R14 + R1_{2})}{(R14 \cdot R1_{2})}$$

$$X_{pwm}(s) = g_{t} \cdot \left(\frac{s}{Freq \cdot \pi} + 1\right)^{-1} \cdot \left[R_{L}^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s}\right)^{-1}\right]^{-1}$$



Converting  $X_{pwm}$  to a function:

R11 := 499	N <sub>t</sub> := 13	$C_{out} := 8800 \cdot 10^{-6}$	$V_{out} \coloneqq 12$
$R14 := 9.09 \cdot 10^3$	$N_{ct} := 50$	$R_{esr} \coloneqq 0.02$	$I_{out} := 60$
R1_2 := 13.2		Freq := 208300	$R_L := \frac{V_{out}}{I_{out}}$

$$g_t := \frac{2 \cdot N_t \cdot N_{ct}}{3} \cdot \frac{(R11 + R14 + R1_2)}{(R14 \cdot R1_2)} = 34.678$$

$$X_{pwm}(s) := g_t \cdot \left(\frac{s}{Freq \cdot \pi} + 1\right)^{-1} \cdot \left[R_L^{-1} + \left(R_{esr} + \frac{1}{C_{out} \cdot s}\right)^{-1}\right]^{-1}$$



### Bode plot for the total Voltage loop gain

The  $R_{esr}$  contributes significantly to the stability of the loop by introducing a zero to the bode of PWM current mode power stage. With  $R_{esr} = 0$ , the phase margin of the complete loop is at a minimum (but still stable). With increasing values of ESR, the phase margin improves and the unity grain frequency increases. The nominal value of  $R_{esr}$  of the ISL6754EVAL board is 0.02 ohms. But as operating temperatures decrease, the  $R_{esr}$  value increases resulting in the unity grain frequency. To avoid PWM switching frequency instability, it is wise to add a pole on the U2 amplifier to reduce the unity grain frequency.

In this design example, if the gain of the compensation amplifier is set for no poles and zeros (except for the inherent pole of the amplifier) by setting R23 to infinity and/or by setting C9 to a very small value (although not zero), the loop is stable without any further compensation. This is the consequence of the single pole of the LMV431 error amplifier and the zero of the PWM current mode stage canceling each other.

As with any analysis, some assumptions are made. In this bode analysis, the following assumptions were made:

1) The esl of the output capacitors are assumed not to significantly contribute the the bode of the PWM to output gain stage.

2) the turn off delays of the PWM control and bridge FETs is assumed to be insignificant. In reality, the turn off delay may result in non-linear transconductance gains of the PWM current mode stage. It is important that the turn off delays be as minimal as possible (~1% of the total PWM switching period).

3) the bandwidth of the opto transistor is assumed to be high enough to not contribute poles that affect the closed loop phase.

Because other parasitic effects may also result with unexpected loop response, it is absolutely necessary to actually measure the bode response to insure that the loop compensation is adequate.

Error amplifier

 $\begin{aligned} &\text{R3} \coloneqq 18 \cdot 10^{3} \\ &\text{R4} \coloneqq 649 \\ &\text{R5} \coloneqq 2.15 \cdot 10^{3} \\ &\text{Rx} \coloneqq 0 \\ &\text{Cx} \coloneqq 100 \cdot 10^{-12} \\ &\text{X}_{error.Amp}(s) \coloneqq \frac{\text{H1}_{U1}(s, \text{R3}, \text{R4}, \text{R5}, \text{Rx}, \text{Cx}) \cdot \text{G}_{\text{LMV431}}(s)}{1 - \text{H2}_{U1}(s, \text{R3}, \text{R4}, \text{R5}, \text{Rx}, \text{Cx}) \cdot \text{G}_{\text{LMV431}}(s)} \end{aligned}$ 

#### Compensation amplifier

R23 := 5000 R13 := 5000 R24 := 5000  $C9 := 1 \times 10^{-6}$  $Cx := 1 \cdot 10^{-126}$ 

$$X_{\text{Comp,Amp}}(s) \coloneqq \frac{-(H1_{U2}(s, R13, R24, R23, C9, Cx) \cdot G_{5111}(s))}{1 - H2_{U2}(s, R13, R24, R23, C9, Cx) \cdot G_{5111}(s)}$$





Compensation Amp



 $X_{total.gain.RLmax}(s) \coloneqq X_{error.Amp}(s) \cdot X_{Comp.Amp}(s) \cdot X_{pwm.RLmax}(s)$ 



X<sub>pwm,RLmin</sub> Gain function for min load

X<sub>pwm.RLmax</sub>Gain function for max load





### Load Regulation

As can be seen in the above bode plots, the low frequency closed loop gains at minimum load and maximum load varies significantly primarily because of the change in gain of the PWM output stage. The consequence is that the output voltage will droop as the load increases from minimum to maximum. This droop is relatively large in this design example because the gain of the LMV431 error amplifier is relatively low (especially when compared to the EL5111).

> Where  $A_{\text{vOLoop}}$  is the open loop gain including all of the gain elements (LMV431, EL5111, and PWM output).

$V_{ref} \coloneqq 1.24V$	The reference voltage of the LMV431
$V_{out} \coloneqq 12V$	The output voltage of the ISL6754EVAL board
R5 := 2.15 KΩ $R3_4 := 18.649 KΩ$	R3_4 is the sum of R3 and R4

1)  $(V_{ref} - V_{neg}) \cdot A_{VOLoop} = V_{out}$ 

also

1

2) 
$$V_{\text{neg}} := \frac{R5}{R5 + R3} \cdot V_{\text{out}}$$

substituting 2) into 1):

$$\left(V_{ref} - \frac{R5 \cdot V_{out}}{R5 + R3\_4}\right) \cdot A_{VOLoop} = V_{out}$$

solving for Vout and converting to a function:

$$Vout(A_{VOLoop}) := \frac{V_{ref}}{\frac{R5}{R5 + R3_4} + \frac{1}{A_{VOLoop}}}$$



Because the Xtotal gain includes the degenerative gain of the voltage scaling resistors R3 4 and R5, we must exclude this gain stage from this load regulation analysis.

 $Vout(V_{db2V}(db(G_{LMV431}, f_0) + db(X_{Comp,Amp}, f_0) + db(X_{pwm,RLmin}, f_0))) = 11.9957 \cdot V$ 

 $\operatorname{Vout}(\operatorname{V}_{db2V}(\operatorname{db}(\operatorname{G}_{LMV431}, \operatorname{f}_{0}) + \operatorname{db}(\operatorname{X}_{\operatorname{Comp}, \operatorname{Amp}}, \operatorname{f}_{0}) + \operatorname{db}(\operatorname{X}_{pwm, RLmax}, \operatorname{f}_{0}))) = 11.9652 \cdot \operatorname{V}_{2}$ 

This is the DC output voltage when  $I_{out.min} = 0.011$ 

This is the DC output voltage when  $I_{out,max} = 66$ 



Load regulation:

$$\text{LoadReg}_{\text{LMV431}} \coloneqq \frac{\text{Vout}(\text{V}_{\text{db2V}}(\text{db}(\text{G}_{\text{LMV431}}, \text{f}_{0}) + \text{db}(\text{X}_{\text{Comp.Amp}}, \text{f}_{0}) + \text{db}(\text{X}_{\text{pwm.RLmax}}, \text{f}_{0})))}{\text{Vout}(\text{V}_{\text{db2V}}(\text{db}(\text{G}_{\text{LMV431}}, \text{f}_{0}) + \text{db}(\text{X}_{\text{Comp.Amp}}, \text{f}_{0}) + \text{db}(\text{X}_{\text{pwm.RLmax}}, \text{f}_{0}))))} = 99.746 \cdot \%$$

If an EL5111 is substituted for the LMV431 as the error amplifier, additional gain is added to the open loop gain which improves the load regulation:

$$\begin{aligned} db(G_{LMV431}, f_0) &= 57 & \text{Low Frequency gain of the LMV431} \\ db(G_{5111}, f_0) &= 68 & \text{Low Frequency gain of the EL5111} \\ Vout(V_{db2V}(db(G_{5111}, f_0) + db(X_{Comp.Amp}, f_0) + db(X_{pwm.RLmin}, f_0))) &= 11.9957 \cdot V & \text{This is } when I_{d} \\ Vout(V_{db2V}(db(G_{5111}, f_0) + db(X_{Comp.Amp}, f_0) + db(X_{pwm.RLmax}, f_0))) &= 11.9871 \cdot V & \text{This is } voltage \\ LoadReg_{EL5111} &\coloneqq \frac{Vout(V_{db2V}(db(G_{5111}, f_0) + db(X_{Comp.Amp}, f_0) + db(X_{comp.Amp}, f_0) + db(X_{pwm.RLmax}, f_0)))}{Vout(V_{db2V}(db(G_{5111}, f_0) + db(X_{Comp.Amp}, f_0) + db(X_{pwm.RLmax}, f_0)))} &= 99.928 \cdot \% \end{aligned}$$

This is the DC output voltage when  $\mathrm{I}_{out.min}=0.011$ 

This is the improved DC output voltage when  $I_{out,max} = 66$ 

# Step 7) Compensation of the Current Error Amplifier

#### Open Loop Gain of the ISL6754 Internal Amplifier

 $G_{6754}(s) := \frac{-V_{db2V}(100)}{\left(\frac{s}{50 \cdot 2 \cdot \pi} + 1\right)}$ 

The GBWP of the internal amplifier is specified as 5MHz. Although, the maximum gain a low frequencies is not specified, for the purpose of this analysis, the max gain is assumed to be 100db.



### Gain of the Current Error Amplifier

The scaling factor for current sensing (From step 4)



For an Inverting Opamp the gain function, X(s), can be simplified to:

$$X_{\text{Ierror.Amp}}(s) = \frac{V_0}{I_{\text{out\_avg}}} = \frac{H1(s) \cdot G_{6754}(s)}{1 - H2(s) \cdot G_{6754}(s)} \cdot \left(\frac{4R_s}{2 \cdot N_t \cdot N_{\text{ct}}}\right)$$

$$H1_{U1}(s, R25, R26, R38, C11) := \frac{\left[\left(\frac{1}{C11 \cdot s} + R38\right)^{-1} + \frac{1}{R26}\right]^{-1}}{\left[\left(\frac{1}{C11 \cdot s} + R38\right)^{-1} + \frac{1}{R26}\right]^{-1} + (R25)}$$

$$H2_{U1}(s, R25, R26, R38, C11) := \frac{\left[\frac{1}{(R25)} + \frac{1}{R26}\right]^{-1}}{\left[\frac{1}{(R25)} + \frac{1}{R26}\right]^{-1} + \left[\left(\frac{1}{C11 \cdot s} + R38\right)^{-1}\right]^{-1}}$$



These values are used to compensate the current regulation closed loop.

$$C11 := .01 \cdot 10^{-6}$$
 R38 := 0

$$X_{\text{Ierror.Amp}}(s) := \frac{H1_{U1}(s, R25, R26, R38, C11) \cdot G_{6754}(s)}{1 - H2_{U1}(s, R25, R26, R38, C11) \cdot G_{6754}(s)} \cdot \left(\frac{4 \times 100}{2 \cdot N_t \cdot N_{\text{ct}}}\right)$$

# Gain of the PWM Current Mode Power Stage

From step 5)





gain block diagram for the Current error amplifier

# **Total Current Regulation Loop**

**Gair**  $_{C11} = 10 \times 10^{-9}$  R38 = 0

 $X_{Iloop.total.gain}(s) \coloneqq X_{Ierror.Amp}(s) \cdot g_t(s)$ 



AN1619 Rev 1.00 May 19, 2011



# ISL6754DBEVAL1Z Schematic



FIGURE 3. ISL6754 CONTROL CARD SCHEMATIC

# ISL6752DBEVAL1Z Schematic

סקע R29 ŵ R8 +12VOUT J2 3 -//// 499 R.30 -/// DNP Ś≚ ≞≷₽ D5 μ R31 Ň OPEN -///-1K TP\_SEC C12 R33 망 홍합  $\bigcirc$ Ċ2 C1 🗍 -///-499 0.1UF , ⊾2≷₽ 0.1UF U1 لم لم PS27Ø1 ïž≶ä 4 U.3 D4 EL5111 SGND MU43LATM K N ζŖ -///-R24 1K C7  $\bigcirc$ 23 C13 0.01UF ¥ ₹Ø.1UF ӡ 0. 1UF ้ณ่ C14 SGND J2 4 PGND  $\uparrow$ TSW-107-08-T-D-RA VDD JI V<u>RE</u>F VREF JI-2 υ4 C11 MMBT2222LT1 16 ŋ∔≒ 85 58 58 VDD 0.1UF VADJ 2 15 VREF OUTLL ø ₽Şĕ 2 01 14 5 JI OUTLR з VERR OUTLR PGND 13 4 7. JI OUTUL CTBUF OUTUL  $\uparrow$ 5 12 9 JI OUTUR OUTUR RTD 6 11 11. JI OURLLN RESDEL OUTLLN 7 10 13 JI OUTLRN СТ OUTLRN VDD ₽₹₹ GND 9 8 -cs VREP ISL6752AAZA ΞŻ R1,3 CS+ JTI-6 R2,3 -\//-499 82 91.95 1.95 ₽Š¥ -///-1M äŞ₹ ₹ġ DЗ TSW-102-08-T-D-RA Ŷ R12 VREF -JZ SR\_ENABLE R19 5 CS JTI B U2 BSS1.38 -//// 10K 2. JZ SGND R,32 R34 m Leder 100F 2 PGND JI 14 -//// 10К ~~~ 1К 1컵 02 EL5111 C5 6.654 30 C1Ø a.i⊑ C4 PS27Ø1 , Péşi cilişi Cilişi TP\_PRI 5Š₽ <u>+</u>4 T ABPF ñ Ş뙺 \_ B2PF 47PF ĥ PGND JI 12 Ş₿ C16  $\bigcirc$ CS- JI-10 PGND PGND ( 는 DISABLE DI-4

FIGURE 4. ISL6752 CONTROL CARD SCHEMATIC

ISL6754DBEVAL1Z REV.B



FIGURE 5. ISL6754 CONTROL CARD TOP ASSEMBLY





# ISL6754DBEVAL1Z REV.B

FIGURE 6. ISL6754 CONTROL CARD TOP LAYER





FIGURE 7. ISL6754 CONTROL CARD BOTTOM LAYER





FIGURE 8. ISL6752 CONTROL CARD TOP ASSEMBLY



# ISL6752DBEVAL1Z REV.B



FIGURE 9. ISL6752 CONTROL CARD TOP LAYER



# ISL6752DBEVAL1Z REV.B



FIGURE 10. ISL6752 CONTROL CARD BOTTOM LAYER



#### Notice

- 1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information
- 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples
- 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- 4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
- Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
  - "Standard" Computers: office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment: industrial robots: etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc. Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

- 6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics oroducts outside of such specified ranges
- 7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
- 8. Plea e contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- 9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions
- 10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
- 11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics
- 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

# RENESAS

#### SALES OFFICES

#### **Renesas Electronics Corporation**

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information

Renesas Electronics America Inc. 1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A. Tel: +1-408-432-8888, Fax: +1-408-434-5351 Renesas Electronics Canada Limited 9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3 Tel: +1-905-237-2004 Renesas Electronics Europe Limited Dukes Meadow, Miliboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K Tei: +44-1628-651-700, Fax: +44-1628-651-804 Renesas Electronics Europe GmbH Arcadiastrasse 10, 40472 Düsseldorf, Germar Tel: +49-211-6503-0, Fax: +49-211-6503-1327 Renesas Electronics (China) Co., Ltd. Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China Tel: +86-10-8235-1155, Fax: +86-10-8235-7679 Renesas Electronics (Shanghai) Co., Ltd. Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China Tel: +86-21-2226-0888, Fax: +86-21-2226-0999 Renesas Electronics Hong Kong Limited Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong Tel: +852-2265-6688, Fax: +852 2886-9022 Renesas Electronics Taiwan Co., Ltd. 13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan Tel: +886-2-8175-9600, Fax: +886 2-8175-9670 Renesas Electronics Singapore Pte. Ltd. 80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949 Tel: +65-6213-0200, Fax: +65-6213-0300 Renesas Electronics Malaysia Sdn.Bhd. Unit 1207, Block B, Menara Amcorp, Amco Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia Unit 1207, Block B, Menara Amcorp, Amcorp Tel: +60-3-7955-9390, Fax: +60-3-7955-9510 Renesas Electronics India Pvt. Ltd. No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India Tel: +91-80-67208700, Fax: +91-80-67208777 Renesas Electronics Korea Co., Ltd. 17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea Tei: +822-558-3737, Fax: +822-558-5338