HI5628EVAL1 User's Manual

Application Note | July 1999 | AN9840

Description

The HI5628EVAL1 evaluation board provides a quick and easy method for evaluating the HI5628IN, 125MSPS Dual 8-Bit, DAC member. Each converter outputs a current into a load resistor to form a voltage which can be measured by using the included SMA connectors. The amount of current out of the DAC is determined by an external resistor and either an internal or external reference voltage. The evaluation board also includes a VME digital interface that is compatible with the HSP-EVAL board, so DDS (Direct Digital Synthesis) can be performed with minimal setup time. A transformer is included to take advantage of differential signal drive.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	CLOCK SPEED
HI5628EVAL1	25	Evaluation Platform	125MHz

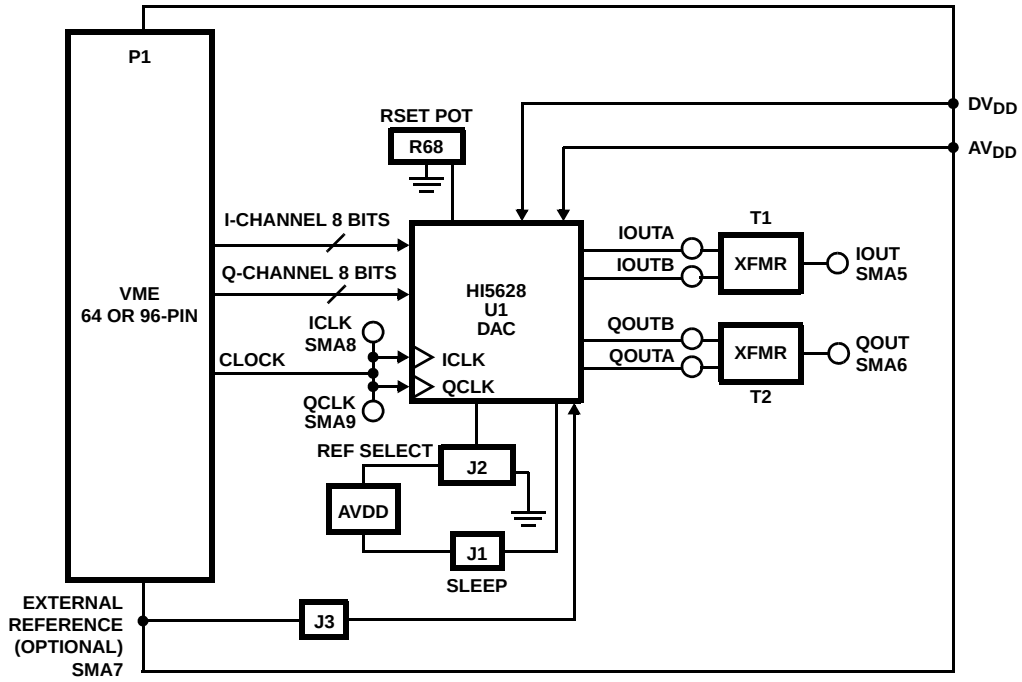
Features

- HI5628IN, 125MSPS, Dual 8-Bit, CMOS DAC
- Simple and Easy to Use
- Standard VME/DSP Interface, HSP-EVAL Compatible
- SMA Outputs with Transformer Option
- Easily Selectable Internal or External Reference

Applications

- I and Q Signal Generation
- Modulated Carrier Generation
- General DAC Performance Evaluation
- Amplitude Modulation Via External Reference

Functional Block Diagram



Functional Description

Overview

The evaluation board is configured to be interfaced using a VME connector. The data input lines are tied together using small, zero ohm resistors on the back side of the board (QD0 is tied to ID0, continued with QD7 connected to ID7; see the schematic, R54, 58-60, 62, 64-66). This is done so that the data can be driven into both of the channels without having to generate two patterns. This aids in simplifying the evaluation of the part. If the user has the ability to generate dual patterns during the evaluation process, these resistors must be removed. Both series and parallel termination resistor footprints are provided, so that the user may customize the termination method. An internal voltage reference is available, as well as a variable resistor for customizing the output current. RF transformers are populated for taking advantage of the complimentary current outputs. They can be disabled from the circuit by removing several zero ohm resistors if a simple load resistor output is desired.

Voltage Reference

The HI5628 has an internal voltage reference (1.16V typical) with a ±60ppm/^{o}C drift coefficient over the full temperature range of the converter. The REFLO pin (15) selects the reference. Access to pin 15 is provided through the center pin of Jumper J2. To enable the internal reference, it is necessary that the jumper be placed such that pin 15 is grounded (J2 is labeled on the board as INT and EXT, for internal and external). The REFIO pin (23) provides access to the internal voltage reference, or can be overdriven if the user wishes to use an external source for the reference. Notice that a 0.1µF capacitor is placed as close as possible to the REFIO pin. This capacitor is necessary for ensuring a quiet reference voltage.

If the user wishes to use an external reference voltage, jumper J3 must be in place and an external voltage reference provided via SMA7, labeled ‘EXT REF’. Jumper J2 must be changed so that pin 16 is tied high (the supply voltage, which is the EXT position of J2) when using an external reference. The recommended limits of the external reference are between 15mV and 1.2V, which provides over 36dB of multiplying capability. Performance of the converter can be expected to decline as the reference voltage is reduced due to the reduction in LSB current size.

If the user wishes to amplitude modulate the reference, the REFIO pin can be overdriven with a waveform. The input multiplying bandwidth of the REFIO input is approximately 1.4MHz. It is necessary that the multiplying signal be DC offset so that the minimum and maximum peaks of the signal are above 0V and less than 1.2V. The output current of each converter is a function of the voltage reference used and the value of R_{SET} (R68 or R35 on the schematic). R68 is a potentiometer that can be used to vary the R_{SET} if the user wishes to explore various output current levels. The board is shipped with R68 set to ~2kΩ. The converter’s performance sometimes improves with reduced output current. R35 is provided if the user wishes to set the output current using a set value. See the ‘Outputs’ section for more information on setting the output current.

The footprints for SMA10 and SMA11 were provided on the evaluation board so that separate multiplying signals could be attached, along with alternate op amps, to overdrive the internal reference op amps via ICOMP1 and QCOMP1 to increase the multiplying bandwidth of the references for DACs I and Q independently. SMA11 was placed next to prototyping area so that an external op amp could be placed between E11 and E7, which provides access to QCOMP1 via a zero ohm resistor, R69. It was intended that this capability also exist between E10 and E6 for access to ICOMP1 so that it could be driven independently if desired, but E6 was mistakenly grounded. So the ability to overdrive ICOMP1 and QCOMP1 exists on this board, but it must be done with a single op amp and signal simultaneously via SMA11, E7, and E11. ICOMP1 cannot be driven independently using SMA10, E6, and E10. R56 should never be populated. See the functional block diagram of the HI5628 in the data sheet and the evaluation board schematic located in this document for more information.

Outputs

The output current of the device is set by choosing R_{SET} and V_{FSADJ} such that the resultant of the following equation is less than 20mA:

$I_{OUT} = 32 \times V_{FSADJ}/R_{SET}$.

For example, using the internal V_{FSADJ} of 1.16V nominal and an R_{SET} (R35 on the schematic) value of 1.86kΩ results in an I_{OUT} of approximately 20mA (maximum allowed). Choose the output loading so that the ‘Output Voltage Compliance Range’ is not violated (-0.3 to 1.25V). If an external V_{REF} is chosen, it should not exceed +1.2V.

The output can be configured to drive a load resistor, a transformer, an operational amplifier, or any other type of output configuration so long as the output voltage compliance range and the maximum output current is not violated.

Load Resistor Output

If the user wishes to use only a load resistor and no transformer, they should remove the zero ohm resistors that connect the outputs to the transformers. These resistors are R51, R57, R70, and R72. See the schematic for details. The output voltage developed is simply a function of the output current multiplied by the output load. Care should be taken to ensure that this voltage does not violate the output compliance range of -300mV to 1.25V.

Differential Output

The board is also configured with the following transformer output which will result in an output voltage amplitude that is twice that of I_{OUT} x Req, where Req is the equivalent resistive loading seen by the current outputs (~12.5Ω = (50//50//25). The transformer used in this circuit is a Mini-Circuits 1:1 RF Transformer, T1-1T. The impedance looking back into the transformer from the 50Ω spectrum analyzer is 50Ω (100Ω/2), so proper termination is achieved and reflections are minimized. The transformer benefits the user by reducing the even-order harmonics and therefore increasing the SFDR (Spurious Free Dynamic Range). It can be taken out of the output by removing the zero ohm jumpers, R51, 57, 70, and 72. With the transformers removed, SMAs 1-4 should be used to measure the output voltages across the included 50Ω loads.

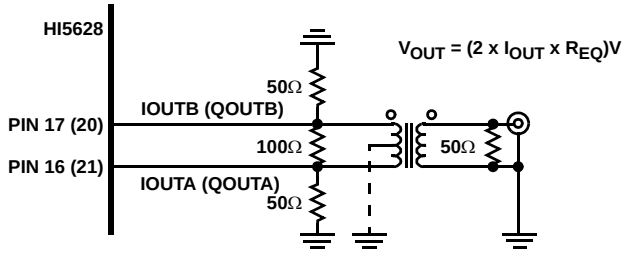


FIGURE 1.

Sleep

The converter can be put into ‘sleep’ mode by connecting pin 8 to either of the converter’s supply voltages. For normal operation, it is recommended that pin 8 be tied to ground. However, the sleep pin does have an active pulldown current, so the pin can be left disconnected. On the evaluation board, jumper J1 is provided for controlling the sleep pin. Remove the jumper from J1 for normal operation and replace it for sleep mode.

Power Supply(ies) and Ground(s)

The user can operate from either a single supply or dual supplies. The DAC is designed to function with the digital and analog voltages at the same value or at different values. The DAC can be driven with a 3 or 3.3V digital supply and a 5V analog supply. In compliance with the absolute maximum ratings for the DAC listed in the datasheet, the digital input voltages should not be more than DV_{DD} + 0.3V. A single power supply wire can be attached to either DV_{DD1} or AV_{DD1}, and then the DV_{DD1} and AV_{DD1} holes jumpered together on the board using regular wire if a single supply is desired. The board uses dual ground planes connected at a single point near the converter (this is the recommended configuration). For dual supply mode, connect a power supply wire to both AV_{DD1} and DV_{DD1} and ground wires to DGND1 and AGND1 independently.

Clock Inputs

The elaborate nature of the clock input circuit (see the schematic) achieves versatility. It provides the means to drive both channels from a single clock via the VME connector, or to drive each with separate clocks via SMAs 8 and 9. Notice that the 0Ω resistors (R28, 29, 50 and 53) are used as jumpers to enable the different clock sources without degrading signal integrity, or they can be replaced by nominal value resistors if series input termination(s) are desired on the clock(s).

Input Termination

For clock rates below 50MSPS, the method of input termination on the data and clock lines could be open, 50Ω, or nominal series, depending on the current drive available from the digital source. The performance of the converter should not vary greatly with the termination method for these update rates. For clock rates above 50MSPS, it may be necessary that 50Ω termination resistors be used on this board to achieve optimum spectral purity. If the digital pattern source cannot drive this load, it is recommended that 200Ω series resistors be used at high clock rates. The board is shipped with 200Ω series resistors on the data and clock lines. Notice that the PCB footprints are available on the board for either termination technique. For high clock rates, adjustment of the timing between the clock and the data may be necessary for optimum performance. When implementing the HI5628 onto a board that contains the digital data/clock source in close proximity to the DAC, it is unlikely that any termination resistors will be required.

Note that the board is also shipped with both input channels tied together via 0Ω, 402 package resistors on the bottom of the board. This is done so that both channels can be evaluated from a single pattern generator. If 50Ω termination is used while the channels are tied together, it should be obvious that they are only needed on one channel, not both; else you will be driving 25Ω.

Getting Started

A summary of the external supplies, equipment, and signal sources needed to operate the board is given below:

1. +3V to +5V power supply(ies) for HI5628.
2. Data Generator capable of generating 8-bit patterns. The HSP-EVAL with the HSP45116 NCOM daughter board is an option (see *‘Learning Your Way Around’*).
3. Clock source (usually part of the Data Generator).
4. Spectrum Analyzer or Oscilloscope for viewing the output of the converter.

Attach a +3V to +5V power supply to the evaluation board connections labeled DVDD1 and AVDD1. Connect the 8 input bits from the data generator to the evaluation board, preferably by using a male, 64 or 96-pin VME (Versa Module Eurocard) connector that mates with the eval board. See the schematic for the correct pin connections. The middle row of the VME is not used on the DAC board, which is why either a

64 or 96-pin connector will work. Connect the clock source to the eval board, also preferably through the VME connector (or using the clock SMAs; see the ‘Clock Inputs’ section for more information). Failure to make clean and short connections to the data input lines and clock source will result in a decrease in spectral performance.

Using a coaxial cable with the proper SMA connector, attach the output of one of the transformers, IOUT or QOUT, to the measurement equipment that will be evaluating the converter’s performance. Make sure that the jumpers are in their proper placement. Consult the ‘Voltage Reference’ section and the ‘Sleep’ section of this document for a definition of the jumpers’ functionality.

Learning Your Way Around

Direct Digital Synthesis

To ensure that everything on the board is configured properly and functional, it is suggested that the following DDS setup be implemented. The board test requires:

1. HI5628EVAL1 Evaluation Board.
2. Spectrum Analyzer.
3. HSP-EVAL Board with the HSP45116 NCOM Daughter Board Attached and included software, NCOMCTRL.
4. Personal Computer (IBM compatible) with a Parallel Port.
5. 50Ω SMA Cable.
6. Two +5V power supplies. One for the DAC Eval Board and one for the HSP Eval Board.

Note: If the HSP-EVAL Board is to be used, it is highly recommended that the user obtain the User’s Manual, the data sheet for the HSP45116 NCOM, and the User’s Manual for the HSP45116-DB. This platform is capable of testing the converter up to 25MSPS, which is the speed of the HSP-EVAL’s on-board clock. The user can choose to substitute this clock with a slower one, but the DSP chip and DSP Eval Board are only designed to work at a maximum of 25MHz (a 52MHz version of this DSP chip does exist but not in this evaluation platform; see the HSP45116A). For testing of the HI5628 at higher speeds, it is recommended that the user obtain a high speed data generator capable of generating 8 bit patterns at the clock speed needed. The HSP45116 NCOM generates two, 16-bit channels of data. HI5628EVAL1 is designed so that both of its input channels mate with both of the DSP’s output channels. The zero ohm resistors that connect the I and Q channels together on the DAC eval board must be removed before using the HSP45116 evaluation board. Also, the DSP Eval Board cannot drive 50Ω.

HSP-EVAL Setup for DDS

Attach the HSP-EVAL and the HSP45116 Daughter Board together; see figure 2. Consult their respective user manuals for details. Connect the HI5628EVAL1 board to the P2 connector of the HSP-EVAL board. Then connect these to an IBM compatible PC via the parallel port. Provide power to both boards. To run the software (NCOMCTRL) that accompanied the HSP evaluation kit, place the diskette into the 3.5” drive of the PC and type:

(drive letter):\,NCOMCTRL

which will run the HSP45116 Control Panel software. Set the control panel’s selections to the following and check one of the outputs of the DACs at either IOUT or QOUT using the spectrum analyzer for a frequency equal to 1.63MHz.

The clock select of the control panel should be set to ‘Osc. CLK’. The control signals should be as follows:

0 $\overline{\text{ENPHREG}}$

0 $\overline{\text{CLROFR}}$

1 $\overline{\text{LOAD}}$

0 $\overline{\text{BINFMT}}$

1 PMSEL

The amplitude of the real output (RIN0-15) should be 8000_{HEX} for full scale output. The center frequency register can be set to $10ABCDEF_{HEX}$ for a 1.63MHz tone. The Offset Frequency, Phase Offset, and Time Accumulator Registers should all be set to zeros. The spurious free dynamic range that can be expected is typically 65dBc with this setup operating at this frequency.

Comments

The HI5628EVAL1 evaluation board is prepared to evaluate the HI5628, 8-bit Dual D/A Converter. It can be modified to evaluate the HI5728, 10-bit Dual D/A Converter with the inclusion of the series resistors that correspond to the 2 LSBs of each channel and the replacement of the HI5628 with the HI5728. The zero ohm resistors to ground on these LSBs will also have to be removed. This allows for easier implementation of future upgrades as the user will only have to order new D/As and not an additional board. The HI5628 and HI5728 share similar pinouts and their respective evaluation boards are identical with only minor changes to the manner in which they are populated. If the user is currently using the 8-bit device, has more bits available digitally, and thinks they might upgrade in the future, it is recommended that the HI5628 be implemented into their system board with similar capabilities.

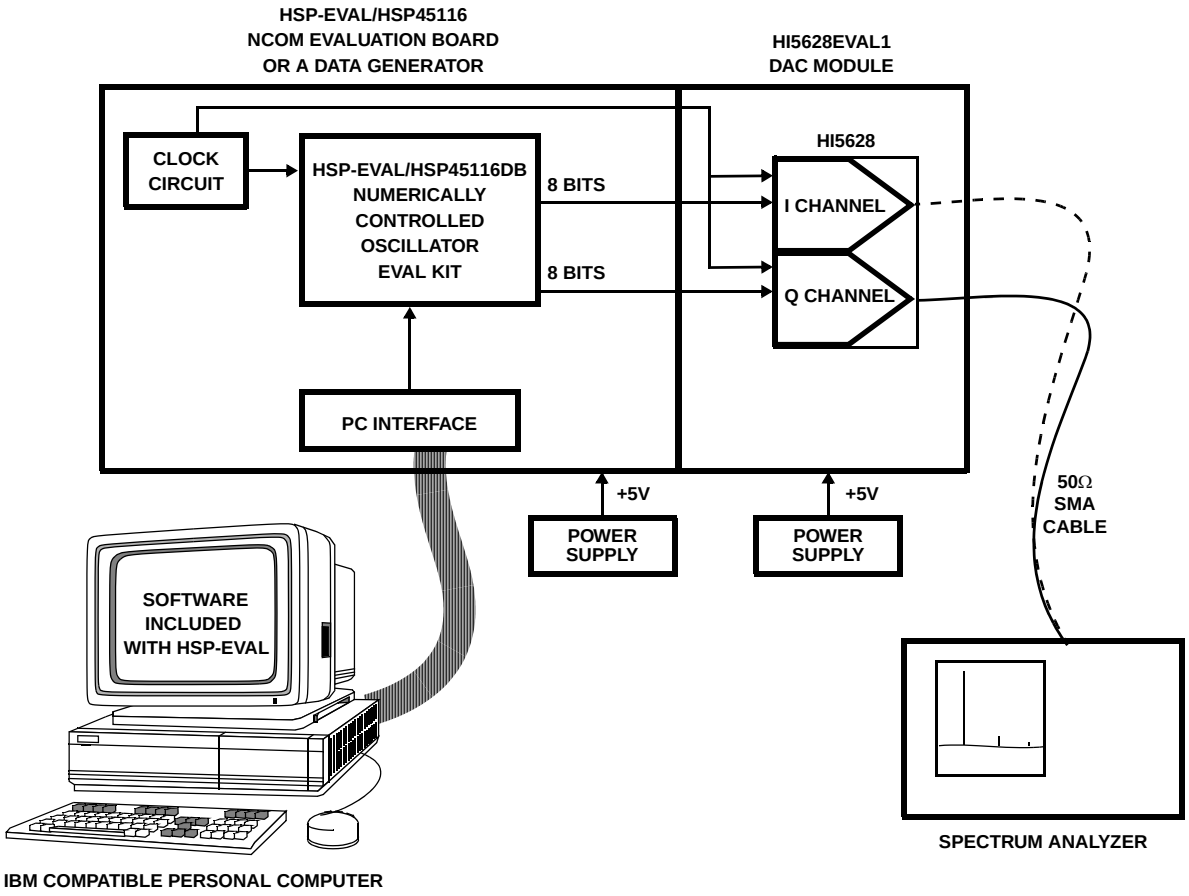


FIGURE 2. INTERSIL HI5628/DDS EVALUATION SYSTEM SETUP BLOCK DIAGRAM

Appendix A Description of Architecture

The segmented current source architecture has the ability to improve the converter's performance by reducing the amount of current that is switching at any one time. In traditional architectures, major transition points required the converter to switch on or off large amounts of current. In a traditional 8-bit R/2R ladder design, for example, the midscale transition required equal amounts of currents switching on and off. In a segmented current source arrangement, transitions such as midscale become one in which you simply have an additional intermediate current source turning on and several minor ones turning off. In the case of the HI5628, there are 31 intermediate current segments that represent the 5 MSBs and 3, binary-weighted current sources representing each of the 3 LSBs. See the Functional Block Diagram in the data sheet for a visual representation. To relate the midscale transition example to the HI5628, consider the following:

Code 01111111 would be represented by 15 intermediate current segments and each of the 3 LSB current sources all turned on. To transition to code 10000000 would simply require turning off the 3 LSB current sources and turning on the next intermediate current segment, bringing the total amount of current switching at this 'major' code transition equal to the same amount switching at 30 other code transition points in the code ramp from 0 to 255, so that the total glitch energy is distributed more evenly.

Appendix B Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
39-32	QD7 (MSB) Through QD0 (LSB)	Digital Data Bit 7, the Most Significant Bit through Digital Data Bit 0, the Least Significant Bit, of the Q channel.
1-5, 48-46	ID7 (MSB) Through ID0 (LSB)	Digital Data Bit 7, the Most Significant Bit through Digital Data Bit 0, the Least Significant Bit, of the I channel.
8	SLEEP	Control Pin for Power-Down Mode. Sleep Mode is active high; connect to ground for Normal Mode. Sleep pin has internal 20µA active pulldown current.
15	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable.
23	REFIO	Reference voltage input if internal reference is disabled and reference voltage output if internal reference is enabled. Use 0.1µF cap to ground when internal reference is enabled.
22	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current Per Channel = 32 x I_{FSADJ}.
14, 24	ICOMP1, QCOMP1	For use in reducing bandwidth/noise of the I and Q channels. Recommended: connect 0.1µF to AV_{DD} as close as possible to each of the pins. These two pins **MUST** be connected together externally.
13, 18, 19, 25	AGND	Analog Ground Connections.
17	IOUTB	The complementary current output of the I Channel. Bits set to all 0s gives full scale current.
16	IOUTA	Current output of the I channel. Bits set to all 1s gives full scale current.
20	QOUTB	The complementary current output of the Q Channel. Bits set to all 0s gives full scale current.
21	QOUTA	Current output of the Q Channel. Bits set to all 1s gives full scale current.
11, 27	NC	No Connect. Recommended: Connect to ground.
12, 26	AV_{DD}	Analog Supply (+2.7V to +5.5V).
6, 7, 10, 28, 30, 31, 41, 44	DGND	Digital Ground.
9, 29, 40, 45	DV_{DD}	Supply voltage for digital circuitry (+2.7V to +5.5V).
43	ICLK	Clock input for I Channel. Positive edge of clock latches data.
42	QCLK	Clock input for Q Channel. Positive edge of clock latches data.

Appendix C Circuit Board Layout

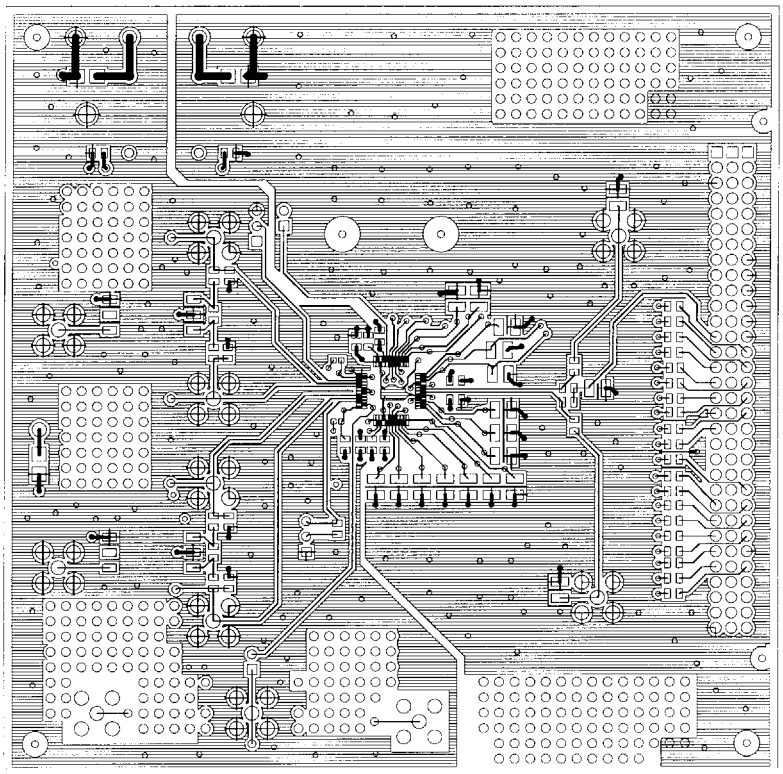


FIGURE 3. PRIMARY SIDE

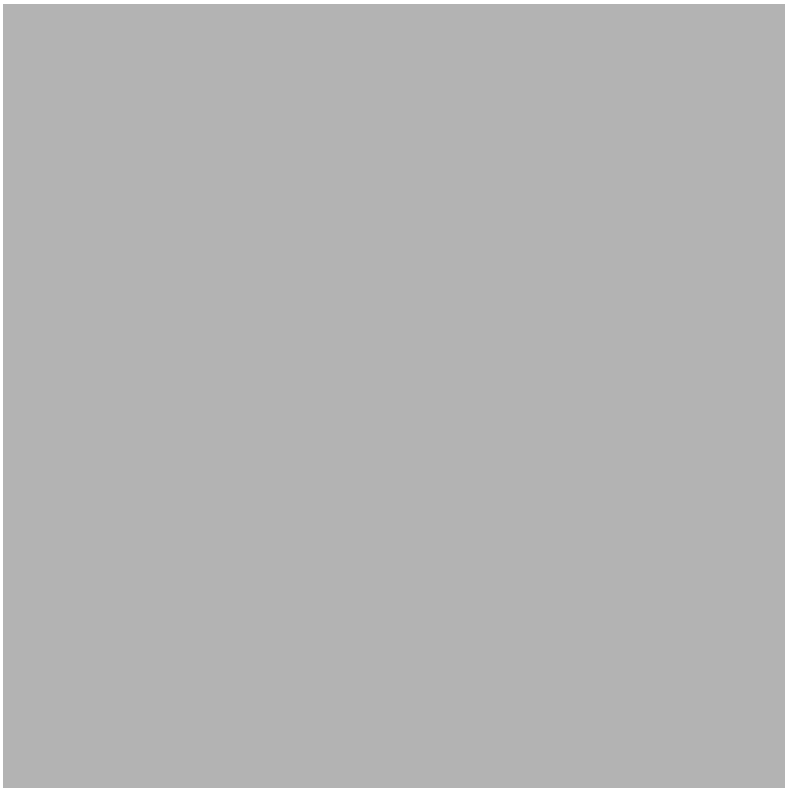


FIGURE 4. GROUND LAYER (2)

Appendix C Circuit Board Layout (Continued)

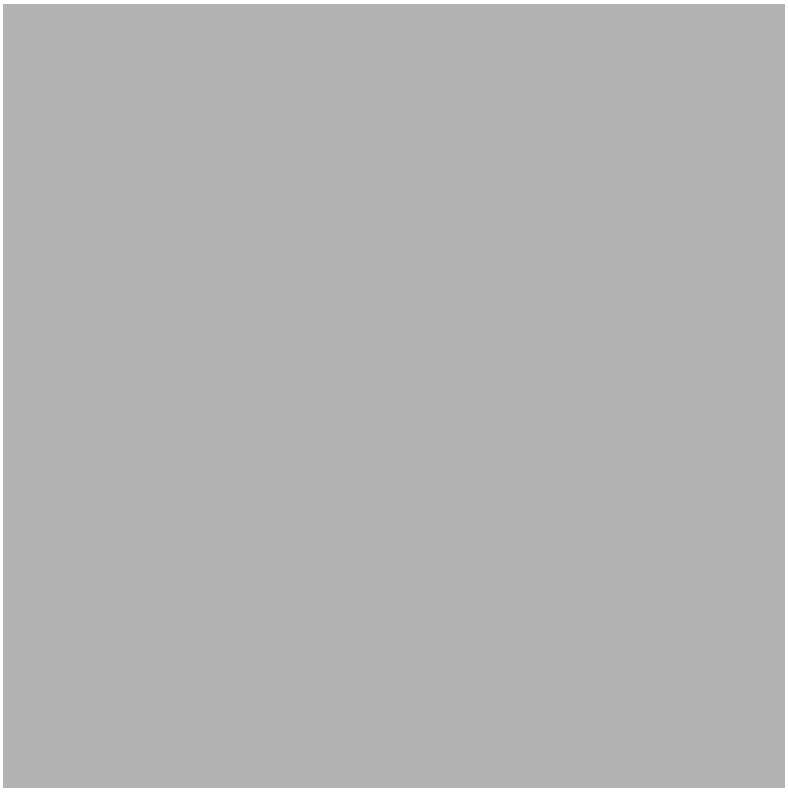


FIGURE 5. POWER LAYER (3)

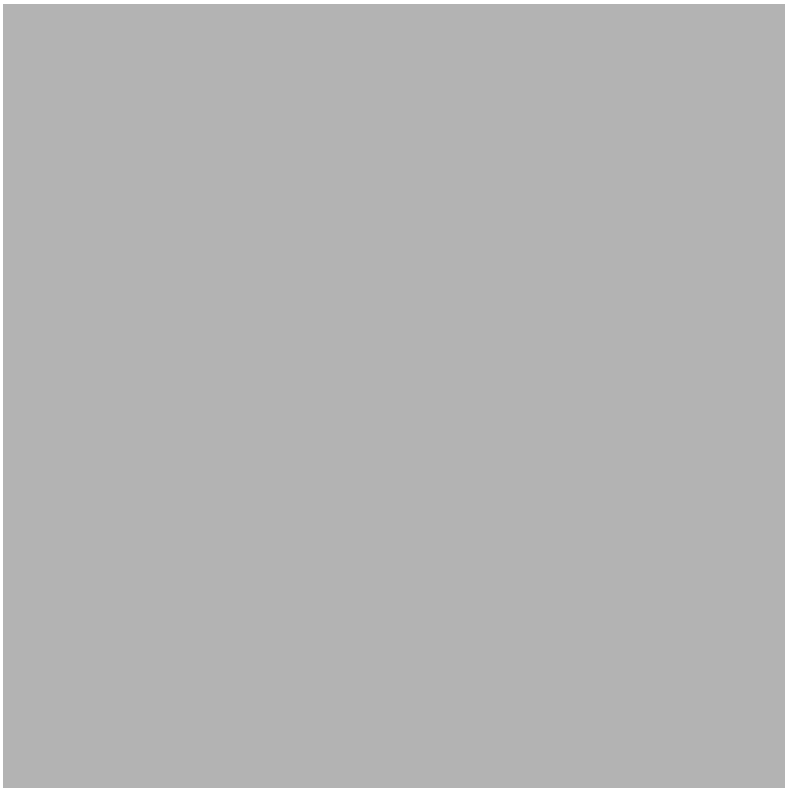
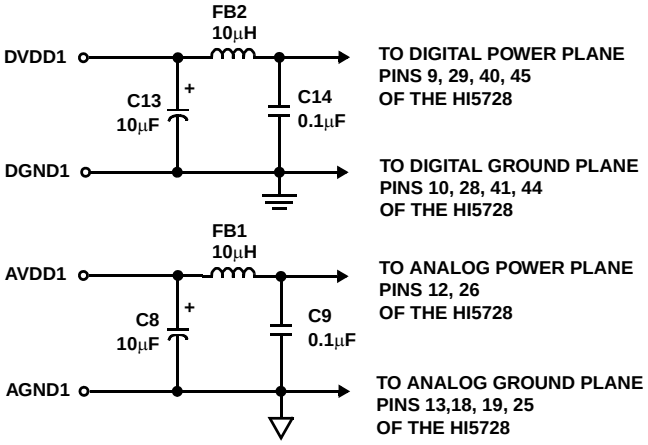


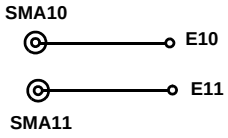
FIGURE 6. SECONDARY SIDE

Power Supply Input Circuit

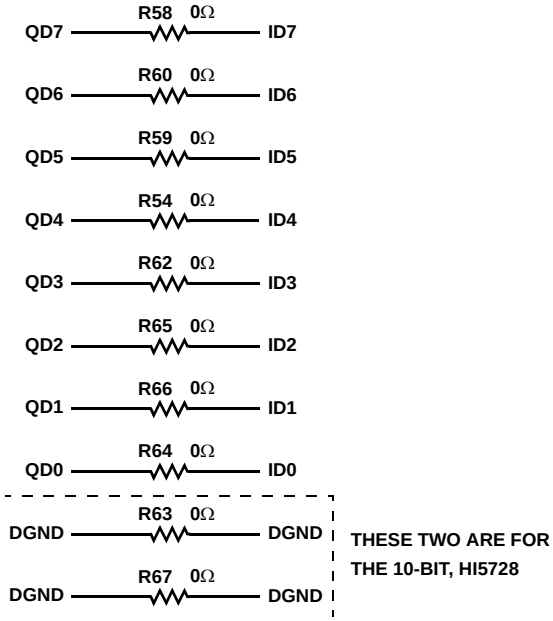


NOTE: DV_{DD} and AV_{DD} can be tied together for single supply operation. AGND1 and DGND1 are tied together at a single point. See text for further explanation.

Extra SMAs (See 'Voltage Reference' text for explanation.)



Digital Input Additional Connections



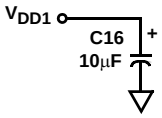
Ground Symbol Definition

= ANALOG GROUND (AGND1)

= DIGITAL GROUND (DGND1)

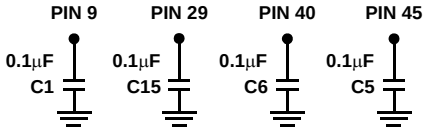
Extra Power Supply Input Located Near Output Proto Area

(Used if additional circuity is added in the proto area)

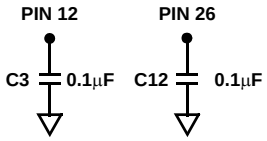


Power Supply Decoupling

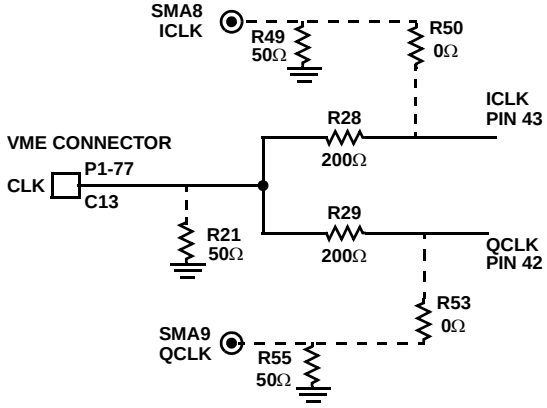
DV_{DD} Power Decoupling Capacitors

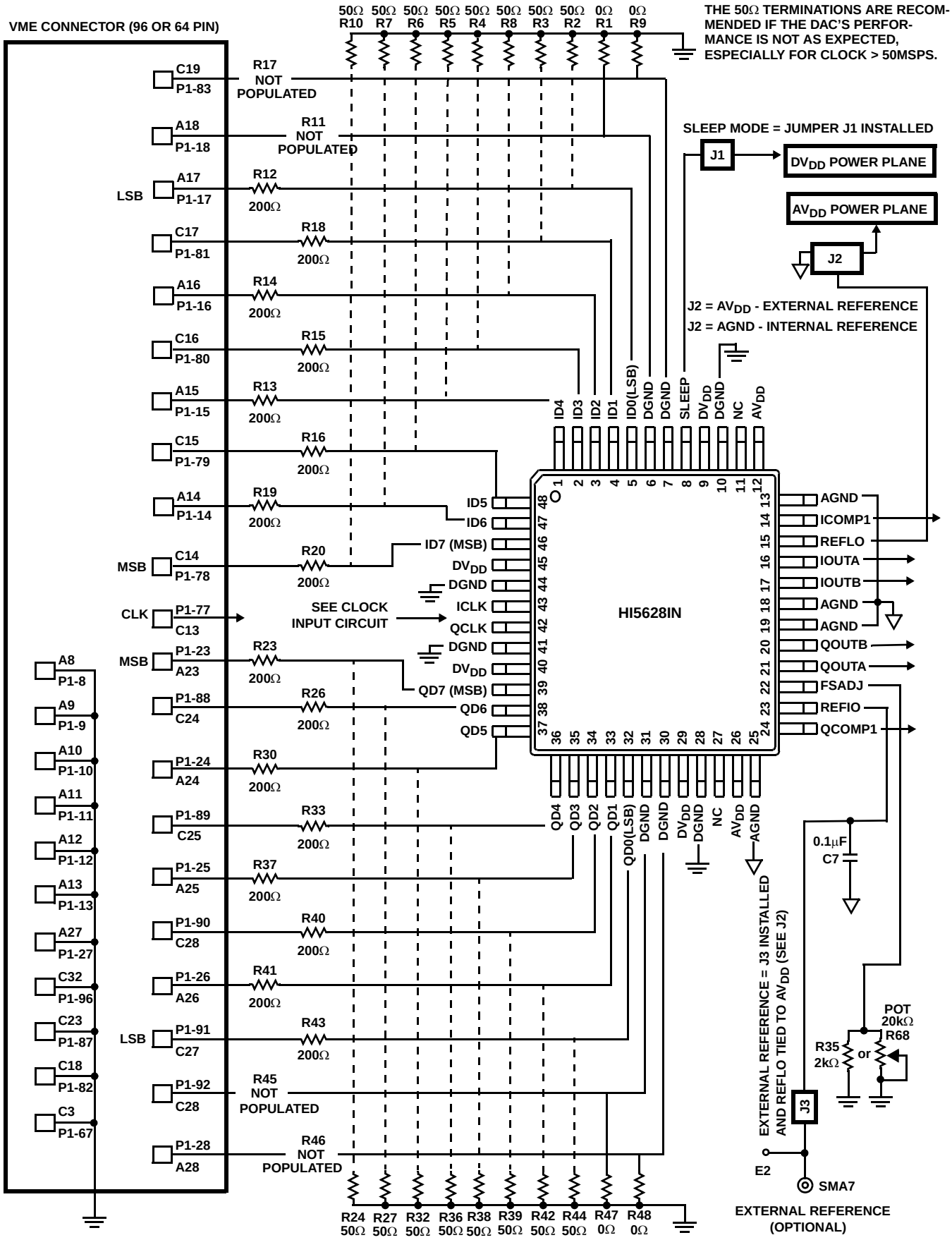


AV_{DD} Power Decoupling Capacitors

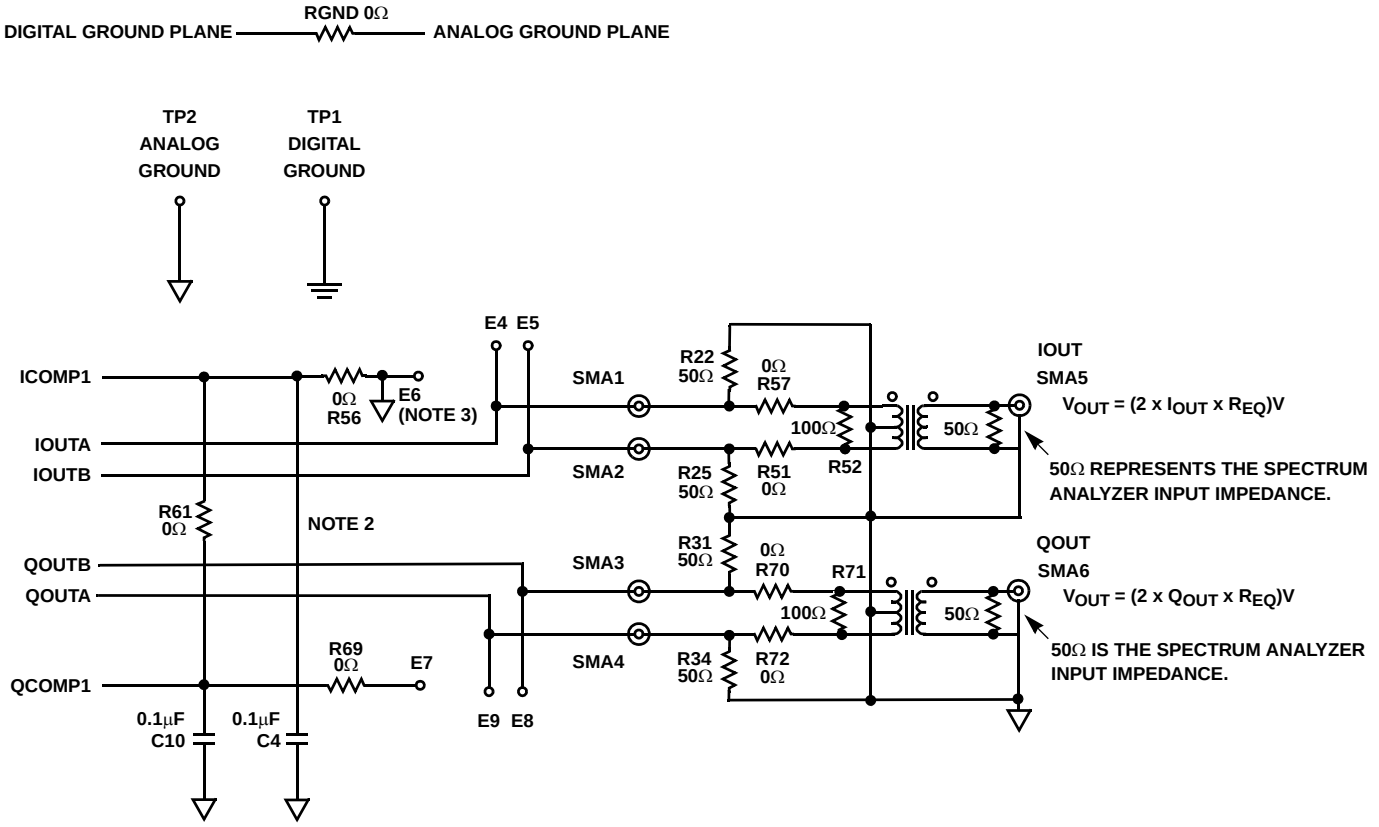


Clock Input Circuit (See 'Clock Inputs' Text)




VME CONNECTOR (96 OR 64 PIN)
50Ω R10
50Ω R7
50Ω R6
50Ω R5
50Ω R4
50Ω R8
50Ω R3
50Ω R2
0Ω R1
0Ω R9
THE 50Ω TERMINATIONS ARE RECOMMENDED IF THE DAC'S PERFORMANCE IS NOT AS EXPECTED, ESPECIALLY FOR CLOCK > 50MSPS.
SLEEP MODE = JUMPER J1 INSTALLED
J1
DVDD POWER PLANE
AVDD POWER PLANE
J2
J2 = AVDD - EXTERNAL REFERENCE
J2 = AGND - INTERNAL REFERENCE
C19 P1-83
R17 NOT POPULATED
A18 P1-18
R11 NOT POPULATED
LSB A17 P1-17
R12 200Ω
C17 P1-81
R18 200Ω
A16 P1-16
R14 200Ω
C16 P1-80
R15 200Ω
A15 P1-15
R13 200Ω
C15 P1-79
R16 200Ω
A14 P1-14
R19 200Ω
MSB C14 P1-78
R20 200Ω
CLK P1-77 C13
SEE CLOCK INPUT CIRCUIT
MSB P1-23 A23
R23 200Ω
P1-88 C24
R26 200Ω
P1-24 A24
R30 200Ω
P1-89 C25
R33 200Ω
P1-25 A25
R37 200Ω
P1-90 C28
R40 200Ω
P1-26 A26
R41 200Ω
LSB P1-91 C27
R43 200Ω
P1-92 C28
R45 NOT POPULATED
P1-28 A28
R46 NOT POPULATED
A8 P1-8
A9 P1-9
A10 P1-10
A11 P1-11
A12 P1-12
A13 P1-13
A27 P1-27
C32 P1-96
C23 P1-87
C18 P1-82
C3 P1-67
ID4 ID3 ID2 ID1 ID0(LSB) DGND DGND SLEEP DVDD DGND NC AVDD
ID5
ID6
ID7 (MSB)
DVDD
DGND
ICLK
QCLK
DGND
DVDD
QD7 (MSB)
QD6
QD5
HI5628IN
AGND
ICOMP1
REFLO
IOUTA
IOUTB
AGND
AGND
QOUTB
QOUTA
FSADJ
REFIO
QCOMP1
QD4 QD3 QD2 QD1 QD0(LSB) DGND DGND DVDD DGND NC AVDD AGND
0.1μF C7
EXTERNAL REFERENCE = J3 INSTALLED AND REFLO TIED TO AVDD (SEE J2)
POT 20kΩ R68
R35 2kΩ
or
J3
E2
SMA7
EXTERNAL REFERENCE (OPTIONAL)
R24 50Ω
R27 50Ω
R32 50Ω
R36 50Ω
R38 50Ω
R39 50Ω
R42 50Ω
R44 50Ω
R47 0Ω
R48 0Ω

Ground Connection



NOTES:

1. AGND1 and DGND1 are tied together at a single point near the DAC. Optimum placement for Rgnd was found by iteration while observing the spectral noise floor.
2. ICOMP1 and QCOMP1 MUST be tied together externally!
3. *E6 was mistakenly grounded so R56 should not be populated! E7, however, is correct and can be used to overdrive the internal reference op amp for increasing the multiplying bandwidth.

Appendix D Evaluation Board Bill Of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION
U1	1	HI5628IN, Intersil Dual, 125MSPS, 8-bit D/A Converter
C8, 13, 16	3	10μF, Tantalum Chip Capacitor, EIA Case B, 10%, 10V
C1-7, 9-12, 14, 15	13	0.1μF, Ceramic Chip Capacitor, 0805, 10%, 10V
R2-8, 10, 21, 24, 27, 32, 36, 38, 39, 42, 44, 49, 55	19	Included, not populated, 51Ω, Chip Resistor, 1210, 5%, 1/4W
R12-16, 18-20, 23, 26, 28, 29, 30, 33, 37, 40, 41, 43, 51, 57, 70	21	200Ω, Chip Resistor, 0805, 1/8W
R52, 71	2	100Ω, Chip Resistor, 0805, 1/8W
R22, 25, 31, 34	4	51Ω, Chip Resistor, 0805, 1/8W
R54, 58, 59, 60-62, 64-66, 69	11	0Ω, Chip Resistor, 0402, 1/10W
R68	1	20kΩ, Potentiometer Resistor, 3296W, 1/8W(Shipped set to ~2kΩ)
R35	1	(2kΩ, Chip Resistor, 0805, 1/8W) (Not Populated)
J1, J2	2	1x2 Header
J3	1	1x3 Header
T1, 2	2	Mini-Circuits, T1-1T KK81, Z1:Z2 ratio of 1:1
P1	1	64-Pin Eurocard, Right Angle
SMA1-11	11	SMA Straight Jack, PCB Mount
FB1, 2	2	10μH, Ferrite Bead
TP1, 2	2	Test Point
-	3	1x2 Header Jumper
-	-	DUT Clamp
-	4	Plastic Legs, 1/2”
R50, 53, Rgnd	3	(0Ω, Chip Resistor, 0805, 1/8W) (R50, 53 Not Populated)
R56	1	(0Ω, Chip Resistor, 0402, 1/10W) (Not Populated)

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029