

# ISL24003

## Multi-Channel Buffers Plus VCOM Driver

FN6118  
Rev 0.00  
December 7, 2005

The ISL24003 integrates eighteen gamma buffers and a single  $V_{COM}$  buffer for use in large panel LCD displays of 10" and greater. Half of the gamma channels in each device are designed to swing to the upper supply rail, with the other half designed to swing to the lower rail. The output capability of each channel is 10mA continuous, with 120mA peak. The gamma buffers feature a 10MHz 3dB bandwidth specification and a 9V/ $\mu$ s slew rate.

The  $V_{COM}$  amplifier is designed to swing from rail to rail. The output current capability of the  $V_{COM}$  in the ISL24003 is 60mA continuous, 150mA peak, and a slew rate of 50V/ $\mu$ s.

### Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG DWG. #
ISL24003IRZ (Note)	ISL24003IRZ	-	44 Ld 7x7mm QFN (Pb-free)	MDP0046
ISL24003IRZ-T7 (Note)	ISL24003IRZ	7"	44 Ld 7x7mm QFN (Pb-free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### Features

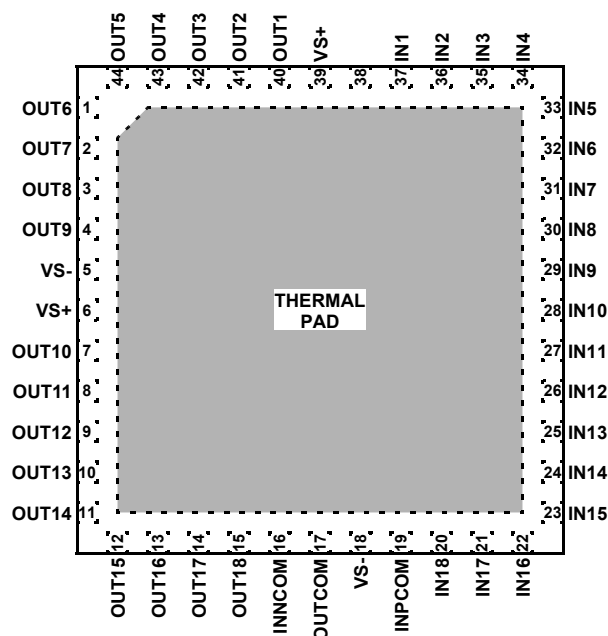
- 18-channel gamma buffers
  - 9 channels swing to the upper supply
  - 9 channels swing to the lower supply
  - 10mA continuous output current
- Single  $V_{COM}$  amplifier
  - 180mA short circuit output current
  - 35MHz -3dB Bandwidth
  - 70V/ $\mu$ s slew rate
- Low supply current
- Pb-free plus anneal available (RoHS compliant)

### Applications

- TFT-LCD monitors
- LCD televisions
- Industrial flat panel displays

### Pinout

ISL24003  
(44 LD 7X7MM QFN)  
TOP VIEW



**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Supply Voltage between  $V_{S+}$  and  $V_{S-}$  ..... +18V  
 Input Voltage .....  $V_{S-} - 0.5\text{V}$ ,  $V_{S+} + 0.5\text{V}$   
 Maximum Continuous Output Current ( $V_{OUT1-18}$ ) ..... 10mA  
 Maximum Continuous Output Current ( $V_{OUTA}$ ) ..... 60mA

Power Dissipation ..... See Curves  
 Maximum Die Temperature ..... +125°C  
 Storage Temperature ..... -65°C to +150°C  
 Ambient Operating Temperature ..... -40°C to +85°C

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:** All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**Electrical Specifications**  $V_{S+} = +15\text{V}$ ,  $V_{S-} = 0$ ,  $R_L = 10\text{k}\Omega$ ,  $C_L = 10\text{pF}$  to 0V,  $T_A = 25^\circ\text{C}$  unless otherwise specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V <sub>OS</sub>	Input Offset Voltage	V <sub>CM</sub> = 0V		2	20	mV
TCV <sub>OS</sub>	Average Offset Voltage Drift	(Note 1)		5		μV/°C
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = 0V		2	50	nA
R <sub>IN</sub>	Input Impedance			10		MΩ
C <sub>IN</sub>	Input Capacitance			1.35		pF
A <sub>V</sub>	Voltage Gain	1V ≤ V <sub>OUT</sub> ≤ 14V	0.992		1.008	V/V
CMIR	Input Voltage Range	IN1 to IN9	1.5		V <sub>S</sub> +	V
		IN10 to IN18	0		V <sub>S</sub> + -1.5	V
INPUT CHARACTERISTICS (V <sub>COM</sub> BUFFER)						
V <sub>OS</sub>	Input Offset Voltage	V <sub>CM</sub> = 7.5V		1	15	mV
TCV <sub>OS</sub>	Average Offset Voltage Drift	(Note 1)		3		μV/°C
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = 7.5V		2	50	nA
R <sub>IN</sub>	Input Impedance			10		MΩ
C <sub>IN</sub>	Input Capacitance			1.35		pF
V <sub>REG</sub>	Load Regulation	V <sub>COM</sub> = 7.5V, -60mA < I <sub>L</sub> < 60mA	-25		+20	mV
CMIR <sub>COM</sub>	Input Voltage Range V <sub>COM</sub>		0		V <sub>S</sub> +	V
A <sub>VOL</sub>	Open Loop Gain	R <sub>L</sub> = 1kΩ	55	70		dB
CMRR	Common Mode Rejection Ratio		50	65		dB
OUTPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V <sub>OH</sub>	High Output Voltage - (Output 1-2)	V <sub>IN</sub> = 15V, I <sub>O</sub> = 5mA	14.85	14.9		V
	High Output Voltage - (Output 3-9)		14.8	14.85		V
		High Output Voltage - (Output 10-18)	V <sub>IN</sub> = 13.5V, I <sub>O</sub> = 5mA	13.45	13.5	
V <sub>OL</sub>	Low Output Voltage - (Output 1-9)	V <sub>IN</sub> = 1.5V, I <sub>O</sub> = 5mA		1.5	1.55	V
	Low Output Voltage - (Output 10-16)	V <sub>IN</sub> = 0V, I <sub>O</sub> = 5mA		150	200	mV
	Low Output Voltage - (Output 17-18)			100	150	mV
I <sub>SC</sub>	Short Circuit Current		100	130		mA
OUTPUT CHARACTERISTICS (V <sub>COM</sub> BUFFER)						
V <sub>OH</sub>	High Level Saturated Output Voltage	V <sub>S</sub> ⁺ = 15V, I <sub>O</sub> = -5mA, V <sub>I</sub> = 15V	14.85	14.9		V
V <sub>OL</sub>	Low Level Saturated Output Voltage	V <sub>S</sub> ⁺ = 15V, I <sub>O</sub> = -5mA, V <sub>I</sub> = 0V		0.1	0.15	V
I <sub>SC</sub>	Short Circuit Current		150	180		mA

**Electrical Specifications**  $V_{S+} = +15V$ ,  $V_{S-} = 0$ ,  $R_L = 10k\Omega$ ,  $C_L = 10pF$  to 0V,  $T_A = 25^\circ C$  unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY PERFORMANCE</b>						
PSRR	Power Supply Rejection Ratio	Reference buffer $V_S$ from 5V to 15V	50	80		dB
		$V_{COM}$ buffer, $V_S$ from 5V to 15V	55	80		dB
$I_S$	Total Supply Current		8.0	11.5	15.5	mA
<b>DYNAMIC PERFORMANCE (BUFFER AMPLIFIERS)</b>						
SR	Slew Rate (Note 2)		4.5	9		V/ $\mu s$
$t_S$	Settling to +0.1% ( $A_V = +1$ )	( $A_V = +1$ ), $V_O = 2V$ step		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$ , $C_L = 10pF$		10		MHz
CS	Channel Separation			70		dB
<b>ISL24003 DYNAMIC PERFORMANCE (<math>V_{COM}</math> AMPLIFIERS)</b>						
SR	Slew Rate (Note 2)	$-4V \leq V_{OUT} \leq 4V$ , 20% to 80%	50	70		V/ $\mu s$
$t_S$	Settling to +0.1% ( $A_V = +1$ )	( $A_V = +1$ ), $V_O = 2V$ step		350		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$ , $C_L = 10pF$		35		MHz
CS	Channel Separation			70		dB

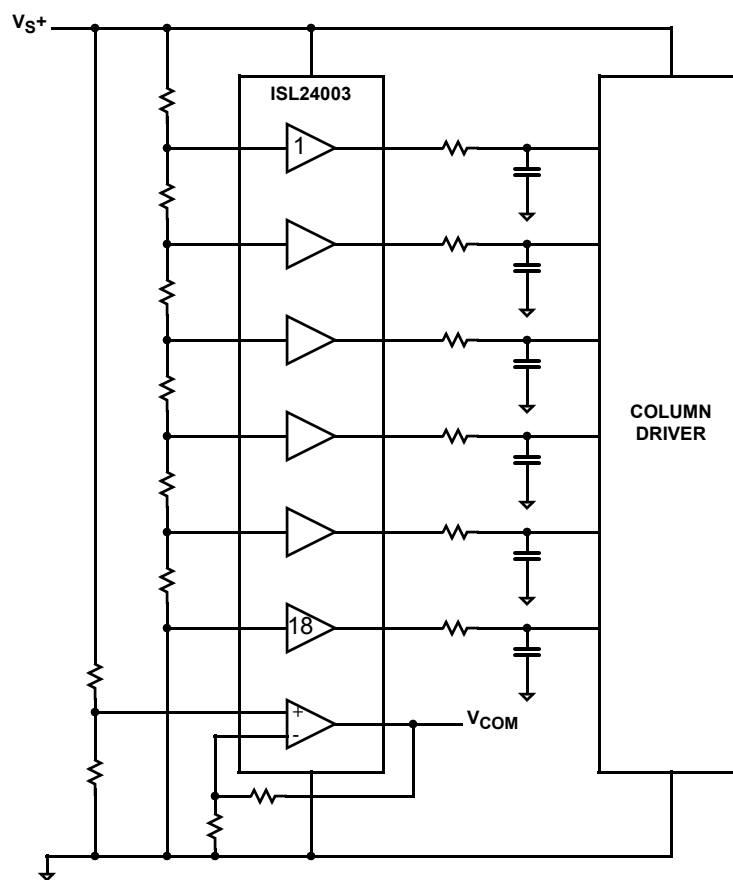
## NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.

## Pin Descriptions

PIN NAME	ISL24003	PIN FUNCTION
6, 39	VS+	Positive supply voltage
40-44, 1-4	OUT1-9	Output gamma channel 1-9
7-15	OUT10-18	Output gamma channel 10-18
16	INNCOM	Negative Input $V_{COM}$
17	OUTCOM	Output, $V_{COM}$
5, 18	VS-	Negative supply voltage
19	INPCOM	Positive Input $V_{COM}$
20-28	IN10-18	Input gamma channel 10-18
29-37	IN1-9	Input gamma channel 1-9
38	NC	No connect

## Block Diagram



NOTE: ISL24003 integrates 18 gamma buffers.

## Typical Performance Curves

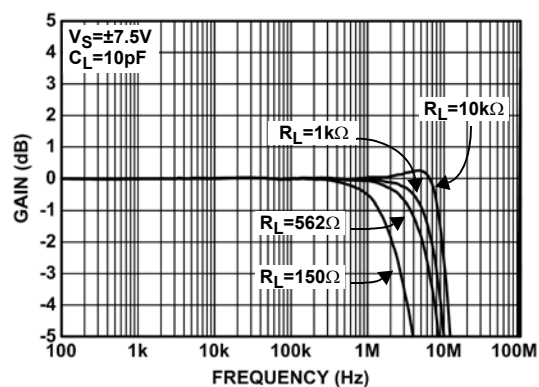


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS  $R_{LOAD}$  (BUFFER)

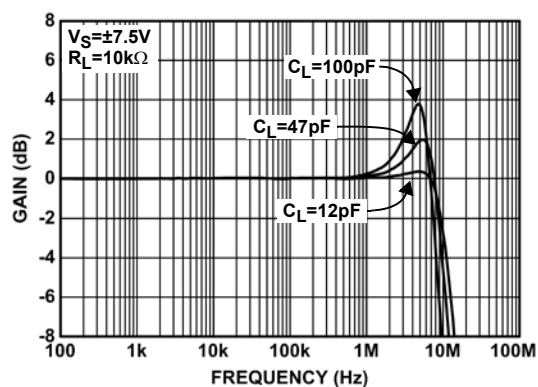


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS  $C_{LOAD}$  (BUFFER)

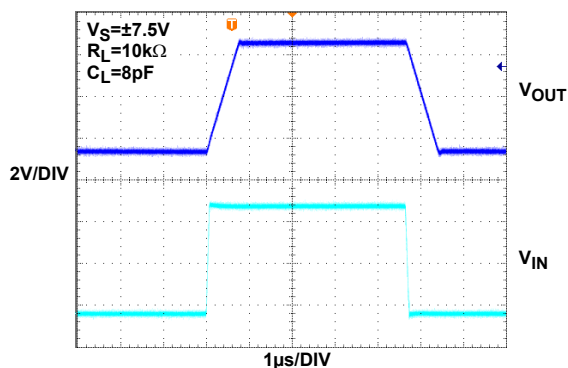


FIGURE 3. LARGE SIGNAL TRANSIENT RESPONSE (BUFFER)

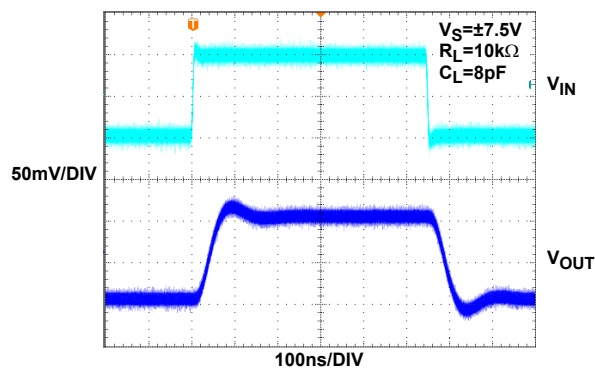


FIGURE 4. SMALL SIGNAL TRANSIENT RESPONSE (BUFFER)

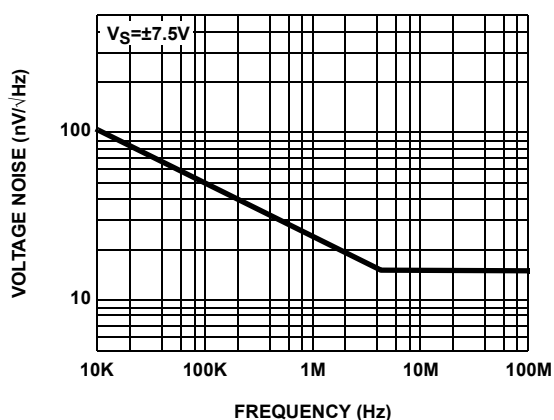


FIGURE 5. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (BUFFER)

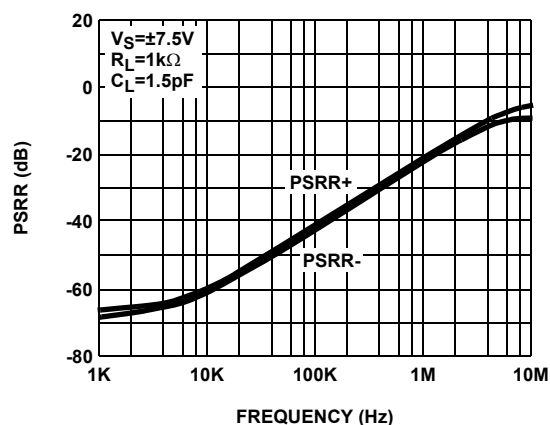


FIGURE 6. PSRR vs FREQUENCY (BUFFER)

## Typical Performance Curves (Continued)

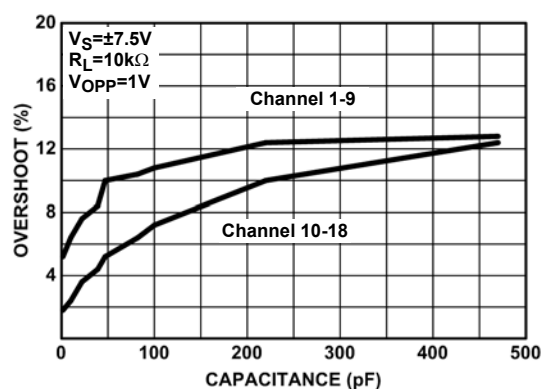
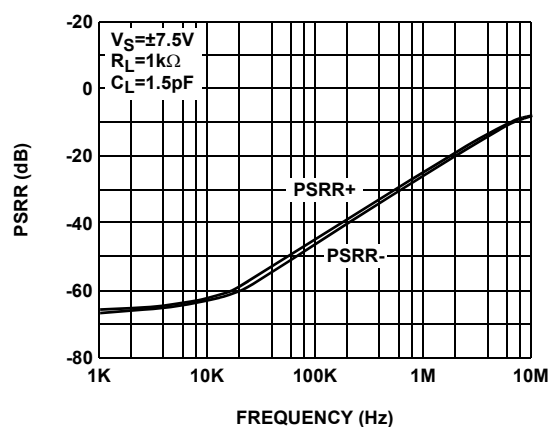
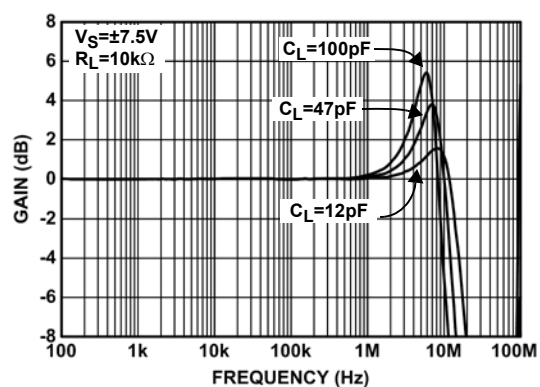
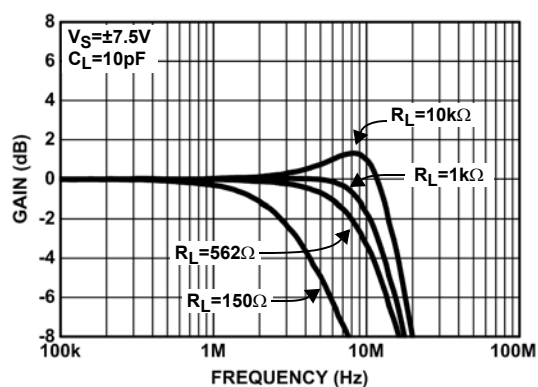
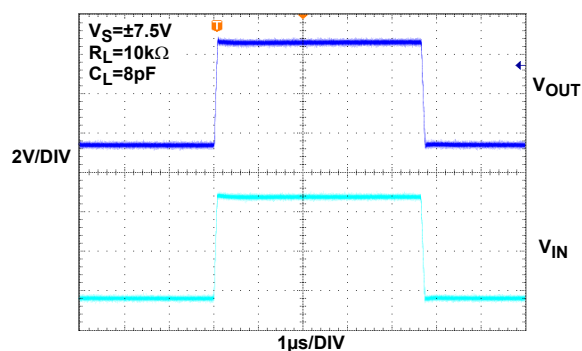
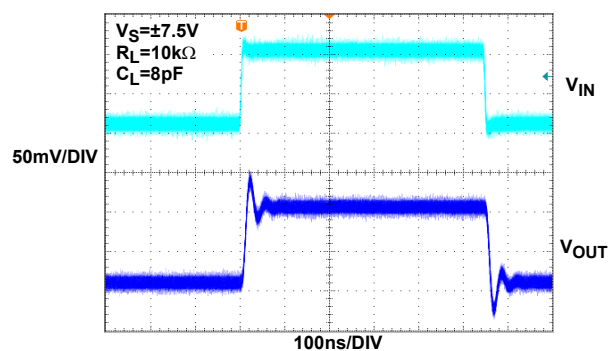


FIGURE 7. OVERSHOOT vs CAPACITANCE LOAD (BUFFER)

FIGURE 8. PSRR vs FREQUENCY ( $V_{COM}$ )FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS  $C_{LOAD}$  ( $V_{COM}$ )FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS  $R_{LOAD}$  ( $V_{COM}$ )FIGURE 11. LARGE SIGNAL TRANSIENT RESPONSE ( $V_{COM}$ )FIGURE 12. SMALL SIGNAL TRANSIENT RESPONSE ( $V_{COM}$ )

## Typical Performance Curves (Continued)

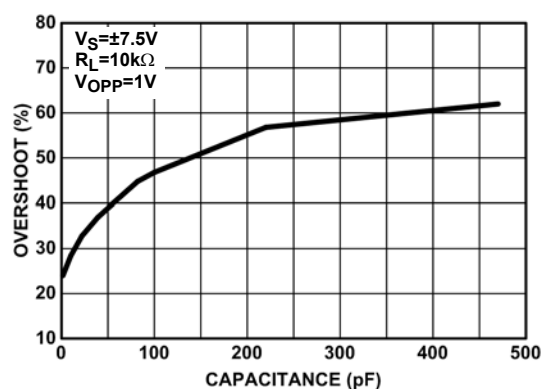
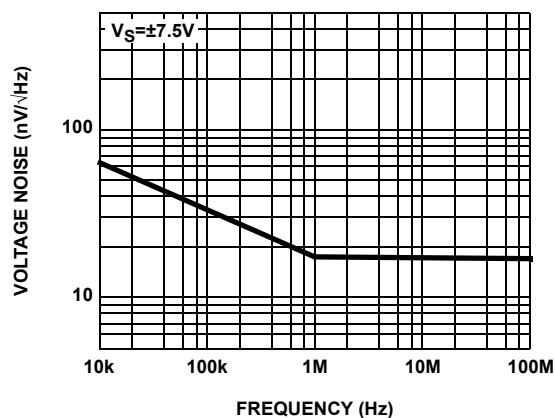
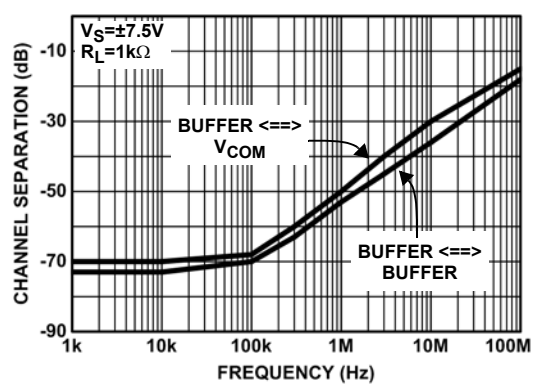
FIGURE 13. OVERSHOOT vs CAPACITANCE LOAD ( $V_{COM}$ )FIGURE 14. INPUT NOISE SPECIAL DENSITY vs FREQUENCY ( $V_{COM}$ )

FIGURE 15. CHANNEL SEPARATION

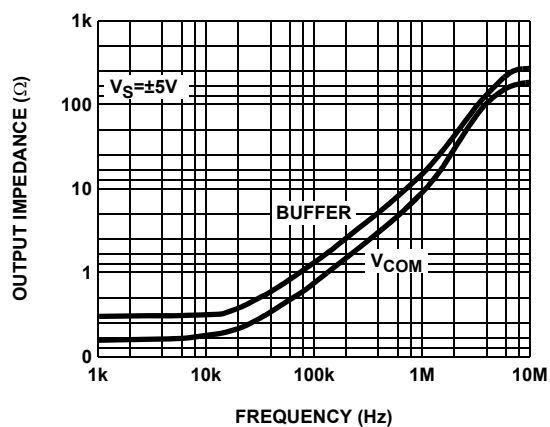


FIGURE 16. OUTPUT IMPEDANCE vs FREQUENCY

## Description of Operation and Application Information

### Product Description

The ISL24003 are fabricated using a high voltage CMOS process. They exhibit rail to rail input and output capability and have very low power consumption. When driving a load of 10K and 12pF, the buffers have a -3dB bandwidth of 10MHz and exhibit 9V/μs slew rate. The V<sub>COM</sub> amplifier has a -3dB bandwidth of 12MHz and exhibit 10V/μs slew rate.

### Input, Output, and Supply Voltage Range

The ISL24003 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range from 4.5V to 16.5V.

The input common-mode voltage range of the ISL24003 within 500mV beyond the supply rails. The output swings of the buffers and V<sub>COM</sub> amplifier typically extend to within 100mV of the positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage even closer to each supply rails.

### Output Phase Reversal

The ISL24003 are immune to phase reversal as long as the input voltage is limited from V<sub>S</sub>- -0.5V to V<sub>S</sub>+ +0.5V. Although the device's output will not change phase, the input's over-voltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diode placed in the input stage of the device begin to conduct and over-voltage damage could occur.

### Output Drive Capability

The ISL24003 do not have internal short-circuit protection circuitry. The buffers will limit the short circuit current to 120mA and the V<sub>COM</sub> amplifier will limit the short circuit current to 150mA if the outputs are directly shorted to the positive or the negative supply. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output continuous current never exceeds 10mA for the buffers and 60mA for the V<sub>COM</sub> amplifier. These limits are set by the design of the internal metal interconnections.

### The Unused Buffers

It is recommended that any unused buffers should have their inputs tied to ground plane.

### Power Dissipation

With the high-output drive capability of the ISL24003, it is possible to exceed the 125°C "absolute-maximum junction temperature" under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load

conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

- T<sub>JMAX</sub> = Maximum junction temperature
- T<sub>AMAX</sub> = Maximum ambient temperature
- θ<sub>JA</sub> = Thermal resistance of the package
- P<sub>DMAX</sub> = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = V_S \times I_S + \sum i \times [(V_{S+} - V_{OUTi}) \times I_{LOADi}] + (V_{S+} - V_{OUT}) \times I_{LA}$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \sum i \times [(V_{OUTi} - V_{S-}) \times I_{LOADi}] + (V_{OUT} - V_{S-}) \times I_{LA}$$

when sinking.

where:

- i = 1 to total number of buffers
- V<sub>S</sub> = Total supply voltage of buffer and V<sub>COM</sub>
- I<sub>S</sub> = Total quiescent current
- V<sub>OUTi</sub> = Maximum output voltage of the application
- V<sub>OUT</sub> = Maximum output voltage of V<sub>COM</sub>
- I<sub>LOADi</sub> = Load current of buffer
- I<sub>LA</sub> = Load current of V<sub>COM</sub>

If we set the two P<sub>DMAX</sub> equations equal to each other, we can solve for the R<sub>LOAD</sub>'s to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P<sub>DMAX</sub> exceeds the device's power derating curves.

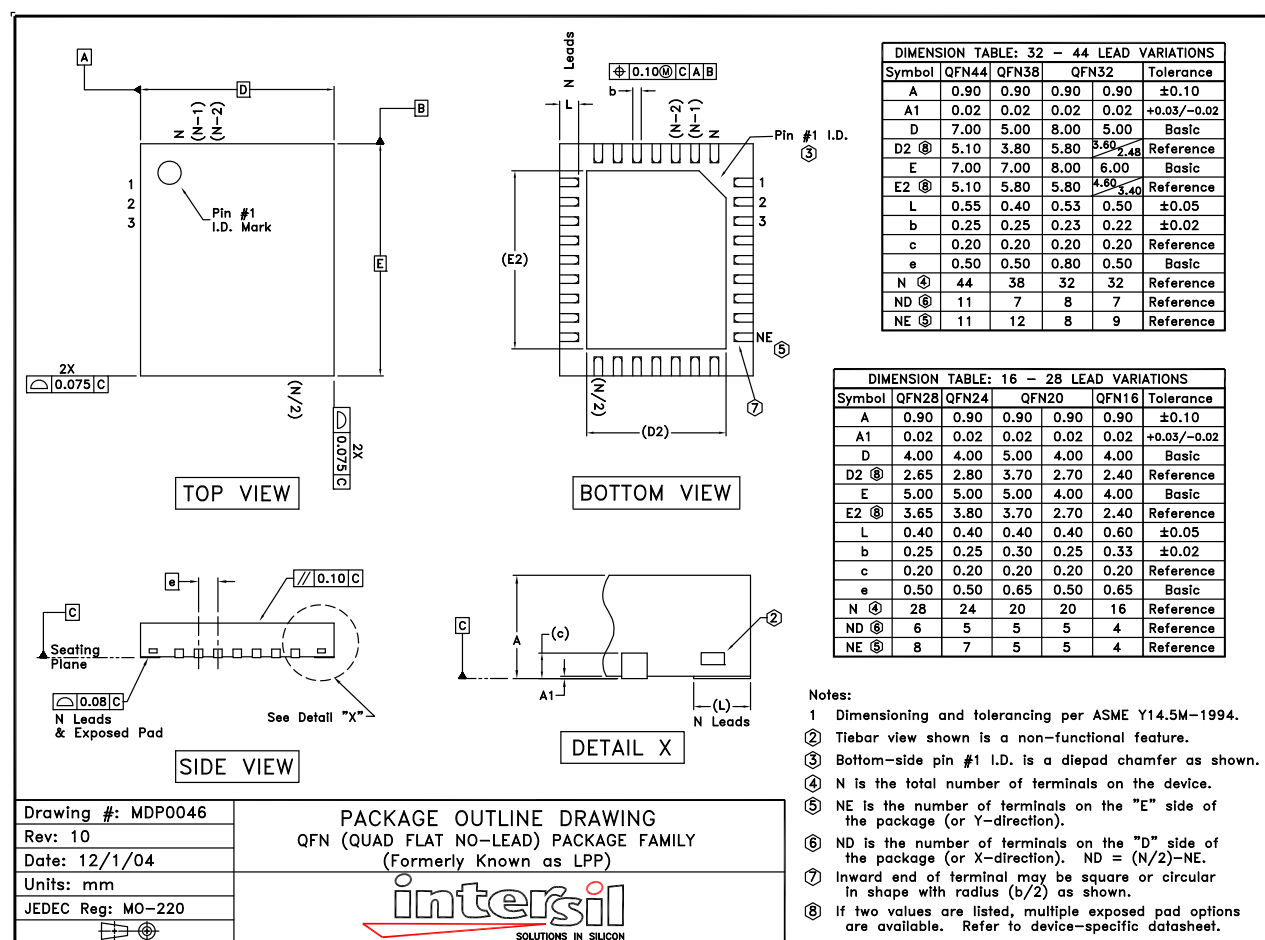


**Power Supply Bypassing and Printed Circuit Board Layout**

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the  $V_{S-}$  pin is connected to ground, one 0.1 $\mu$ F ceramic capacitor should be placed from the  $V_{S+}$  pin to ground. A 4.7 $\mu$ F tantalum capacitor should then be connected from the  $V_{S+}$  pin to ground. One 4.7 $\mu$ F capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

***Important Note: The metal plane used for heat sinking of the device is electrically connected to the negative supply potential ( $V_{S-}$ ). If  $V_{S-}$  is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad must be isolated from any other power planes.***

# QFN Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <<http://www.intersil.com/design/packages/index.asp>>

© Copyright Intersil Americas LLC 2005. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)